Function-Based Cost Modeling for Wafer Manufacturing And its Application to Strategic Management

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Abstract - In this paper a function-based cost modeling methodology is proposed, which consists of three major steps: function analysis, cost modeling and strategic management. A system analysis technique IDEF0 is used as the basis of function analysis. Function-based cost models are then constructed, and with which pie-chart analysis and sensitivity analysis provide managers important information for critical decision-making. A generic photolithography process is used as a test bed. Results show that IDEF0 is an effective tool for modeling IC manufacturing processes and the manufacturing cost based on the proposed methodology is more easily and accurately calculated than the current practices.

INTRODUCTION

As the capital investment for wafer fabrication increases significantly, effective fab operations has become even more important than before. To be competitive, IC manufacturers must accurately model and control the manufacturing cost. In real practices, operational performance metrics such as cycle time, WIP and throughput are more often characterized in evaluating the overall operational performance. The resulting wafer manufacturing cost, however, is usually poorly quantified.

Several reasons contribute to the difficulties of modeling and control of the wafer manufacturing cost. First, the IC manufacturing processes are typically very complicated and the technology is changing rapidly. Second, it is very difficult for both accounting people and manufacturing people to communicate in the same "language". In many practices the cost accounts are empirically classified and the manufacturing overhead is allocated based on a pre-assigned accounting budget. The resulting manufacturing cost provides little or distorted information for effective operations evaluation. On the other hand, the activity-based costing (ABC) [1] method has been proposed as a better methodology, but in real practices seldom adopted by the IC manufacturers. It is either too complicated to model and implement the detailed "activities" in IC processes or there is no effective tool for defining such activities.

To overcome these difficulties, a function-based cost modeling methodology is proposed in this paper. To be more specific, the goals of this paper are three folds:

- to model the functions of IC manufacturing process using a system analysis technique: IDEF0,
- to design a function-based cost model using a generic photolithography process as the test bed, and
- to apply the cost model to strategic management.

Figure 1 illustrates the framework of the proposed methodology. It consists of three major steps: Function Analysis, Cost Modeling, and Strategic Management. As can be seen, the manufacturing processing functions are first modeled and decomposed using a system analysis technique called IDEF0 (Integrated CAM DEFinition method) [2]. With this technique, the Input, Constraint, Output, and Mechanism (ICOM) of a process flow can be clearly identified and abstracted. Transformation rules are used to transform the ICOM into three cost accounts: direct material (DM), direct labor (DL), and manufacturing overhead (MOH). Each wafer's manufacturing cost is then calculated based on the allocation of these cost accounts. Once the model is complete and verified, managers can perform pie-chart analysis or sensitivity analysis for strategic management. In the following sections, we will describe the three major steps.

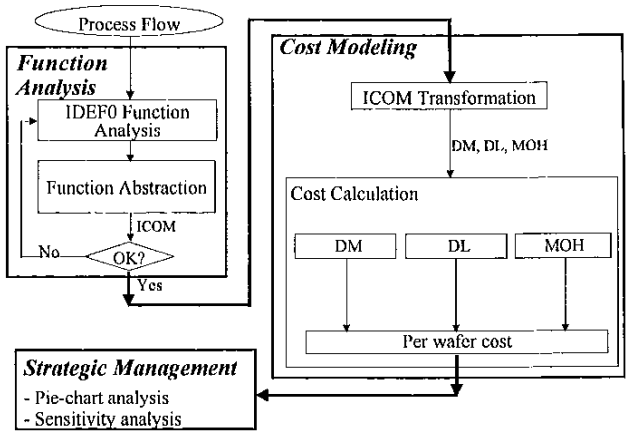

Figure 1: Framework of the proposed methodology

FUNCTION ANALYSIS

In the proposed methodology, we use IDEF0 as the basis of functional modeling. Originally developed by US Air Force, IDEF0 has been recognized as a standard methodology to better understand complex systems and to aid the implementation of changes [2]. Basically, it is a

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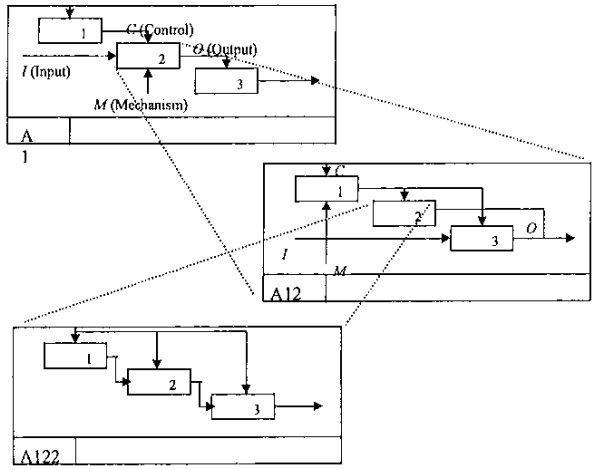
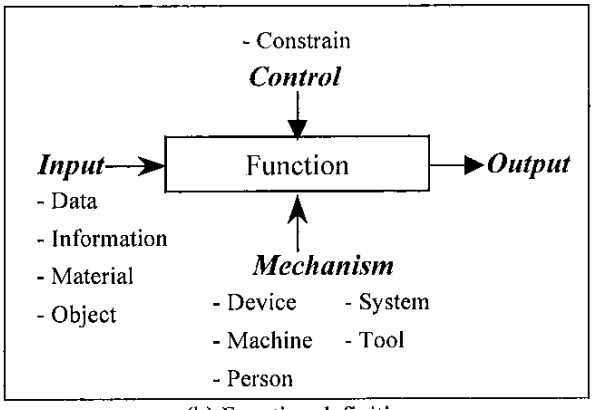
decomposition of processing functions. The higher level functions are explored into lower level functions (Figure 2a). For each function, a box represents the function that is performed and the connecting arrows represent the *Input*, *Constraint*, *Output*, and *Mechanism* (ICOM) of the function (Figure 2b).



(a) Decomposition of functions

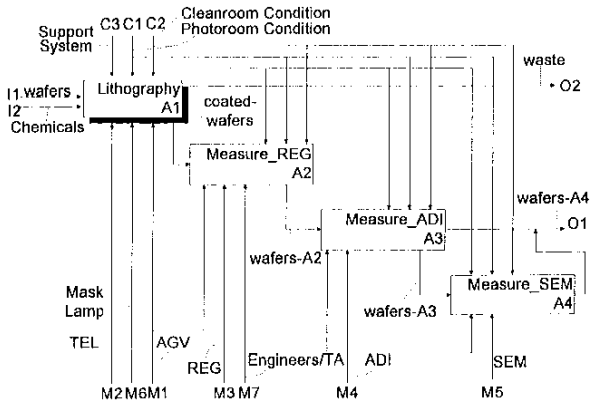


(b) Function definition

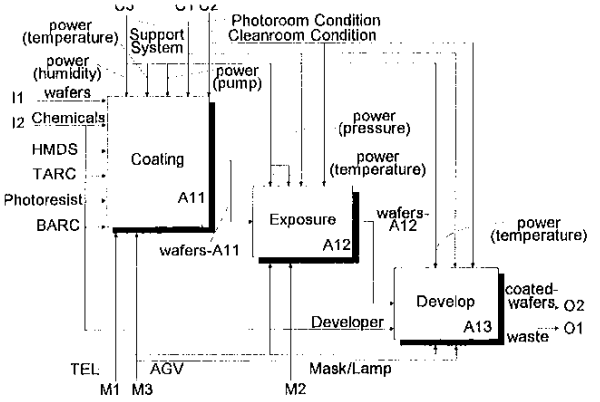
Figure 2: IDEF0 structural functional analysis

To test the feasibility of applying IDEF0 to modeling IC manufacturing processes, a generic photolithography process is modeled. As shown in Figure 3a, the photolithography process is decomposed into four first-level functions, "Lithography", "Measure_ADI", "Measure_REG" and "Measure_SEM". Boxes with shaded area can be further decomposed into the next level of functions. Figure 3b shows the second-level decomposition on "Lithography".

Although it is possible to continue the decomposition into the lowest-level function or activity, a "desired level of decomposition" should be determined so that the model can represent the process flow well enough without being too complicated to implement. Because the systematic and graphical representation of IDEF0 models provides an easy common language for discussions among people with different disciplines, an agreement, such as the level of decomposition, would not be difficult to reach. In brief, the IDEF0 modeling can rapidly model the manufacturing processes based on the requirements in a dynamic environment and facilitate the communication between different functional groups in a concurrent development environment. For the photolithography process example, the complete set of ICOM is abstracted in Table 1.



(a) First-level decomposition



(b) Second-level decomposition on Lithography

Figure 3: Decomposition of photolithography process

Input	Control	Output	Mechanism
Wafers	Clean room con.	Coated wafers	TA
HMDS	Photo room con.	Waste	Engineers
BARC	Support system	Wafers	Mask
TARC	Power		Lamp
Photoresist	Water		AGV
EBR			TEL
Developer			REG
Coated wafers			ADI
			SEM
			Insurance
			Maintenance

Table 1: Abstracted ICOM of the photolithography process

COST MODELING

In the next step of cost modeling, a transformation from the ICOM into different cost accounts is first performed. Each

wafer's manufacturing cost is then calculated based on the allocation of these cost accounts.

The transformation is accomplished by a set of rules that transform the ICOM into three cost accounts: direct material (DM), direct labor (DL), and manufacturing overhead (MOH). For the photolithography process, these rules are:

- transform Input to DM
- transform Control to MOH
- transform waste in Output to MOH
- transform TA in Mechanism to DL, and transform the rest of Mechanism to MOH

Coated wafers in Input and Output are work-in-process wafers so they won't be transformed into any cost account (to prevent double calculation). Wafers in Output are finished wafers so they won't be transformed either. With these rules applied to the ICOM listed in Table 1, we have the transformed results shown in Table 2. Here italic items are added to represent the detailed transformed cost accounts that will be used as the basis of cost calculation.

	Input	Control	Output	Mechanism
DM	*Pd_Wafer* *C_Wafer* Wafer *Chemical* HMDS BARC TARC Photoresist EBR Developer			
DL				*DL* TA
MOH		*FAB_dep* *Misc.* Clean room con. Photo room con. Support system *Water* Water *Power* Power	*Waste* Waste	*IDL* Engineers *EQ_dep* AGV、TEL REG、ADI、SEM *IDM* Lamp *Mask* Mask *Insurance* Insurance *Maintenance* Maintenance

Table 2: Transformation results of photolithography process

Figure 4 illustrates the procedure of cost calculation. Per wafer cost is calculated based on the allocation of DM, DL and MOH. For DM, per wafer cost is calculated by tracing the direct usage of PD_wafer (production wafer), C_wafer (control wafer) and Chemicals. For DL, per wafer cost is also calculated by tracing the direct usage of TA (technical assistant or operator). Formula (not shown here) for each account allocation have been derived based on the discussion with fab engineers and managers.

For MOH, per wafer cost calculation is more complicated. Here we further divide MOH into two categories: MOH_EQ for equipment and MOH_FAB for fab facilities. As shown in Figure 4, both categories adopt a two-stage procedure and an equipment-based approach to allocate the cost accounts to per wafer cost. For MOH_EQ, the first stage aggregates all the cost accounts associated with equipment i and calculates the hourly rate for equipment i. Then in the second stage per wafer cost due to equipment i is obtained by multiplying the hourly rate by the equipment usage hours. Per wafer cost due to MOH_EQ is given by:

$$\text{Per wafer cost} = \sum_{i=1} (\text{EQ\_hourly rate})_i \times (\text{EQ\_hr})_i \qquad (1)$$

For MOH_FAB, it has the similar procedure except in the first stage for the calculation of hourly rate of equipment i. The allocation of all the cost accounts to each equipment i is based on the equipment's space ratio in the fab. In the second stage, it uses the similar procedure as defined in (1).

It is interesting to point out how the function-based costing (FBC) approach differs from the traditional cost accounting practices and the ABC approach in terms of wafer manufacturing cost modeling. Compared with the traditional approach, FBC approach:

- classifies all cost accounts more systematically;
- allocates the cost accounts based on the real usage of resource instead of a pre-assigned budget;
- adopts an equipment-based procedure to allocate manufacturing overhead; and
- provides a more accurate method for the calculation of wafer manufacturing cost.

Compared with the ABC approach, FBC approach:

- provides a tool for defining the functions or activities at the desired level of abstraction;
- adopts a two-stage procedure (same as the ABC approach) in allocating manufacturing overhead costs but only uses equipment usage as the cost driver; and
- provides an easy-to-implement method for the calculation of wafer manufacturing cost.

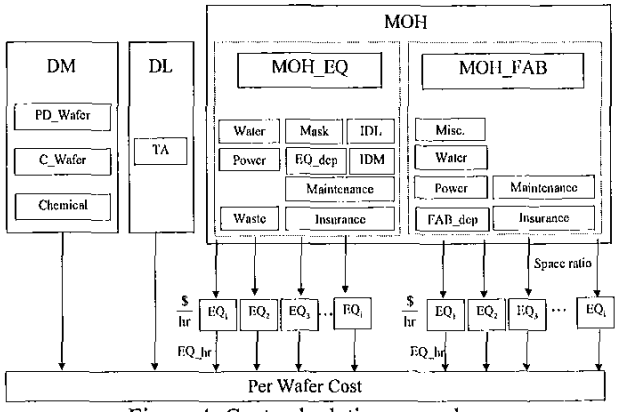
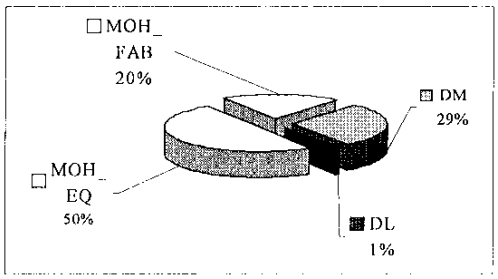


Figure 4: Cost calculation procedure

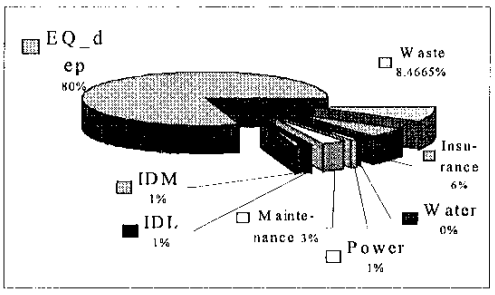
STRATEGIC MANAGEMENT

Once the model is verified, managers can perform pie-chart analysis or sensitivity analysis for strategic management.

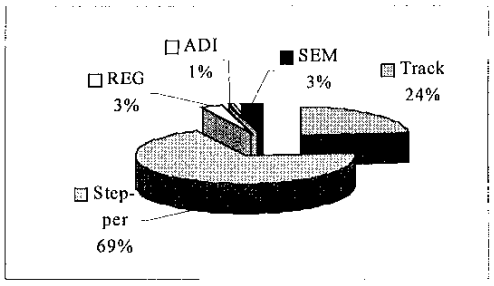
In the pie-chart analysis, cost breakdown of different levels is presented graphically. Figure 5 illustrates one example of pie-chart analysis resulted from a photolithography process. This model's input data were taken from a local fab. As can been seen in Figure 5a, manufacturing overhead constitutes the largest portion (70%) of the manufacturing cost. If managers want to drill down the information, manufacturing overhead can be further broken down. Figures 5b shows the breakdown results of MOH_EQ by cost accounts. Equipment depreciation here constitutes the largest potion of MOH_EQ. Alternatively, managers can also breakdown the cost by equipment types. Figure 5c shows the breakdown results of MOH_EQ by equipment types. The stepper, one of the most critical equipment in semiconductor manufacturing, constitutes the largest portion of MOH_EQ. The pie-chart analysis provides managers important information for decision making.



(a) Total breakdown



(b) MOH_EQ breakdown by cost accounts



(c) MOH_EQ breakdown by equipment types

Figure 5: Pie-chart analysis results

In the sensitivity analysis, managers can perform what-if analysis and identify critical factors that affect the manufacturing cost most. For example in Figure 6, by changing the utilization rate by 10% on each machine, managers can easily see that the stepper has the largest impact on the total cost. This is not a surprising result as the stepper is usually the bottleneck equipment in the photolithography process. What happens if managers increase the throughput of stepper? As shown in Table 3, total cost will decrease as the stepper's throughput (WPH) increases. However, there is a limit to the decrease of total cost as the bottleneck will switch to another equipment. This is clearly indicated in Table 3, in which the idle ratios of the track machine becomes zero as the throughput of the stepper increases by 6.3%.

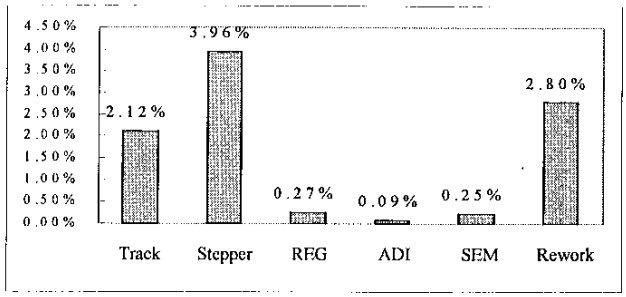


Figure 6: Sensitivity analysis of equipment utilization

△Stepper WPH	Idle ratio					△Total
	Track	Stepper	REG	ADI	SEM	
initial	0.0280	0	0.4342	0.4543	0.4738	--
1%	0.0247	0	0.4423	0.4638	0.4840	- $ 0.2302
2%	0.0201	0	0.4418	0.4635	0.4839	- $ 2.9720
3%	0.0154	0	0.4413	0.4632	0.4837	- $ 5.7138
4%	0.0107	0	0.4407	0.4629	0.4836	- $ 8.4556
5%	0.0061	0	0.4402	0.4625	0.4835	- $ 11.1974
6%	0.0014	0	0.4397	0.4622	0.4834	- $ 13.9392
6.1%	0.0009	0	0.4396	0.4622	0.4834	- $ 14.2134
6.2%	0.0005	0	0.4396	0.4622	0.4833	- $ 14.4876
6.3%	0.0000	0	0.4395	0.4621	0.4833	- $ 14.7557

Table 3: Sensitivity analysis of increasing stepper's WPH

CONCLUSIONS

In this paper a function-based cost modeling methodology is proposed. A system analysis technique IDEF0 is used as the basis of function analysis. Cost models are then constructed, and with which pie-chart analysis and sensitivity analysis provide managers important information for critical decision-making. Results show that IDEF0 is an effective tool for modeling IC manufacturing processes and the manufacturing cost based on this methodology is more easily and accurately calculated than the current practices.

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