A High-Speed Scalable Shift-Register Based On-Chip Serial Communication Design for SoC Applications

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Abstract—In this paper, a high-speed, scalable on-chip serial transmission design is proposed to provide 2Gb/s transmission bandwidth for SoC applications. By using the dynamic control technology and the single-phase pulse-triggered TSPC shift register design, we can provide high-speed on-chip serial transmission. Moreover, the shift register design is a scalable design. By using the proposed method, we can provide 3 times wider bandwidth as compared to the prior art design [6].

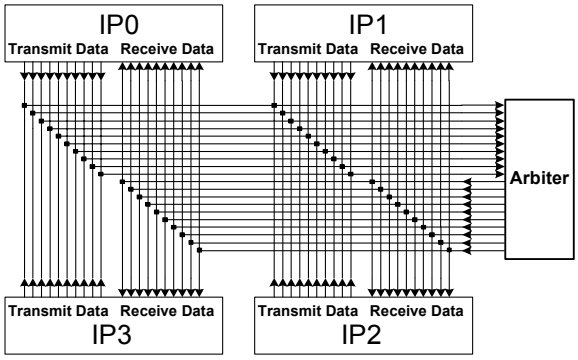
I. INTRODUCTION

System-on-a-chip (SoC) designs provide possible and economical method to integrate complex systems on a single chip. However, the exponential growth in speed and integration levels of intellectual properties (IPs) has increased the interconnection complexity, which dominates the performance of SoC design [1-6]. As a result, On-Chip Networks (OCN) have been actively studied recently to reduce the wire complexity and solve the problems of scalability in the bus-based SoC communication [2-4]. On the other hand, serial communication is the key technology to overcome the wire complexity to make the implementation of OCN is possible and practical [5,6]. However, the bandwidth of OCN transmission will be limited by the serial communication clock frequency. High-speed design becomes the critical demand in the on-chip serial communication architecture. Therefore, we propose a new technology to overcome the speed bottleneck in the on-chip serial communication design.

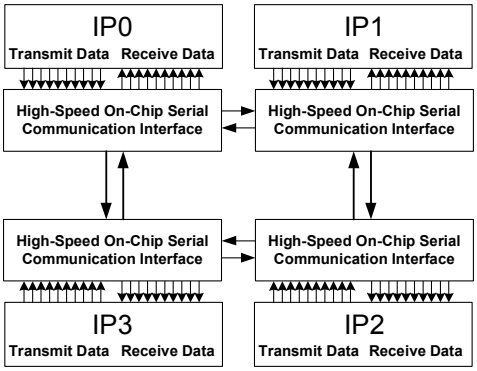
As illustrated in Fig. 1(a), on-chip parallel-shared bus communication requires enormous wire interconnections between IPs. In our proposed on-chip high-speed serial communication architecture, as illustrated in Fig. 1(b), wire complexity can be greatly reduced by 90% and the speed bottleneck can be overcome to provide 2Gb/s transmission bandwidth. Moreover, the proposed design can be easily scalable for higher-bandwidth designs.

II. PROPOSED ON-CHIP SERIAL COMMUNICATION DESIGN

The proposed high-speed on-chip serial communication architecture is constructed by the transmitter with parallel to serial converter and the receiver with serial to parallel converter, as illustrated in Fig. 2(a).



(a) On-Chip Parallel-Shared Bus Communication



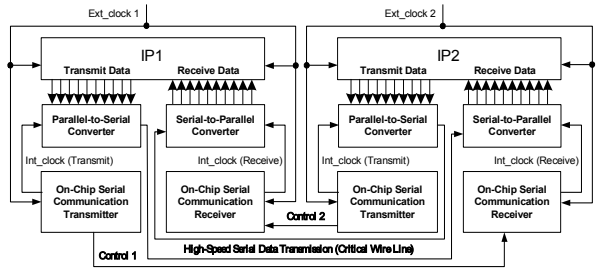
(b) On-Chip High-Speed Serial Communication

Fig. 1: Comparisons of wire complexity between the parallel-shared bus and the proposed on-chip high-speed serial communication architecture

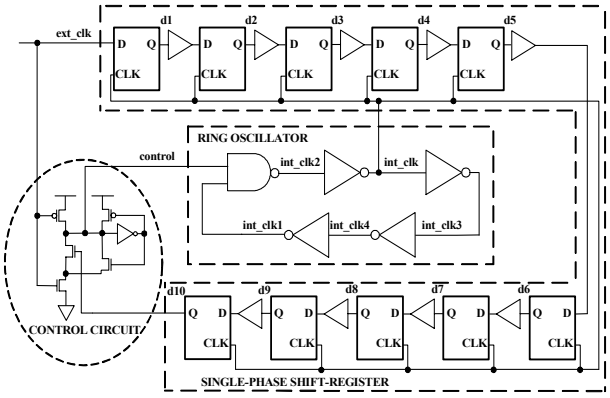
A. The Proposed Transmitter Design

The transmitter, as illustrated in Fig. 2(b), is composed of the ring oscillator, the shift register, and the control circuit. The ring oscillator is used to generate the high-speed clock (int_clk) to synchronize the serial transmission data. In our design, the ring oscillator can oscillate above 2 GHz to provide high transmission bandwidth. In [6], the speed bottleneck in the transmitter is limited by the control circuit and the counter because of critical synchronization timing constraints. Therefore, we propose the shift register based transmitter to overcome the speed bottleneck.

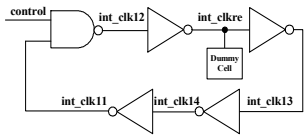
In the transmitter, the number of serial transmission bits is determined by the stage of shift register. In the shift



(a) Proposed High-Speed On-Chip Serial Communication Architecture



(b) On-Chip Serial Communication Transmitter



(c) On-Chip Serial Communication Receiver

Fig. 2: The proposed high-speed, reliable on-chip serial communication design.

register, each single bit is constructed by the Pulse-Triggered True-single-phase- clocking D Flip-Flop (PTTFF) [7] with delay buffer. The PTTFF is adopted as fast register with shorter set-up time. In this paper, the shift register is designed to be single-phase, which is realized by connecting the external-clock (ext_clk) as the shift register input. The single-phase design can provide wider synchronization timing constraint tolerance to meet the high-speed demand. Moreover, the single phase can make the shift register to be scalable.

The control circuit is used to synchronize the int_clk between transmitter and receiver. The oscillator starts with the positive edge of ext_clk and stops with a fixed number of shift register latency. In the proposed dynamic control circuit, the control signal can be fast precharged to "high" to trigger the int_clk. As the final stage shift register output (d10) changes from logic "0" to logic "1", the control signal will be fast pulled down to stop the int_clk.

B. The proposed Receiver Design

The receiver is constructed by the ring oscillator with nearly the same frequency as int_clk, as illustrated in Fig. 2(c). To get the same oscillation frequency in the receiver (int_clkre), the dummy cell is inserted to int_clkre with the same size as the loading in int_clk.

III. HIGH-SPEED SCALABLE DESIGN AND TIMING ANALYSIS

To meet the speed constraint and wide-bandwidth demand in SoC, we propose the single-phase pulse-triggered TSPC shift-register design in the on-chip serial communication transmitter to replace the counter-based transmitter in [6]. The proposed single-phase shift register timing constraint analysis is illustrated in Fig. 3. With single-phase advantage, the proposed design can provide larger synchronization timing constraint tolerance. Operating at about 2.5GHz, the proposed design can provide 0.151ns synchronization timing constraint tolerant range. Every single-bit shift register can be viewed as the same and we only need to consider the case of read logic "1" in the D flip-flop. Therefore, it can be easily scalable to any transmission bit number meet the future SoC demand.

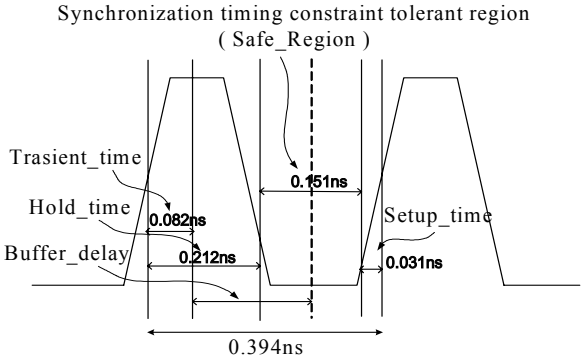


Fig. 3: The timing constraint analysis of the proposed single-phase shift register

In the asynchronous counter (ripple counter), as illustrated in Fig 4(a), the delay time is proportional to the bit number, because each present counter state input is triggered by the previous state output. As a result, the speed will be slow, especially as the bit number increases. In the synchronous counter, as illustrated in Fig. 4(b), every counter clock input is parallel triggered at the same time. However, the circuit complexity in the counter will be raised as the bit number increases. Also the delay time will be increased. In the proposed shift register based design, as illustrated in Fig. 4(c), the delay time is constant and independent from the serial transmission bit number. The speed comparison of counter-based design and proposed shift register based design is demonstrated in Fig. 5. In the 10-bit shift register, the speed can be improved about 80% as compared to 10-bit counter. Consequently, it is suitable for the wide-bandwidth SoC applications. Furthermore, it can be easily extended to any transmission number.

To generate a fast control signal, we propose a new dynamic control technology. The operation timing analysis of the proposed dynamic control technique is demonstrated in Fig. 6. In the precharge period, the int_clk is triggered by the positive edge of ext_clk (the negative edge of ext_clkbar). In the evaluation period, with the single-phase property, the

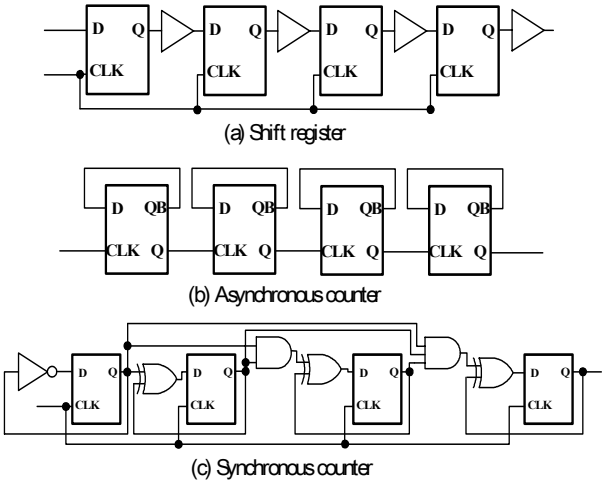


Fig. 4: Comparisons of the shift-register circuit and the counter circuit

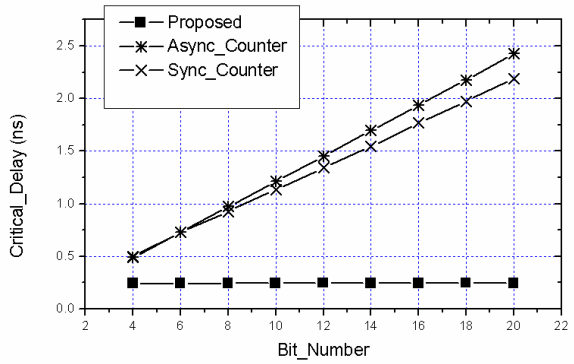


Fig. 5: The speed comparison of counter-based design and proposed shift register based design

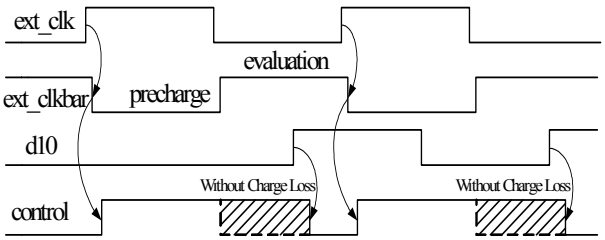


Fig. 6: The operation timing analysis of the proposed dynamic control technique

shift register outputs always change from logic ”0” to logic “1”. Therefore, there will be no charge loss through the pull-down network even though the signal switches in the evaluation period of dynamic control circuit. Consequently, the final stage shift register output can be directly connected to the dynamic pull-down nMOS. Besides, in the output of control circuit, we add 4 transistors to construct the feedback latch to boost gain and avoid floating situation. The control signal can be fast pulled down to stop the int_clk because only one nMOS serial connected with the evaluated nMOS in the pull-down network and the precharged pMOS has been turned-off.

IV. PERFORMANCE COMPARISONS AND SIMULATION RESULTS

The detailed performance comparison of various on-chip serial communication designs is illustrated in Table 1 and the speed timing comparison is illustrated in Fig. 7. All the comparison results are based on the post-layout simulation got from HSPICE.

In the on-chip serial communication with parallel-to-serial ratio of 10, the 90% interconnection wires between IPs can be reduced. In the proposed on-chip serial communication design, the critical delay time can be reduced to 4.25ns with about 65% improvement and can provide about 3 times bandwidth. The delay in the proposed single-phase shift register based on-chip serial transmitter can be reduced to 0.243ns with about 80%improvement in speed as compared to the counter based transmitter in [6]. By using the proposed dynamic control technique, the speed can be accelerated about 20%. Moreover, the proposed on-chip serial communication design possesses good scalability, wide timing constraint toleranc. In Fig7, we can find that the proposed design can operate fastest because of fast serial data transmitted by the proposed single-phase shift-register based transmitter.

Table 1: Performance comparisons of various on-chip serial communication designs

	This Work	Async[6]	Sync[6]
Tr. Count	384	394	562
Wire Reduction	90%	90%	90%
P/S Ratio	10	10	10
Tcritical (ns)	4.25	13.18	12.12
Improvement		67.75%	64.93%
Int_Clk Frequency	2.54GHz	0.73GHz	0.80GHz
Bandwidth	2Gb/s	0.645Gb/s	0.690Gb/s
Improvement		3.10X	2.90X
T_transmitter	0.243	1.213	1.134
Improvement		79.97%	78.57%
T_control	0.166	0.214	0.214
Improvement		22.43%	22.43%
Energy (uw/MHz)	1.65	1.63	1.81
Scalability	Good	Worse	Worse
Timing tolerance	Wide	Narrow	Narrow

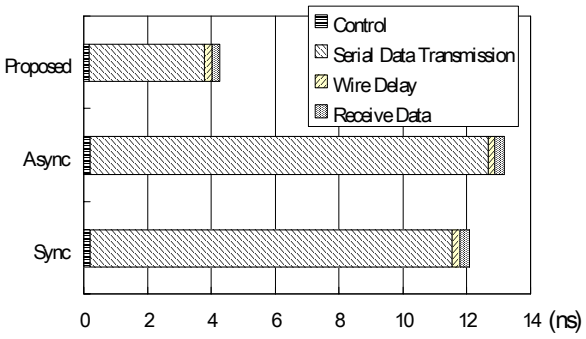


Fig. 7: The speed timing comparison of various on-chip serial communication designs

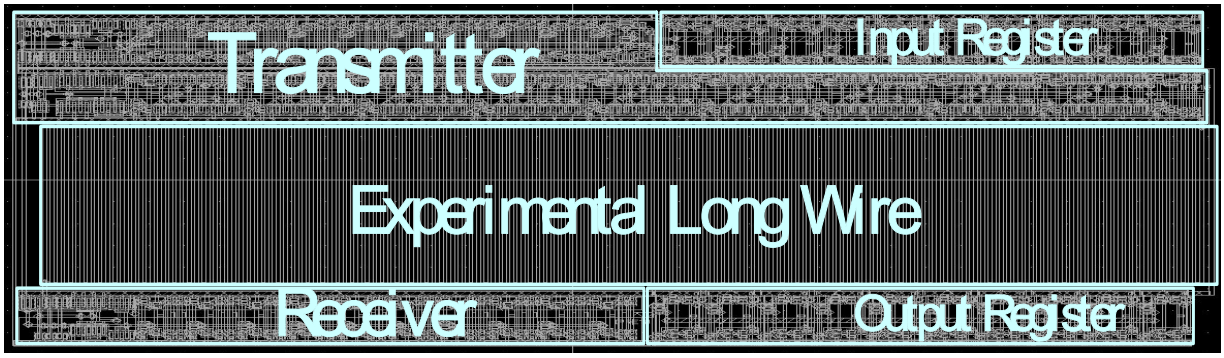


Fig. 8: The layout of proposed high-speed, scalable on-chip serial communication design

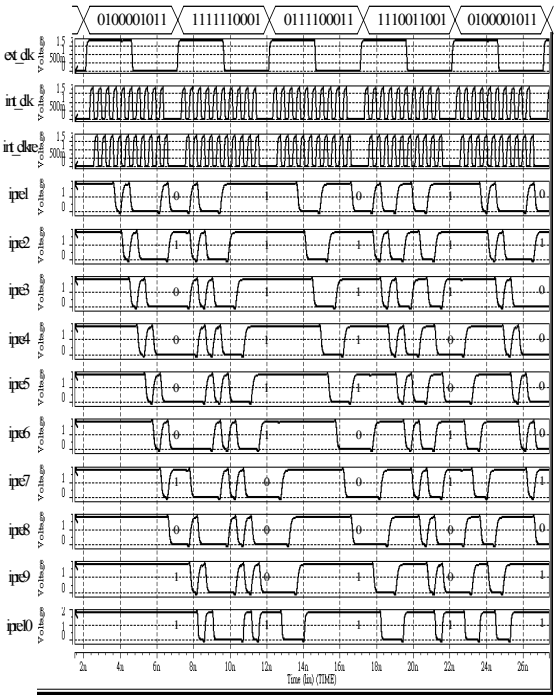


Fig. 9: Waveform of the proposed high-speed, scalable on-chip serial communication design

Table 2: Performance Summary

Process	**UMC 0.18um**
Supply Voltage	**1.8V**
Transistor count	**384**
Transmission Bandwidth	**2Gb/s**
Int_clock Frequency	**2.54GHz**
Ext_clock Frequency	**200MHz**
Implementation Area	**180um* 40um**
Experiment Wire Length	**6mm**

To verify the function and performance in silicon, we layout the proposed design in UMC 0.18um process, as illustrated in Fig. 8. A 6mm experimental long wire is drawn to simulate the SoC communication environment. The function is verified to be correct in 2Gb/s transmission rate as demonstrated in Fig. 9. Finally, Table2 shows the performance summary of the proposed high-speed, scalable on-chip serial communication design. In the proposed design, the total transistor number is 384. In the UMC 0.18um process, the proposed design can support 2Gb/s transmission bandwidth with 2.54GHz int_clk and 200MHz ext_clk. The total implementation area is 180um*40um, excluding experimental wire area.

V. CONCLUSIONS

In this paper, a high-speed, scalable on-chip serial communication interface design is proposed in UMC 0.18um process. The serial communication clock frequency is designed to work correctly at 2.54GHz to provide 2Gb/s transmission bandwidth for SoC applications. By using the dynamic control technology, we can generate a fast and reliable control signal with about 20% improvement in speed. By using the single-phase pulse-triggered TSPC shift register design, the speed can be accelerated about 65% to provide about 3 times serial transmission bandwidth. Moreover, the proposed design can be easily scalable.

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