Microwatt MOSLED Using SiO_X With Buried Si Nanocrystals on Si Nano-Pillar Array

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***Abstract*—Microwatt light emission from a metal–oxide–semiconductor light-emitting diode (MOSLED) made by using SiO_x film with buried Si nanocrystals on Si nano-pillar array is demonstrated. The Si nano-pillar array obtained by drying the rapidly self-aggregated Ni nano-dot-masked Si substrate exhibit size, aspect ratio, and density of 30 nm, 10, and 2.8×10^{10} cm^{-2}, respectively. These high-aspect-ratio Si nano-pillar array helps to enhance the Fowler–Nordheim tunneling-based carrier injection and to facilitate the complete relaxation on total internal reflection, thus increasing the quantum efficiency by one order of magnitude and improving the light extraction from the nano-roughened device surface by three times at least. The light-emission intensity, turn-on current and power-current slope of the MOSLED are 0.2 mW/cm^2, 20-30 μA, and 3$\pm$0.5 mW/A, respectively. At a biased current of 400 μA, the highest external quantum efficiency is over 0.2% to obtain the maximum EL power of >1 μW. Compared with the same device made on smooth Si substrate under a power conversion ratio of 1×10^{-4}, such an output power performance is enhanced by at least one order of magnitude.**

***Index Terms*—Metal–oxide–semiconductor light-emitting diode (MOSLED), plasma-enhanced chemical vapor deposition (PECVD), Si nano-pillar array.**

I. Introduction

PLASMA-enhanced chemical vapor deposition (PECVD)-grown Si-rich SiO_2 or SiO_x with embedded Si nanocrystals (referred hereafter as SiO_x:nc-Si) of extremely high density have been extensively investigated as a new class of light-emitting material over decades [1]–[3]. The SiO_x : nc-Si-based metal–oxide–semiconductor light-emitting diode (MOSLED) is indeed a potential candidate for next-generation optoelectronic applications such as optical interconnect, optical communication, and microdisplay panels. The advantages of SiO_x : nc-Si-based MOSLEDs include wavelength-tunable and full-color emission, processing compatibility with other MOS devices, system feasibility, and low cost of fabrication. Electroluminescence (EL) from the SiO_x : nc-Si film grown by the anomalous PECVD recipe has previously been observed [4]–[8]; however, the EL intensity and external quantum efficiency is extremely low due to the nature of indirect recombination, the insulating property of the host oxide, and the tunneling dependent carrier injection. Versatile methods were proposed to improve the efficiency of carrier injection into nc-Si, which include the increasing on density of the nc-Si embedded in SiO_x film, the decreasing thickness of the nc-Si layer, and the bandgap engineering of the contact metal. However, an efficient approach to improve the carrier injection into the nc-Si embedded in the SiO_x film via the Si nano-roughened surface-based electrode has never been reported. Recently, the fabrication of the Si nano-pillar array based on the electron-beam (E-beam) lithography and inductively couple-plasma reactive ion etching (ICP-RIE) process were introduced [9]–[12]. The Si nano-pillar array with its rod size of <10-nm can be reproduced under the control of E-beam lithography [12]. In addition, the self-assembled metallic nano-dots have also emerged to function as nano-sensor for either bio-photonics or etching-mask for nano-electronics. Ni has been considered as an alternative to the other noble metals (Au or Ag) for dry-etching the high-aspect-ratio Si nano-pillars on Si substrate [12]–[15]. It is thus worthy discussing the external quantum efficiency for light emission from a SiO_x:nc-Si-based MOSLED made on such a high-aspect-ratio Si nano-pillar array on Si. In principle, there is an inherent limitation on the quantum efficiency since the light extraction efficiency of most conventional LEDs is limited by the total internal reflection (TIR) of the emitting light from the active region of the LED, which always occurs due to the large difference in the refractive index at the interface between LED top-surface and air. [16] In this letter, we demonstrate a novel SiO_x:nc-Si MOSLED made on the dense Si nano-pillar array to enhance both the carrier injection and light extraction efficiencies, in which the Si nano-pillars is fabricated by reactive-ion etching an oxide-covered Si substrate encapsulated with the self-assembled Ni nano-dot mask. Anomalous photoluminescence (PL) spectra of Si nano-pillars at visible and near-infrared spectral regions are also investigated. Such a Si nano-pillar array is proposed to enable a microwatt power emitting from the SiO_x:nc-Si-based MOSLED. The broadband electroluminescent (EL) spectrum and improved turn-on characteristics of such a novel MOSLED, with its external quantum efficiency increasing by enhanced carrier injection and light-extracting mechanisms, are reported.

Manuscript received Septeber 30, 2007; revised Febuary 26, 2008. This work was supported in part by the National Science Council of Taiwan, R.O.C., and U.S. Air-Force AOARD Office under Grants NSC96–2215-E-002–099 and FA 4869-07-1-4081.

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Digital Object Identifier 10.1109/JLT.2008.922177

II. Sample Preparation

To fabricate a SiO_x-based MOSLED on Si nano-pillar array, the Si nano-pillar roughened Si substrate surface is obtained by rapid thermal annealing a 5-nm-thick Ni film evaporated on a 20-nm-thick SiO_2 layer covered Si substrate to induce self-aggregation of a two-dimensional randomized Ni nano-dots mask [17]. Subsequently, a large-area Si nano-pillar array with rod

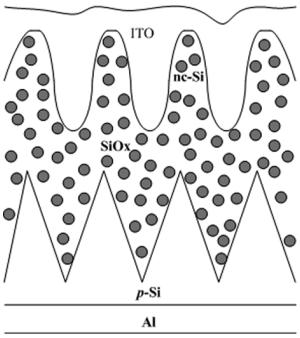

Fig. 1. Device structure of a silicon nanocrystal-based MOSLED on silicon nanopillar array.

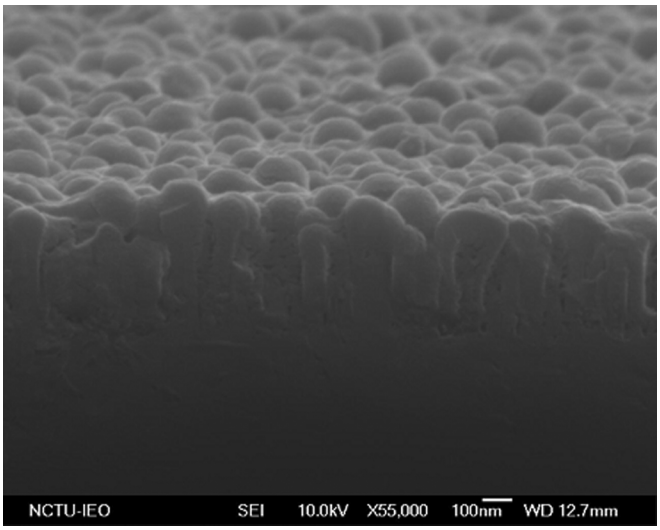

Fig. 2. SEM cross-sectional photograph of the SiO_x on Si nano-pillar array.

diameter of 30 nm and height of 350 nm can be formatted on Si substrate through the ICP-RIE procedure with such a self-assembled Ni/SiO_2 nano-dots-based nano-mask [18]. Afterwards, the Si-rich SiO_x film was deposited on p-type (100)-oriented Si substrate with a Si nano-pillar roughened surface using PECVD with a recipe of SiH_4/N_2O fluence ratio of 1/5, chamber pressure at 60 mtorr, and plasma power of 30 W and substrate temperature of 400 °C [19], [20]. After deposition, the Si-rich SiO_x film with thickness of 240 nm was postannealed in a quartz furnace with flowing N_2 at 1100 °C for 60 min to precipitate nc-Si. The size and density estimated from high-resolution transmission electron microscopy (TEM) are 4 ± 0.5 nm and 2×10^{18} cm^{-3}. The device structure of an $ITO/SiO_x/Si/Al$ MOSLED with buried Si nanocrystals made on a silicon nano-pillar array is illustrated in Fig. 1. The MOSLED with a circular contact diameter of 0.8 mm is top bonding by a Cu wire and thermal-electric controlled at the bottom side for EL analysis. To confirm the surface roughening effect, the cross-sectional photograph of the Si-rich SiO_x deposited Si nano-pillar surface obtained from secondary electron microscopy (SEM) is shown in Fig. 2.

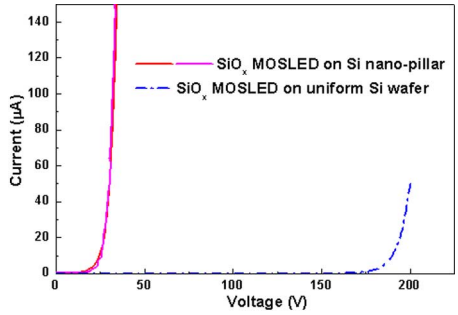

Fig. 3. Current-voltage response of the SiO_x-based MOSLED made on a Si nano-pillar array (red circles) and uniform Si substrate (blue squares).

III. Results and Discussions

A. Enhancement on Carrier Transport of the SiO_x-Based MOSLED

In Fig. 3, the measured current-voltage response of the $ITO/SiO_x:nc\text{-}Si/p\text{-}Si/Al$ MOSLED made on Si nano-pillars reveals a significant improvement on its turn-on characteristic as compared to that of the same device made on a uniform p-type Si wafer. In general, four possible carrier transport mechanisms can be involved in the MOSLED made by SiO_x with embedded Si nanocrystals, which include direct tunneling, Fowler–Nordheim (F–N) tunneling, thermionic emission, and Poole–Frenkel (P–F) tunneling. The direct tunneling of carriers usually occurs when the applied voltage on the MOSLED structure is relatively smaller than the barrier height of the metal–SiO_x interface, in which electrons can only tunnel through the whole SiO_x film with a thickness of thinner than 5 nm. In contrast, when the applied voltage is equivalent to or larger than the barrier height of the metal-oxide interface, the electrons from the metal side experience a triangular barrier when tunneling into the SiO_x. Such a case is referred to as the F–N tunneling effect. Theoretically, the current density of the direct and F–N tunneling mechanisms ($J_{\rm dir}$ and $J_{\rm F-N}$) are expressed by [21]–[23]

$$J_{\rm dir} = \frac{AE_{ox}^2}{\left[1-\sqrt{\frac{1-qV_{ox}}{\Phi_B}}\right]^2}\exp\left(\frac{-B\left[1-\left(\frac{1-qV_{ox}}{\Phi_B}\right)^{1.5}\right]}{E_{ox}}\right) \tag{1}$$

$$J_{\rm F-N} = \frac{q^3\left(\frac{m}{m_{ox}}\right)}{8\pi h\Phi_B}E_{ox}^2\exp\left(\frac{-8\pi\sqrt{2m_{ox}\Phi_B^3}}{3qhE_{ox}}\right) \tag{2}$$

$$A = \frac{q^3\left(\frac{m}{m_{ox}}\right)}{8\pi h\Phi_B} = 1.54\times10^{-6}\frac{\left(\frac{m}{m_{ox}}\right)}{\Phi_B}\left[\frac{A}{V^2}\right] \tag{3}$$

$$B = \frac{8\pi\sqrt{2m_{ox}\Phi_B^3}}{3qh} = 6.83\times10^7\sqrt{\left(\frac{m_{ox}}{m}\right)\Phi_B^3}\left[\frac{V}{cm}\right] \tag{4}$$

where q is the electron charge, h is Planck's constant, E_{ox} is the applied electric field on the SiO_x, m_{ox} is the effective electron mass in the SiO_x, m is the free electron mass, Φ_B is the barrier height at the metal-oxide interface, and V_{ox} is the biased

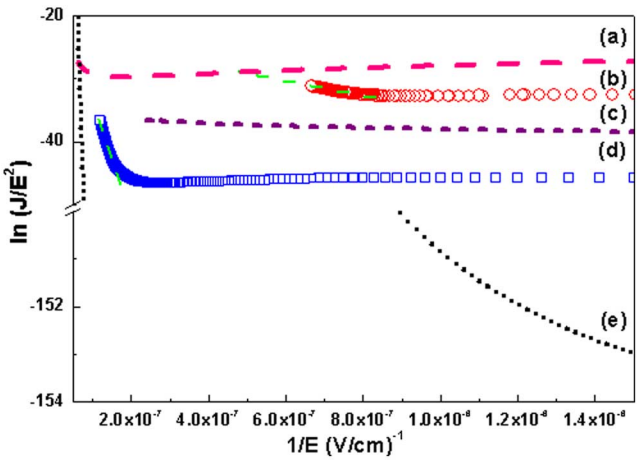

Fig. 4. The MOSLED current contributed by versatile carrier tunneling mechanisms. (a) Direct tunneling current. (b) F–N tunneling current of SiO_x MOSLED on Si nano-pillar. (c) P–F tunneling current. (d) F–N tunneling current of SiO_x MOSLED on uniform Si substrate. (e) Thermionic emission current. The green dashed line illustrate the fitting curve from the theoretical F–N tunneling model.

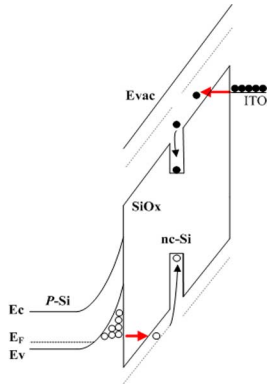

Fig. 5. Band diagram of MOSLED on Si substrate under positively biased condition.

voltage across the MOSLED. To realize if F–N tunneling is the dominated mechanism for the carrier transport behavior in the ITO/SiO_x:nc-Si/p-Si/Al MOSLED, the electric field (E) dependent emission current density (J) is also plotted and shown in Fig. 4. A linear $\ln(J/E^2)$ versus $1/E$ relationship is observed and the experimental data of the MOSLED can be well fitted by F–N tunneling model as compared to other mechanisms. For example, a simulated direct tunneling current with a m_{ox}/m ratio of 0.26, barrier height of 3.8, and oxide thickness of 2.3 nm is also shown in Fig. 4, which is much larger than the actual currents flowing through the ITO/SiO_x:nc-Si/p-Si/Al MOSLED. In our case, the direct tunneling current is negligible since the SiO_x thickness is much thicker.

On the other hand, the current density through a metal-semiconductor contact dominated by thermionic emission is also discussed if we consider the Si nanocrystals within in the SiO_x as a possible carrier transport path [24], which is give by

$$J_{\text{thermionic}} = A^* T^2 \exp\left(\frac{-q\Phi_B}{kT}\right)\left(\exp\left(\frac{qV}{kT}\right)-1\right) \quad (5)$$

where $A^* = 4\ \text{pqk}^2 m^*/h^3 = 120(m_{ox}/m)$, $\text{A/cm}^2\text{K}^2$ is Richardson's constant, m is free electron mass, m_{ox} is the effective electron mass in SiO_x film, and T is the absolute temperature. By setting $m^*/m = 0.26$, $T = 300\,\text{K}$, and $\Phi_B = 3.8\,\text{eV}$, a simulated thermionic current is shown in Fig. 4, which is much larger than the measured current of the ITO/SiO_x:nc-Si/p-Si/Al MOSLED. Therefore, it is impossible to observe thermionic current in the ITO/SiO_x : nc-Si/p-Si/Al MOSLED. Furthermore, the Si nanocrystals could also be treated as the defects to contribute another carrier transport so-called P–F tunneling, which can be evaluated by using the following expression [25], [26]:

$$J_{\text{PF}}(E_{ox},T) = qN_t E_{ox}\mu \exp\left(-\frac{q\Phi_{\text{PF}}}{kT}\right)\exp\left(\frac{1}{kT}\sqrt{\frac{qE_{ox}}{(4)\pi\varepsilon_{ox}}}\right) \quad (6)$$

where N_t is the volume density of occupied traps, μ is the carrier mobility, Φ_{PF} is the barrier height for hopping carriers, and ε_{ox} is the permittivity of the SiO_x film. The P–F tunneling and Schottky emission are not differentiated from each other by their electric field and temperature dependence, except that a factor 4 presented in the bracket of the field-dependent term of (6) is assumed to be negligible for thick oxide film (> 10 nm) in the Schottky emission case. In our case, the possible P–F tunneling current is also simulated by using parameters of the ITO/SiO_x : nc-Si/p-Si/Al MOSLEDs such as the electron charge q of 1.6022×10^{-19} C, estimated volume density (N_t) of 10^{18} cm^{-3}, carrier mobility μ of 20 $\text{cm}^2/\text{V s}$ at 300 K, thermal energy kT of 0.02586 eV at 300 K, barrier height Φ_{PF} of 1.37 eV, and permittivity of SiO_x film ϵ_{ox} of 3.24 ($\epsilon_{ox} = n^2 = 1.8^2$, where n is refractive index of the SiO_x film), which has therefore been addressed as a less pronounced mechanism as compared to the F–N tunneling effect.

From these theoretical analyses, it is confirmed that the light emission from the SiO_x-based MOSLED is indeed based on the electron-hole recombination in the Si nanocrystals, in which the electrons and holes are tunneling through ITO–SiO_x and Si–SiO_x barriers, respectively [27]–[30]. Originally, the F–N tunneling effect also occurs in the MOSLED sample made on a smooth Si wafer without Si nano-pillars, however, which suffers from insufficient large tunneling carriers tunneled through the oxide structure and injected into the Si nanocrystals. The corresponding band diagram of the MOSLED for explaining the Si-nanopillar enhanced F–N tunneling effect is shown in Fig. 5, which indicates either the reduced size of Si nanocrystals or decreased barrier height at SiO_x-Si and metal-SiO_x interfaces can provide such MOSLED an exceptionally high EL output. This has also been concluded from our experimental result and the fitting of F–N tunneling process. In particular, the effective barrier height for carriers at the junction interfaces of the MOSLED can be further greatly reduced due to both the synthesis of Si nanocrystals and the formation of Si nano-pillars, as shown in Fig. 5. Similar reports were addressed by Prakash and coworkers [31]. The existence of Si nano-pillars facilitate the growth of Si-rich SiO_2 with well size-controlled Si nanocrystals in between, in which the effective barrier height at the Si–SiO_2 interface reduces to cause the shrinkage of the tunneling distance of the oxide triangular barrier between metal/p-Si and Si nanocrystals. Therefore, both the densities of electrons and holes injected

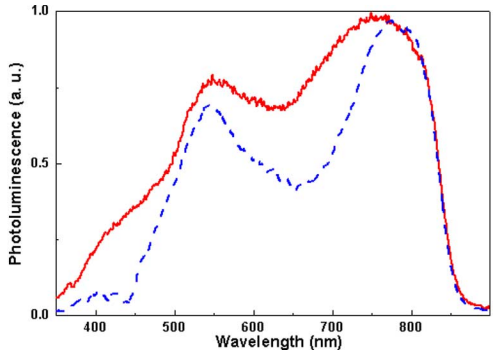

Fig. 6. EL (solid line) and PL (dashed line) spectra of SiO_x-based MOSLED.

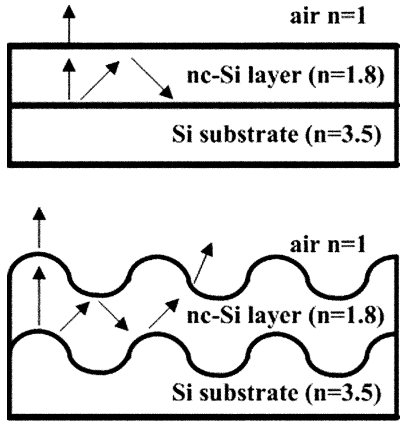

Fig. 7. Schematic illustration of light-emitting paths from the SiO_x-based MOSLEDs made on uniform Si substrate (upper) and Si nano-pillar array (lower).

into the Si nanocrystals can be significantly increased due to such a hybrid Si nano-pillar array and Si-rich SiO_x structure. As a result, the carrier recombination process is greatly enhanced due to the increasing carriers injected into the Si nanocrystals, which essentially gives rise to an improved EL performance and an enlarged light-emitting power.

B. Enhancement on Light Extraction of SiO_x-Based MOSLED

Under a bias of 100 mA, the EL spectrum of the MOSLED is compared with its PL spectrum and shown in Fig. 6. The EL and PL is alike each other except the enhanced part on the short-wavelength region contributed by the small-size Si nanocrystals. Such a difference is attributed to the higher carrier tunneling probability of carriers to the Si nanocrystals with smaller sizes. In addition, it may partially arise from the consecutive hot-carrier injection from one Si nanocrystal to another, leading to a higher probability of recombination at the higher quantized states of the Si nanocrystals. In principle, there are two principal approaches for improving the LED efficiency: the first is increasing the internal quantum efficiency, which is determined by crystal quality and epitaxial layer structure, and the second is increasing light extraction efficiency. Roughening the top surface of an LED is one of the methods for improving the light extraction. The roughened top surface reduces internal light reflection and scatters the light outward. In our case, the light-extraction efficiency of the SiO_x-based MOSLED with buried Si nanocrystals is limited mainly due to the large difference in the refractive index between the nc-Si film and surrounding air. The critical angle determined by Snell's law, that is, the angle that the photons can escape from the nc-Si layer to air, is crucially important to improve the light-extraction efficiency of the nc-Si-based MOSLED. The key to enhancing the escape probability of light is to give the photons generated in the active layer of the nc-Si-based MOSLED structure multiple opportunities to find the escape cone. Our device structure shown in Fig. 1 exactly meets the demand on angular randomization or scrambling of the photons, which is the concept of our design by using the Si nano-pillar array to achieve such a purpose. Fig. 7(a) shows the possible photon paths at the interface between the nc-Si layer and surrounding air for nc-Si-based MOSLEDs without surface roughening. For a nc-Si-based MOSLED with a nc-Si top surface which was roughened, the angular randomization of photons can be achieved by surface scattering from the roughened top surface of the MOSLED, as shown in Fig. 7(b). Thus, the

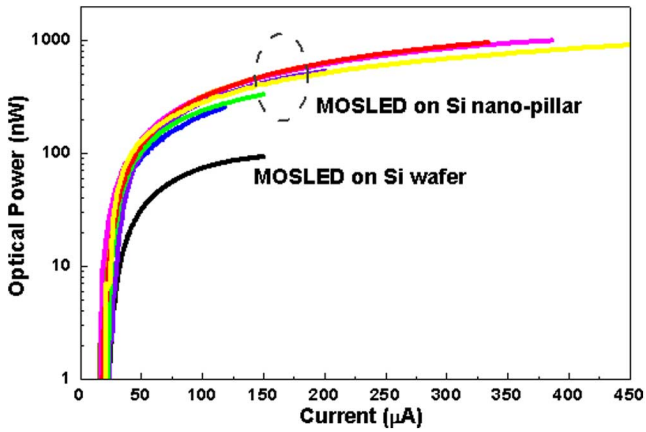

Fig. 8. Optical output power as a function of biased current for the SiO_x-based MOSLEDs made on Si nano-pillar array and uniform Si substrate.

roughened surface structure can improve the probability of escaping the photons outside from the nc-Si-based MOSLED, resulting in an increase in the light-out power of the MOSLED, as shown in Fig. 8. However, there are still different P-I characteristics among samples even though the Si nano-pillar arrays are fabricated on same wafer at once. The maximum output power of the SiO_x-based MOSLED made on the Si nano-pillar can be increased by almost one order of magnitude higher than that of the same device made on a uniform Si wafer. The maximum optical output power, biased current, biased voltage, and external quantum efficiency are 1 μW at biased current and voltage of 0.4 μA and 36 V, respectively. The peak wavelength and electrical to optical power conversion ratio of the SiO_x-based MOSLED with Si nano-pillars are 0.76 μm and about 1×10^{-4}, respectively.

For nc-Si-based MOSLEDs, the refractive indexes of nc-Si ($n_{\mathrm{nc-Si}}$) and air (n_{air}) are 1.8 and 1, respectively. In this case, the critical angle ($\theta_c = \sin -1 n_{\mathrm{air}}/n_{\mathrm{nc-Si}}$) for the light generated in the active region to escape is about 33.7°. Assuming the light emission from the active region of an nc-Si-based MOSLED is isotropic, and the light can escape from the chip if the angle of incidence to the chip wall is less than the critical angle, a small fraction of light generated in the active region of

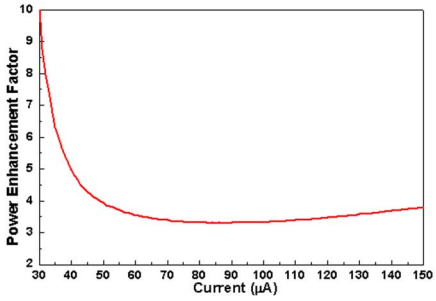

Fig. 9. Power enhance factor of the SiO_x-based MOSLED made on Si nano-pillar at different biased currents.

the nc-Si-based MOSLED can escape to the surrounding air. In our MOSLED device, the output power is uniformly distributed over the whole half-spherical surface with a full solid angle of $\Omega_{\text{half}} = 2\pi$, and the emitting solid angle of the MOSLED limited by the total internal reflection (Ω_{TIR}) is 0.34π. Assuming the maximum power can be emitted is P, the output power can be emitted from the MOSLED without the limitation of the total internal reflection is $P \times (\Omega_{\text{TIR}}/\Omega_{\text{half}}) = 0.17P$. Only a small fraction of light (about 17%) can escape from the nc-Si-based MOSLED even though the refractive index of the top ITO contact layer is nearly the same with the Si-rich SiO_x film to prevent additional reflection. Therefore, for a conventional nc-Si-based LED, the external quantum efficiency limits to a few percent due to the high refractive index of nc-Si as well as the absorption in the metal pad for current injection and free carriers, even if the internal quantum efficiency close to 100% is reached. The improvement on light-extraction efficiency of the nc-Si-based MOSLED relies on the angular randomization or scrambling of the photons via surface roughening effect. The comparison on the nc-Si-based MOSLED made on Si nano-pillar array and smooth Si substrates under the same biased current of 150 μA clearly shows an increase on output EL power by a 3.8 times, as shown in Fig. 9.

The power enhancing factor of our devices is better than those ever reported on the other LED devices based on compound semiconductor material. Previously, the surface roughening induced EL power enhancement on GaN- or InGaN-based LEDs has been reported [32]–[34]. In particular, Fujii *et al.* [16] have reported the output power of a GaN-based LED made on optimally roughened surface, which shows a two- or three-fold enhancement as compared to that of a GaN-based LED made on the substrate without surface roughening. Huang [15] also demonstrated the emitting power and wall-plug efficiency of a InGaN-GaN LED with a nano-roughened top p-GaN surface can be improved by 1.4 times and 45% higher than that of a conventional LED with top-surface roughening process. In comparison, our experiments conclude that the Si nano-pillar array improves not only the carrier tunneling but also the light extraction in the nc-Si MOSLED. Obviously, the nano-roughening top surface of the SiO_x MOSLED is also one of the efficient methods for increasing the light extraction rate to improve the external quantum efficiency of the LED. If we define the external quantum efficiency as the ratio of the output photo number and input electron number described by the equation below

$$\eta = \frac{\int_{t_0}^{t_1} P_{\text{opt}} \times t dt}{\frac{\frac{1.24}{\lambda} \times 1.6 \times 10^{-19}}{\int_{t_0}^{t_1} I \times t dt}} = \frac{P_{\text{opt}}}{I \times \left(\frac{1.24}{\lambda}\right)} \tag{7}$$

where P_{opt} is optical output power, t is experimental duration, λ is wavelength, and I is biased current. The highest external quantum efficiency obtained from our SiO_x-based MOSLED on Si nano-pillars is up to 2×10^{-3}, which is mainly attributed to the enhanced carrier transport through the nano-tip structure. Note that internal quantum efficiency contributed by the buried Si nanocrystals within the SiO_x-based MOSLED made on Si nano-pillars could be much larger than the external quantum efficiency. The PECVD growth of SiO_x on the Si nano-pillar array can also help to confine the size and thus promote the density of Si nanocrystals among the Si nano-pillars. Further improvement on the light-emitting power and external quantum efficiency relies on the optimization of both the height and aspect ratio of Si nano-pillars, which helps to enhance the F–N tunneling-based carrier injection and to facilitate the complete relaxation on the total internal reflection at the MOSLED top surface.

IV. Conclusion

In conclusion, we have demonstrated the MOSLED made by SiO_x with buried Si nanocrystals on Si nano-pillar array to enable microwatt light-emitting power. The Si nano-pillar array on Si substrate is fabricated by using the rapidly self-aggregated Ni nano-dots on Si substrate covered with a thin SiO_2 buffered layer as an etching mask, while the Ni nano-dots can be formatted after rapid thermal annealing at 850 °C for 22 s with size and density of 30 nm and 2.8×10^{10} cm^{-2}, respectively. The Si nano-pillar array with aspect ratio as high as 10 can be obtained after dry-etching the Ni nano-dot masked Si substrate surface. The EL performance of the SiO_x-based MOSLED with buried Si nanocrystals made on such high-aspect-ratio Si nano-pillars is greatly enhanced. The emitting optical intensity, turn-on current and power-current slope of the MOSLED are 0.2 mW/cm^2, 20-30 μA, and 3 ± 0.5 mW/A, respectively. The highest external quantum efficiency is exceeding 0.2% to provide maximum EL power of > 1 μW at biased current of 400 μA, and the EL power is already improved by one order of magnitude as those obtained from similar devices made on the smooth Si wafer under a power conversion ratio of 1×10^{-4}. The reduction of turn-on threshold voltage and the enhancement on Fowler–Nordheim tunneling performances of the nc-Si-based MOSLED made on Si nano-pillar array essentially raise the possibility of its EL power toward 10 s-μW regime.

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