行政院國家科學委員會補助專題研究計畫成果報告

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※ 微機電微波元件之研究子計畫(1)- ※

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※ 三五族微機電技術研發及應用 ※

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計畫類別： ■整合型計畫

計畫編號： NSC 89-2218-E-002-020

執行期間： 88 年 7 月 1 日至 89 年 6 月 30 日

計畫主持人：張培仁 教授

共同主持人：呂學士 教授 ； 黃榮堂教授

本成果報告包括以下應繳交之附件：

■出席國際學術會議心得報告及發表之論文各一份

■本計劃研究成果之專利說明書一份

執行單位：國立台灣大學電機所

中 華 民 國 89年 9 月 28 日

行政院國家科學委員會專題研究計畫成果報告

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一、中文摘要

本計劃中，我們提出了一種名為【V 形谷空橋閘極】的新型閘極結構。這種閘極結構利用了砷化錠的非等向濕蝕刻特性，僅以單層光阻與常用的 1 微米接觸式光學微影技術，就可以製作出具有大閘極橫截面的次微米閘極。以對於 V 型谷蝕刻之通盤研究為基礎，我們設計了一為實現 V 型谷空橋閘極用的異質磊晶結構，並針對此磊晶結構發展出一最佳化製程方法。此製程方法相當簡單且可靠，並具有非常高的良率，這對量產是非常的重要的。

在試製此 V 型谷空橋閘極成功之後，我們將其實際應用於磷化銦鎵/砷化鎵/砷化銦鎵通道摻雜場效電晶體的製作上。同時，我們也以同樣的製程技術在同一異質磊晶結構上製作具傳平面型閘極的通道摻雜場效電晶體以作比較，具 V 型谷閘極的元作均有較佳的表現，包括了較大的轉導值（166 mS/mm），較大的通道電流（260mA/mm，當 Vgs=-0.5, Vds=5V），以及較高的電流截止頻率(13.86GHz)。

關鍵詞：V 形谷空橋閘極，磷化銦鎵，異質接面場效電晶體

Abstract

In this project, a gate structure named V-groove Airbridge Gate is firstly proposed. This novel gate, taking advantage of anisotropic V-Groove etching of undoped GaAs, can achieve submicrometer gate length and have large cross sectional area at the same time, employing only one layer of photoresist and common 1-um optical contact lithography. Based upon a thorough consideration of V-groove etching characteristics, an epitaxial heterostructure is designed, and a feasible processing procedure as well as optimum process conditions for fabricating the gate structure is also developed. This processing procedure is relatively simple and reliable, and is proved to have a very high production yield, which is important to industrial mass-production applications.

The V-groove air-bridge gate structure is applied to practical fabrication of In0.49Ga0.51P/GaAs/In0.2Ga0.8As DCFET's. As compared with traditional gate DCFET's fabricated with the same epi and the same lithographic technology, better DC and microwave performances are obtained by the V-gate devices. They exhibit a better current drivability, and leads to larger values of transconductance, channel current, and current-gain cut-ff frequency. These better performances imply the potential of being used as a high-speed power device.

Keywords: V-groove gate, InGaP, HEMT

2. Introduction

For field-effect transistors, short gate lengths are essential to high frequency device performance. Besides, the parasitic gate resistance has to be kept small simultaneously as the gate length shortened; otherwise the device would suffer from increased noise figure. There, proposed are ate structures exhibiting small gate length and large cross

section such as so-called mushroom gate or T-gate. However, there realization has to be attained by delicate multi-layer-resist rechnique and costly electron beam lithography, and the yield is not satifactory either.

3.1 Realization of V-Groove Gate

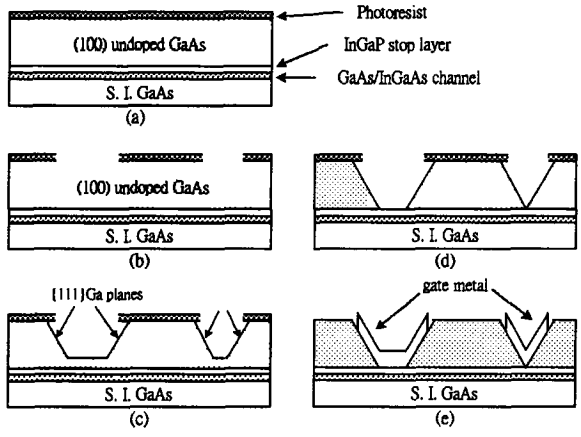


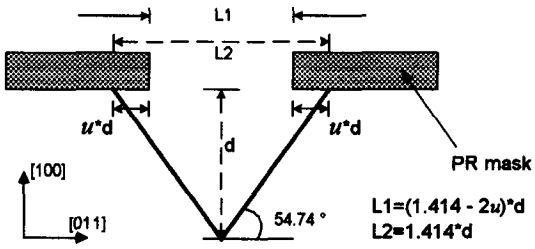
Fig. 1. V-groove gate formation.

Fabrication steps of submicron V-groove gates are illustrated in Fig. 1. Using gas source MBE, a thick layer of (100) undoped GaAs is grown on top of a InGaP etch-stop layer, which is in turn grown on top of conducting channels. The substrate is firstly spun on a film of photoresist (Fig. 1(a)). The resist is then patterned into finite openings by 1-μm contact printing lithography, as shown in Fig. 1(b). Anisotropic wet etching is subsequently conducted to form V-grooves through the openings (Fig. 1(c)). Due to etching selectivity between GaAs and InGaP, the etching process in vertical direction essentially stops automatically as soon as the InGaP layer is reached (Fig. 1(d)). Finally, the gate metal is evaporated and then defined by lift-off technique (Fig. 1(e)).

Theoretically, with a finite opening of mask material, one can obtain infinitely small feature at the tip of etched V-groove, just as illustrated by the gate in the right-hand side in Fig. 1(e). Even if the V-groove is not etched down to the tip; i.e. the wet etching only results in a U-groove with a flat bottom rather than a tip (see the gate in the left-hand side in Fig. 1(e)), the bottom is definitely of submicron size provided 1-μm technology is used to define on the opening. Fig. 2 shows the V-groove gate we fabricated on the (100) undoped GaAs layer. As can be seen clearly in this SEM picture, the effective gate length has been reduced to zero substantially.

In addition to the size of mask opening, equally important is the extent of undercut (side etching) of GaAs beneath the mask. This can be illustrated clearly in Fig. 3. Note that the angle θ between the V-groove slopes {111} and the surface of the substrate (100) is 54.74°. Let d be the depth of V-groove, then the top opening of the groove (L2) can be found as

$$L2 = 2 \times d \times \cot\theta = \sqrt{2}d \approx 1.414d \,. \qquad (1)$$



This is, however, not the opening of mask material (L1) if the undercut factor u is taken into account. The undercut factor u is defined as the ratio of undercut extent to etching depth d., i.e., the undercut extent is of magnitude $u*d$. Therefore, in order to attain the V-groove tip at a depth of d below the substrate surface, the mask opening L1 has to be

$$L1 = L2 - 2 \times u \times d = \left(\sqrt{2} - 2u\right) \times d \,. \qquad (2)$$

The larger value of u means that a narrower mask opening is needed to attain the V-groove tip at the same depth d. Since the minimum line width attainable is determined by the lithographic technology employed, the minimum mask opening is fixed for a certain lithographic technology. Therefore, the larger value of u implies that one has to etch deeper in order to attain the V-groove tip. This will affect the thickness of undoped GaAs layer we need in Fig. 1. If we want to realize V-groove gates with a thinner undoped GaAs layer (which is always desired), the undercut factor u has to be minimized by choosing an appropriate etching solution. In view of Eq.(2), if u exceeds $\sqrt{2}/2$ for some etchant, the tip of the V-groove can never be formed

with it. Therefore, the first consideration of V-groove gate design is the undercut factor, which should be as small as it can be.

It has been reported many times that H_2SO_4-based etchants have high etching selectivity between GaAs and the lattice-matched $In_{0.49}Ga_{0.51}P$, ranging from hundreds to thousands.[6, 7] For example, the ratio of etch rates of GaAs:InGaP can be as high as 4190:1 for H_2SO_4:H_2O_2:H_2O = 1:1:10 solution.[8] Therefore, we choose $In_{0.49}Ga_{0.51}P$ as the etch-stop layer. As for the first design consideration, it is reported that, among a series of H_2SO_4-based etchants, the H_2SO_4(98 w/o)-H_2O_2(30 w/o)-H_2O mixed in volume ratio of 4:1:5 has the smallest value of undercut factor u in [011] direction, which is 0.29.[5] We re-calibrated the u value for this etchant in a controlled etching environment of 20 °C, and found the u to be around 0.202. We also measured its etch rate to be about 1083 A/sec, or 6.5 m/min.

3.2 Device fabrication

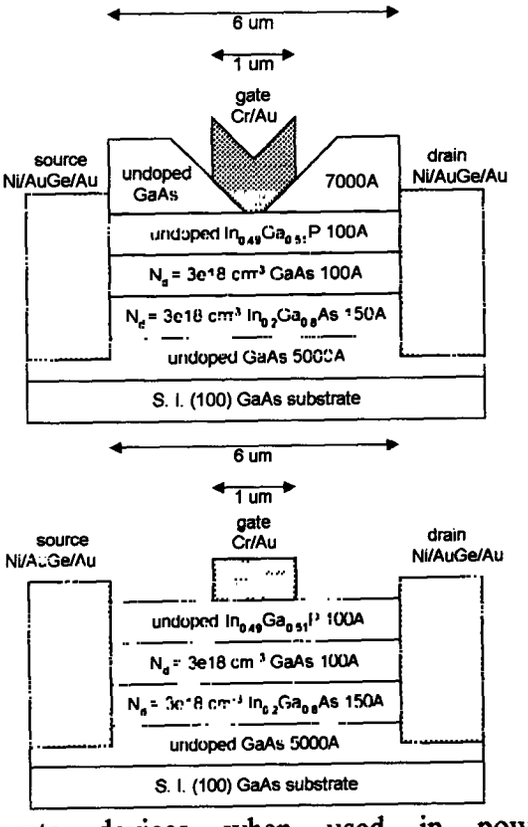
We fabricated V-groove gate DCFET's using micromachined V-groove technology on GSMBE grown substrate. For comparison, we also fabricated DCFET's with conventional strip gates using the same epitaxial layers, only taking away the uppermost i-GaAs layer in advance. Cross sectional views of both types of DCFET's are illustrated in Fig. 4.

Common wet etching process is employed to conduct the mesa etching down to undoped GaAs buffer layer. This is for the isolation between active areas of FET's. Pure HCl is used to etch the InGaP layer with an etching rate over 500 A/sec, and HF:H_2O_2:H_2O = 1:1:10 solution is used to etch both GaAs and InGaAs layers. The HF-based etchant can lead to mesas of outward slopes in both (011) and $(01\bar{1})$ cross sections. The slopes are so mild that they guarantee good step coverage of drain/source and gate metalization.

Subsequently, drain and source regions are defined, and the exposed InGaP in the drain/source regions is selectively etched away by HCl: H_3PO_4 = 1:3 solution. The ohmic metals of Ni/Au-Ge/Au are vacuum evaporated in sequence under the pressure of 2×10^{-6} torr, to a total thickness of 6000 Å. Contacts are formed by a lift-off process followed by rapid thermal annealing at about 400°C.

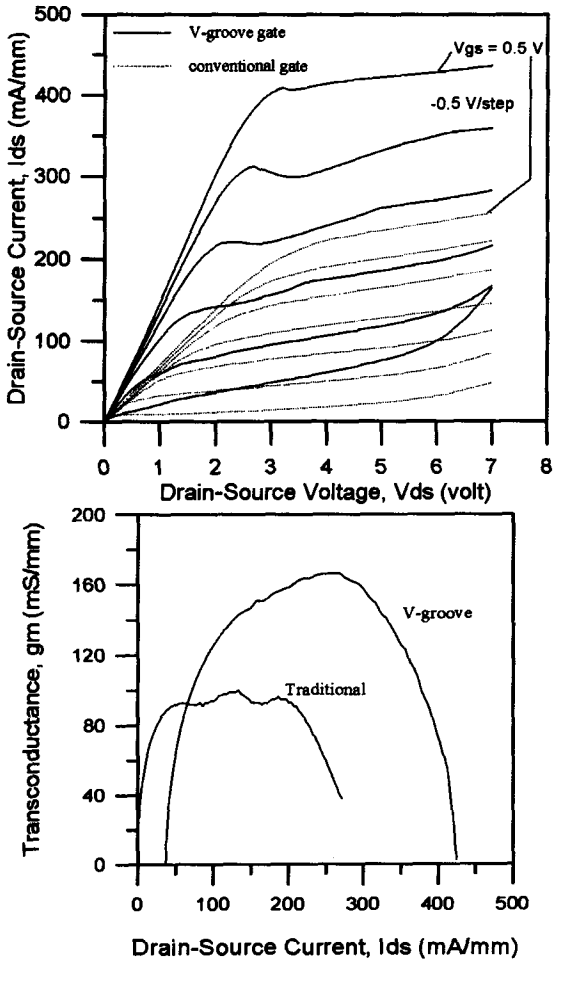
4. Results and discussion

Fig. 7 shows the plot of transconductance vs. drain-source current for both types of devices. Apparently, V-gate DCFET's have a larger dynamic range of I_{DS} of about 350 mA/mm for external transconductance exceeding 80 mS/mm. In contrast, the dynamic range of I_{DS} of traditional DCFET's is only about 200 mA/mm for $g_{m,ext}$ over 80 mS/mm. This implies better performance of



V-gate devices when used in power applications. We also observe a soft pinch-off characteristic in V-gate DCFET's. By soft pinch-off we refer to the increase of the gate turn-off voltage with increasing drain-source voltage. Also, the pinch-off voltage of V-gate DCFET's seems larger than that of conventional DCFET's. These consequences are in agreement with the simulation and experimental results reported by others. Microwave S-parameter measurements of both devices were also

carried out by a HP-8510C network analyzer in conjunction with a cascade direct probe station. The measurement spectrum ranges from 45 MHz to 26.5 GHz, and the DC bias point is chosen corresponding to the maximum DC transconductance of individual device. From the S-parameters we calculated the current gain cut-off frequency f_T, which is 8.3 GHz for strip-gate DCFET and 13.9 GHz for V-gate DCFET. Fig. 10 shows the I_{DS} dependence of f_T for both devices. Since the V-gate DCFET's exhibit higher values of f_T in a wider I_{DS} dynamic range, V-gate DCFET's are of better potential to work in high-speed high-power applications than their conventional gate counterparts.



5. Conclusion

In this work, a novel gate structure named *V-groove gate* is proposed as an attempt to achieve effectively submicrometer gate lengths using conventional 1-μm contact printing photolithography. The short gate length is obtained by anisotropically etching the uppermost undoped GaAs layer into a V-shaped groove. With proper etching solution and delicately designed i-GaAs thickness, theoretically an extremely short gate length can be achieved. Additional advantages of V-groove gates such as higher production yield and thicker attainable gate metal thickness are unveiled during process development. These are all favorable to mass production for commercial purposes.

The V-groove gate structure is applied to actual fabrication of $In_{0.49}Ga_{0.51}P/GaAs/In_{0.2}Ga_{0.8}As$ DCFET's. Compared with conventional strip gate devices, they exhibit a better current drivability, and leads to larger values of transconductance, channel current, and current-gain cut-off frequency. These better performances imply their potential of being used as a high-speed power device.

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< 專利說明書 >

一 發明名稱

含蝕刻停止層之 V 型谷空橋閘極的製造方法

Processing Method of V-groove Airbridge Gate with Etch-Stop Layer

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本發明可突破微影技術的限制而縮小閘極長度，對整個積體電路工業有根本的影響。本發明相較於其他具類似目的的技術有更高的良率及製程均一性，非常適合業界在量產方面的應用。

< 專利申請書 >

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Processing Method of V-groove Airbridge Gate with Etch-Stop Layer

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三 計劃名稱 磷化銦鎵／砷化鎵電晶體及電路(3/3)

計劃編號 NSC86-2221E002-046

呂學士 NT$

四、中文摘要：（以簡明文字說明敘述發明或創作內容之特點）

在此提出一種稱之為 "V 型谷空橋閘極" 的新穎閘極結構及其製造方法。首先於成長在元件主動層上面之未摻雜半導體層（例如砷化鎵、矽）中，以非等向性濕蝕刻技術蝕刻出一 V 型谷；接著蒸鍍上金屬，再以剝離法定義出閘極形狀。由於 V 型谷之斜坡的關係，可以在谷底得到比所使用之微影技術所能達到的最小線寬還要小很多的等效閘極長度。藉著一層位於元件主動層和未摻雜半導體層之間的蝕刻停止材料，吾人可以控制閘極金屬底部的垂直位置，使之恰好位在蝕刻停止層上。在閘極金屬條和閘極金屬極板之間，使用一空橋形狀的閘極饋線予以連接；此閘極饋線是以表面微加工技術，將原來位於閘極饋線下方的半導體材料蝕刻掉而形成的。

這種新穎的閘極結構可突破微影技術的限制，進一步縮小等效閘極長度，但不增加閘極電阻，並可得到較小的閘極雜散電容值。其應用在磷化銦鎵/砷化鎵/砷化銦鎵異質接面通道摻雜場效電晶體的製作上，已獲得了良好的成果。而蝕刻停止層的使用可獲致高的良率及製程均一性，非常適合業界在量產方面的應用。

英文摘要：

A novel gate structure called *V-groove Airbridge Gate* is proposed here, as well as the processing method to fabricate it. The gate is formed by anisotropic wet etching of undoped semiconductor (e.g. GaAs, Si) layer grown on top of device active layer(s), followed by standard metal evaporation and lift-off process. Owing to the outward slope of the sidewalls of the V-groove, effective gate length that is substantially smaller than the minimum feature size of available lithographic technology can always be obtained. The vertical location of the bottom of the gate metal is controlled by introducing a layer of etch-stop material between the uppermost undoped layer and device active layer(s). Gate strip and gate pad are connected by an airbridge-like gate feeder, which is fabricated by a surface micromachining technique that etches away the semiconductor materials beneath the gate feeder.

This kind of novel gate structure can shorten the effective gate length without the penalty of increased gate resistance, and can achieve smaller parasitic gate capacitances. It has been applied to the fabrication of InGaP/GaAs/InGaAs hetrojunction doped-channel FET's, and relatively good results have also been achieved compared with traditional gate structure. The introduction of the etch-stop layer leads to high

五、發明或創作背景：(即目前技術水平，本發明或創作所欲解決之問題及其技術範疇)

對場效電晶體而言，閘極長度的大小和電晶體本身的特性有著密切的關聯。一般來說，閘極長度越小，其高頻特性及噪音表現就越佳。目前商品化的積體電路，其閘極長度大都在 0.5 微米以下，以期能夠高速操作。這樣短的閘極，是以所謂的電子束微影技術(electron-beam lithography)來定義的。和一般的光學接觸式微影技術(optical contact printing)比較起來，電子束微影技術雖然具有定義次微米圖樣的能力，但它也有成本昂貴、製程費時的缺點。此外，隨著閘極長度的縮減，閘極金屬的雜散電阻也以同樣的比例增加。此增加的閘極電阻會增加電晶體的時間常數，而在某種程度上抵銷了縮短閘極長度所帶來的好處。因此，如何能夠同時達到縮短閘極長度及降低閘極電阻的目的，乃是朝高頻段-低雜音應用邁進的關鍵。

所謂的 T 形閘極或蘑菇形閘極，因為具有上寬下窄的橫截面形狀，因而可以同時縮短閘極長度並降低閘極電阻。歐美及日本均已先後發展出製造此種閘極的製程技術，並應用於電晶體的實際製造上，其結果證明上寬下窄的 T 形閘極或蘑菇形閘極的確可以達到比傳統平面形閘極更佳的頻率及雜音表現。但是在這些製程方法中，都需應用前述的電子束微影技術，並需配合所謂的多層光阻系統才能達成。由於製程的繁複導致不高的良率與製程均一性，再加上電子束微影技術的昂貴與費時，此種閘極在量產方面的應用始終有其限制。

本發明所欲解決的問題，即是想發展出一種較簡單的製程方法，來

製作出與 T 形閘極或蘑菇形閘極有相同優點的閘極結構，以達到高良率及高製程均一性。在本發明中，我們提出了一種名為"V 型谷空橋閘極"的新穎結構及其製程方法，作為前述問題的解決方案。其製程方法只牽涉到單層光阻與傳統的光學接觸式微影技術，不但大幅降低成本、簡化製程，並可達到高良率及高製程均一性。我們將此閘極結構直接應用在次微米閘極長度的磷化銦鎵/砷化鎵/砷化銦鎵異質接面通道摻雜場效電晶體的製作上，已獲得了良好的成果。

六、發明或創作說明：(應載明有關之先前技術，發明或創作之目的、技術內容、特點及功效，使熟習該項技術者能了解其內容並可據以實施)

對於場效電晶體而言，若能同時縮短閘極長度及降低閘極電阻，則可操作在更高的頻率範圍，並有更低的雜音指數[1]。所謂的 T 形閘極或蘑菇形閘極，因為具有上寬下窄的橫截面形狀，因而可以同時縮短閘極長度並降低閘極電阻。歐美及日本均已先後發展出製造此種閘極的製程技術[2]-[6]，並應用於電晶體的實際製造上，其結果證明上寬下窄的 T 形閘極或蘑菇形閘極的確可以達到比傳統平面形閘極更佳的頻率及雜音表現。但是在這些製程方法中，都需應用昂貴且費時的電子束微影技術，並需配合多層光阻系統才能達成，且其良率及製程均一性也都不甚令人滿意。

在本發明中，我們提出了一種名為"V 型谷空橋閘極"的新穎結構及其製程方法。此種閘極與 T 形閘極或蘑菇形閘極有著相同優點，即具有上寬下窄的橫截面形狀，可同時達到縮短閘極長度及降低閘極電阻的雙重目的。它優於 T 形閘極或蘑菇形閘極的地方是，其製程方法只牽涉到傳統的光學接觸式微影技術，且只使用單層光阻，大大地簡化了 T 形閘極繁複的製程方法，從而提高了製程良率及製程均一性，使得此種閘極結構適合於業界在量產方面的應用。

本發明中的閘極結構之所以稱為"V 型谷空橋閘極"，乃是因為它是藉著非等向性的 V 型谷濕蝕刻技術[7]-[8]來達成縮小等效閘極長度的目的。簡單來說，首先於成長在元件主動層上面之未摻雜半導體層（例如砷化鎵、矽）中，以非等向性濕蝕刻技術蝕刻出一 V 型谷；接著蒸

鍍上金屬，再以剝離法定義出閘極形狀。由於 V 型谷之斜坡的關係，可以在谷底得到比所使用之微影技術所能達到的最小線寬還要小很多的等效閘極長度。藉著一層位於元件主動層和未摻雜半導體層之間的蝕刻停止材料，吾人可以控制閘極金屬底部的垂直位置，使之恰好位在蝕刻停止層上。至於"空橋"一詞，乃是指在閘極金屬條和閘極金屬極板之間，使用一空橋形狀的閘極饋線予以連接；此閘極饋線是以表面微加工技術，將原來位於閘極饋線下方的半導體材料蝕刻掉，而形成類似空橋的外形。這樣的空橋結構具有較小的閘極雜散電容值，可進一步改善電晶體的高頻響應[9]；此外，空橋結構也可增加電晶體的崩潰電壓，而提高其輸出功率[10]。

以下，以一磷化銦鎵/砷化鎵/砷化銦鎵異質接面通道摻雜場效電晶體為例，詳述 V 型谷空橋閘極結構應用在電晶體製作上的製程方法及獲致的結果。

此電晶體的異質磊晶層結構如第一圖所示。最上面的是一層厚約 1 微米的未摻雜砷化鎵，V 型谷就是在這一層未摻雜砷化鎵上利用非等向性濕蝕刻技術蝕刻出來的。接下來的是一層厚 100 埃的未摻雜磷化銦鎵，它對於砷化鎵有很好的蝕刻選擇率[11]-[14]，故可做為 V 型谷蝕刻時的蝕刻停止層。同時，它也扮演了通道摻雜場效電晶體中絕緣層的角色。接下來，同為 3×10^{18} cm^{-3} n 型摻雜的一層 100 埃的砷化鎵和一層 150 埃的砷化銦鎵，是做為元件之通道層。其下是 5000 埃的未摻雜砷化鎵緩衝層，以及(100)砷化鎵基板。

此電晶體之 V 型谷閘極的製程方法如第二圖所示。在以濕蝕刻完

成一般的島狀元件隔離，並以退火處理源-汲極的蒸鍍金屬以形成歐姆接點後，先在閘極區域上旋覆一層光阻，請參見第二圖(a)。其次，以傳統的光學接觸式微影技術，沿著$(01\bar{1})$的方向在光阻上定義出閘極長度約為 1 微米的閘極金屬條之圖樣，如第二圖(b)所示。接著，以非等向性蝕刻溶液(如硫酸-雙氧水-水之蝕刻溶液系統)，在閘極定義區域進行蝕刻。由於砷化鎵的晶格結合是屬於閃鋅結構，因此在非等向性蝕刻溶液中會呈現{111}Ga 的斜面，如第二圖(c)所示。此非等向性蝕刻過程會在往下蝕刻至磷化銦鎵蝕刻停止層時自動停止，而形成如第二圖(d)所示的 V 型谷結構。最後，以真空蒸鍍的方式蒸鍍上鈦/鉑/金或鉻/金等金屬，再以剝離法定義出閘極金屬區域，如第二圖(e)所示。在第二圖(e)中可以清楚地看出，V 型谷閘極的等效閘極長度(即閘極金屬和磷化銦鎵絕緣層接觸部份的長度)，比起微影技術在光阻上定義出來的長度要小了許多。若適當地選擇最上面的未摻雜砷化鎵層的厚度和恰當的蝕刻溶液，理論上我們甚至可以達成等效閘極長度幾乎為零的V型谷閘極。除了縮短閘極長度之外，V 型谷閘極結構還有下面幾項優點：(1) V 型谷蝕刻可幫助達到將近 100 % 的閘極金屬剝離良率；(2) V 型谷蝕刻使得吾人可以增加閘極金屬的厚度，而進一步降低閘極電阻；(3) V 型谷閘極與 T 形閘極或蘑菇形閘極一樣，具有上寬下窄的橫截面形狀，適合於自我對正閘極(self-aligned gate)的實現，可降低源極及汲極電阻。

至於空橋形狀之閘極饋線的形成方法，請參見第三圖。首先我們在製作完成的 V 型谷閘極上旋覆一層光阻，再於閘極饋線的區域以光學

接觸式微影技術開出一個窗口。接著，以硫酸-雙氧水-水和鹽酸-磷酸蝕刻溶液進行表面微加工技術，以蝕刻掉閘極饋線下方的各半導體層。其中，鹽酸-磷酸蝕刻溶液是用來蝕刻磷化銦鎵，而硫酸-雙氧水-水蝕刻溶液則是用來蝕刻砷化鎵及砷化銦鎵的。第四圖中顯示了傳統閘極結構(第四圖(a))和空橋閘極結構(第四圖(b))的上視圖和側視圖。從圖中可以看出兩者明顯的不同。

製作完成的 V 型谷閘極結構剖面圖請參見第五圖。在第五圖(a)中可以清楚看出，一等效閘極長度約為 0.6 微米的 V 型谷閘極已成功地被製作在未摻雜砷化鎵的 V 型谷中，其閘極金屬的底部恰好接觸在磷化銦鎵蝕刻停止層上。此 V 型谷閘極乃是用線寬為 1.2 微米的光學接觸式微影製程技術製作出來的。而在第五圖(b)中，我們使用線寬為 1 微米的微影技術，在較厚的未摻雜砷化鎵層中，可以製造出谷底長度(即等效閘極長度)幾乎為零的 V 型谷閘極。另外值得注意的是，因為在金屬蒸鍍前多了 V 型谷蝕刻的製程步驟，閘極金屬可以較一般平面型閘極鍍得更厚，閘極電阻也可因而進一步降低。在第五圖(b)中清楚地顯示出，即使閘極金屬厚至 1 微米以上，仍可順利地完成金屬剝離。

上面的實驗結果顯示，V 型谷空橋閘極是一種達到次微米閘極電晶體的有效方法。它和現有的方法比較起來，有著較低的成本和較高的良率與製程均一性，極具工業界量產的潛力。雖然本發明已以一較佳實例揭露如上，然其並非用以限定本發明，任何熟習此項技藝者，在不脫離本發明之精神和範圍內，當可作些許之更動與潤飾，因此本發明之保護範圍後附之申請專利範圍所界定者為準。

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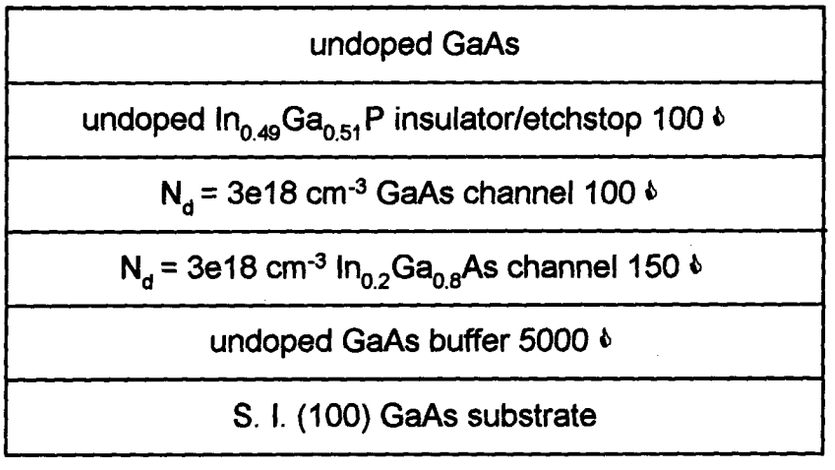
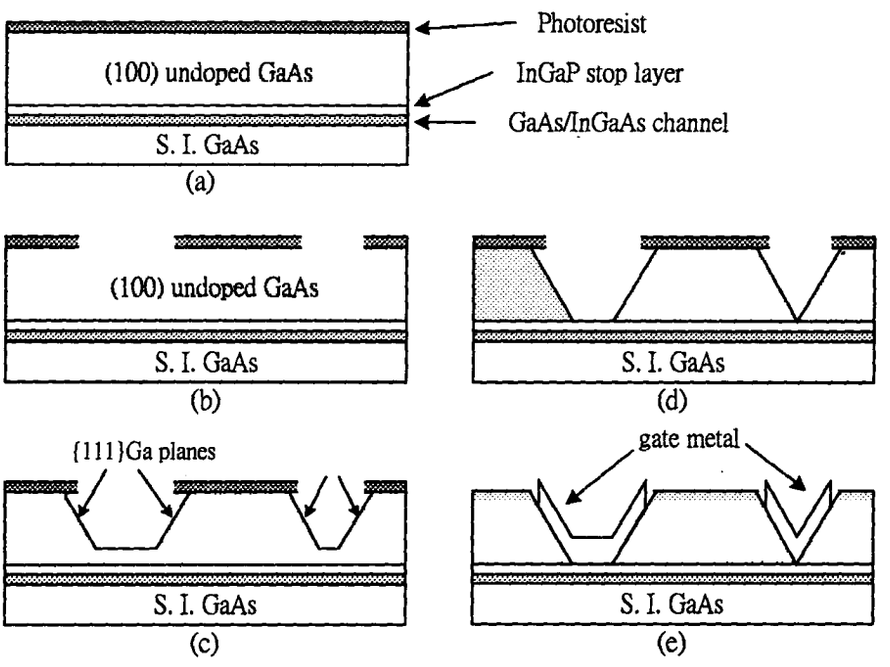
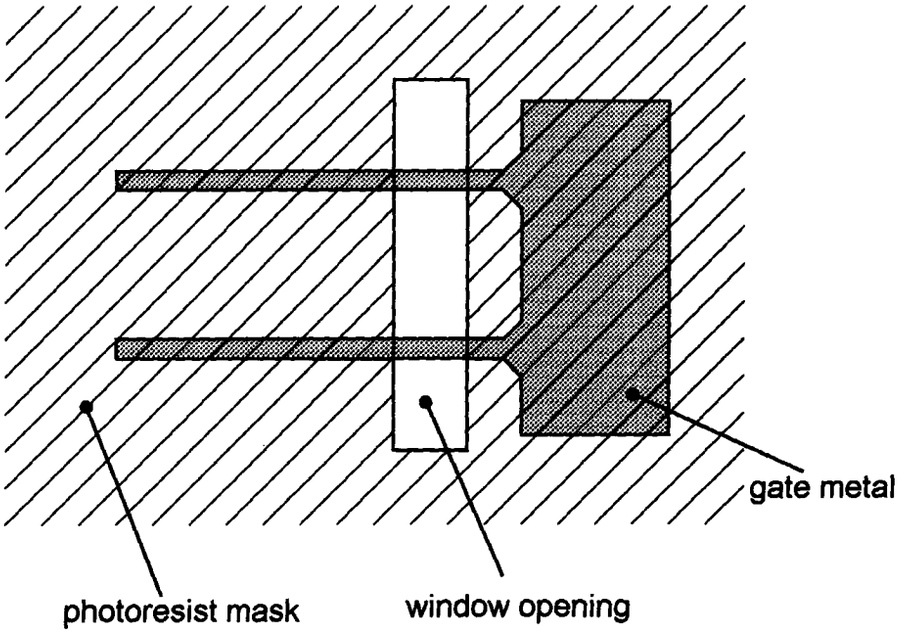


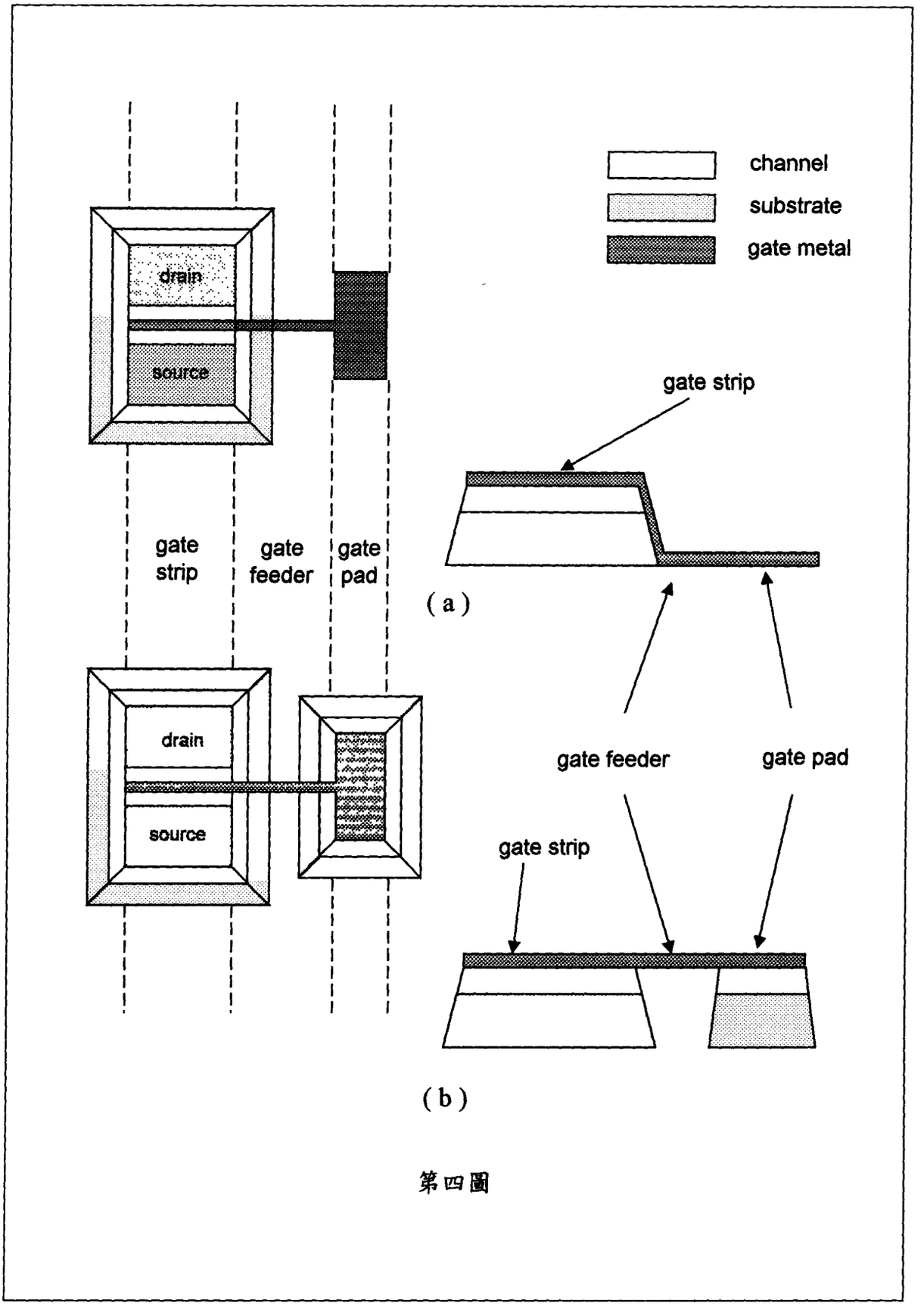
第一圖


Photoresist
(100) undoped GaAs
InGaP stop layer
GaAs/InGaAs channel
S. I. GaAs
(a)
(100) undoped GaAs
S. I. GaAs
(b)
S. I. GaAs
(d)
{111}Ga planes
S. I. GaAs
(c)
gate metal
S. I. GaAs
(e)

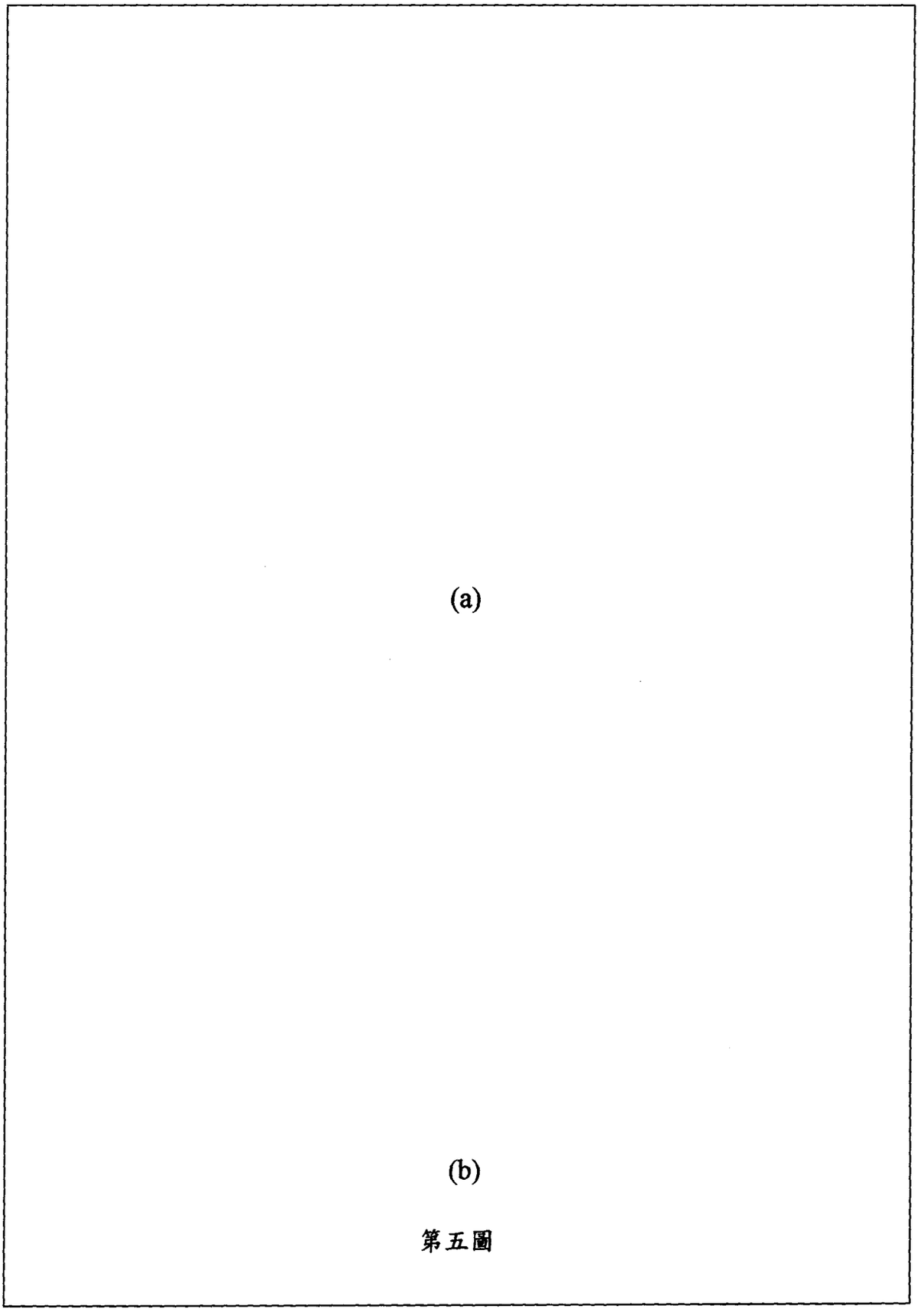
第二圖


gate metal
photoresist mask
window opening

第三圖


channel
substrate
gate metal
drain
source
gate strip
gate feeder
gate pad
(a)
gate strip
gate feeder
gate pad
drain
source
gate strip
(b)

第四圖



(a)

(b)

第五圖

七、申請專利範圍：（即 Claims，惟在撰寫申請專利範圍前，請考慮其①新穎性②進步性③實用性之組成、配方、製程、條件等，並以條列方式詳述說明之。）

1. 一種場效電晶體或其積體電路的閘極製造方法，包括下列步驟：
   (a) 提供一半導體基板；
   (b) 在該半導體基板上，以磊晶成長或離子佈植等方式，形成一層或一層以上的元件通道層；
   (c) 在元件通道層的上方，成長一層或一層以上的蝕刻停止層；
   (d) 在蝕刻停止層的上方，成長一層未摻雜半導體層；
   (e) 在未摻雜半導體層上，定義出閘極圖樣，並用非等向性蝕刻技術在未摻雜半導體層上蝕刻出一 V 型谷，使其下的蝕刻停止層於 V 型谷谷底曝露出來；
   (f) 在 V 型谷中放置閘極材料形成閘極。

2. 如申請專利範圍第 1 項所述之製造方法，其中在步驟(e)、(f)之間，更包括了：
   (ei) 去除曝露於谷底的蝕刻停止層。

3. 如申請專利範圍第 1 項所述之製造方法，其中在步驟(f)之後，更包括了：
   (g) 去除閘極饋線之下的半導體材料以形成空橋閘極結構。

Processing Method of V-groove Airbridge Gate with Etch-Stop Layer

Field of The Invention

A novel gate structure called V-groove Airbridge Gate is proposed here, as well as the processing method to fabricate it.

Background of The Invention

For field effect transistors (FET), the effective gate length is closely related to the characteristics of the FET. In general, the smaller the gate length the better the performance of high frequency and noise, etc.. Among current GaAs IC commercialized products, most of the gate lengths are shorter than 0.5 um for high-speed operations. Such short gate length is better defined by electron-beam lithography. Compared with the general optical contact printing technology, the electron-beam lithography can define sub-um pattern, is more expensive and waste more time in processing. In addition, when the gate length decreases, the parasitic resistance of gate metal is proportionally increased as well. The increased gate resistance will increase FET's time constant and discount the benefit obtained from the shortened gate lengths. Therefore, how to achieve shorter gate length and lower gate resistance at the same time is the key to the applications of the high-frequency and low-noise.

The so-called T-shape gate or mushroom-like gate, owing to its broader upper side and narrower lower side in a cross section, can shorten gate length and, at the same time, lower gate resistance. Most industrialized countries like Japan or the United States have developed the processing method for this kind of gates and applied it to the manufacturing of transistors. They have proved that T or mushroom gates are better than conventional plain gates in terms of high frequency and noise performances. However, T gate and mushroom gate are processed or produced by applying previously mentioned electron-beam lithography and by multiple layer photoresist system. Because of its complex production process which leads to low yield and low uniformity of the product, as well as high-cost and length of time needed for electron-beam lithography, it has certain restrictions in mass production applications.

The novel invention has considered the above-mentioned drawbacks in producing T-shape or mushroom-like gate and hence develop a much simpler method to fabricate the T-shape gate but with high yield and uniformity.

Therefore, we propose here a V-groove Airbridge Gate as well as the processing method to fabricate it. The production or fabrication of the novel gate is only involved with single

layer photoresist and conventional optical contact lithography, which greatly lowered the production costs and simplified the production techniques to achieve high yield and uniformity in the processing method.

Cross-reference To Previous Techniques

In 1979, H. Fukui reported in *IEEE Trans.* Electron Devices, ED-26(7), that shorter gate length and lower gate resistance will have higher frequency operating ranges and lower noise figures. And the T-shape or mushroom gate mentioned above are a much better choice in this regard due to its broader upper side and narrower lower side in cross section. From 1980 onwards, many techniques have been developed for the production of a variety of gates, in Japan, Europe and the U.S. In 1987, P. C. Chao, et al, proved in IEEE IEDM Tech. Digest, pp.410-413, that T-shape or mushroom-like gates are better than conventional plain gates in terms of high frequency and low noise performances. But it was processed or produced by applying previously mentioned electron-beam lithography and multiple layer photoresist system. Because of its complex production process which leads to low yield and low uniformity of the production process, the electron-beam lithography is time-consuming and incurs a high cost.

The so-called novel gate structure of the "V-groove Air-bridge Gate" refers to the papers concerning anisotropic V-groove wet etching technique reported by S. Iida, et al, in 1971 in J. Electrochem. Soc., 118(5), pp.768-771 and D. W. Shaw, et al, in the same year of the same Journal, 128(4), pp.874-880. Simply speaking, the technique involves, firstly, the use of anisotropic wet etching technique to etch a V-groove on the undoped semiconductor(e.g. GaAs, Si) layer grown on top of the device active layer(s); and, secondly, the use of standard metal evaporation and lift-off process to define gate patterns. Owing to the outward slope of the sidewalls of the V-groove, effective gate length that is substantially smaller than the minimum feature size of the available lithographic technology can always be obtained. The vertical location at the bottom of the gate metal is controlled by introducing a layer of etch-stop material between the uppermost undoped layer and device active layer(s) and thus etching stops at the etch-stop layer. As to the term "airbridge", it refers to the gate strip and gate pad which are connected by an airbridge-like gate feeder fabricated by a surface micromatching technique that etches away the semiconductor materials beneath the gate feeder and forms the airbridge-like configuration.

This kind of air-bridge structure has smaller parasitic gate capacitances. According to K. Y. Hur, et al, in 1993 *IEEE Trans. Electron Devices*, ED-40(10), pp.1736-1739, the novel structure can further improve transistor's high-frequency performances. In addition, Y. J. Chan, et al, in 1991 of IEEE Electorn Device Lett., EDL-12(7), pp.360-362, reported that it can also

increase EFT's breakdown voltages to enhance its output power.

Summary of The Invention

The V-groove gate is much like the T-shape gate in that it has a broader upper side and narrower lower side in its cross section, and achieve short gate length and low gate resistance, at the same time. However, the production or working process of the proposed novel V-groove gate only involves single layer photoresist and conventional optical contact lithography. This processing method greatly lowers the production costs and simplifies the production techniques to achieve high yield and uniformity, and is better than traditional T-shape gate.

Brief Descriptions of Drawings:

Figure 1 shows the epitaxial structure of the device to be purchased

2...undoped GaAs as the major layer for V-groove formation
3...undoped InGaP as the layer of etch-stop
5...GaAs channel 6...InGaAs channel
7...undoped GaAs buffer
100...S.I. GaAs

Figure 2 is a diagram which briefly illustrates the V-groove gate processing method

(a) spin on photoresist

(b) photo exposure to define1 um gate length

(c) use sulfuric acid solution to etch away GaAs and expose {111}Ga sloped plane

(d) etching stops at the layer of InGaP

(e) metal evaporation

1...photoresist 2...(100) undoped GaAs
3...InGaP stop layer 4...GaAs/InGaAs channel
8...gate metal 9...{111}Ga slope

Figure 3 shows how air-bridge gate structure is formed.

11...photoresist mask 12...window opening
13...gate feeder zone

Figure 4 shows traditional gate structure and air-bridge gate structure.

(a) top view (b) side-section view

14...drain 15...source
17...substrate 18...channel
19...gate strip 20...gate feeder
21...gate pad

Figure 5 shows the V-groove gate structures we have fabricated.

(a) 0.6 um V-groove gate (b) V-groove gate with almost zero um gate length

Figure 6 is a cross section view that shows the V-groove gate structure

(a) effective gate length of 0.6 um of an V-groove gate

(b) gate length close to 0 of an V-groove gate

Detail Descriptions of The Invention

A method of producing sub um gate transistor using anisotropic wet etching and selective etching, followed by standard evaporation and lift-off process, which consists of the following steps:

(a) provide a semiconductor substrate.

(b) grow unit's channel layer(s) on the semiconductor substrate by epitaxial growth or ion implantating.

(c) grow etch-stop layer(s) on the channel layer.

(d) grow an undoped semiconductor on the etch-stop layer.

(e) define gate patterns on the undoped layer and use selective etching to etch away an anisotropic V-groove on the undoped semiconductor layer and let the etch-stop layer beneath the undoped layer be exposed to the bottom of the V-groove.

(f) put gate materials into V-groove to form gate strip.

(g) remove the semiconductor material under the gate feeder to form air-bridge gate structure.
The above steps are the method used for producing the novel V-groove gate structure.

Among them, the semiconductor substrate can be any semiconductors upon which other III-V compound semiconductor can be grown, the most suitable substrate is GaAs. The channel semiconductor has high electron mobility, the most suitable channel material is GaAs or InGaAs. The undoped semiconductor layer has low electrical conductivity, the most suitable material is GaAs. The material used for the etch-stop layer is different from the undoped semiconductor layer in terms of the etching rate, for example, using InGaP.

The above-mentioned gate patterns are contained in the photosensitive layers on the surface of the gate substrate; the photosensitive layer has been patterned by the process of exposure and developing. Because of the patterned photo sensitive layer, some areas underneath the epitaxial layer are exposed to the air while other areas are not. The photosensitive layer illustrated here is essentially a photoresist layer which can be exposed through photo mask and ultraviolet light. Chemical etching solutions can be any solutions that have different etching rates to undoped semiconductor and etch-stop layer respectively; and the chemical solutions can etch V-groove on the undoped semiconductor. The airbridge structure is formed by using any solutions that have different etching rates to the gate and the layers beneath it. The solutions for etching can be hydrochloric acid and phosphoric acid solution and sulfuric acid peroxide-H2O solution.

Detail Descriptions of The Preferred Enbodiments

The following example uses InGaP/GaAs/InGaAs heterojunction doped-channel FET to illustrate and describe

the application of the V-groove airbridge gate structure in transistor fabrication, its processing method and the demonstrated results.

Figure 1 shows heterojunction epitaxial layer structure. The uppermost layer is undoped GaAs with the thickness of 1 um, of which the V-groove is etched by anisotropic wet etching technique. The layer below it is undoped InGaP with a thickness of 100Å(10^{-8} m) and, according to H. Ito et al, in 1995, J. Electrochem. Soc., 142(10), pp.3383-3386, undoped InGaP is good for V-groove etching as etch-stop layer because of its etching selectivity between GaAs and InGaP. And, at the same time, it also acts as an isulator to doped-channel FET. The subsequent layers are 3×10^{18} cm^{-3} N-type doped 100Å(10^{-8} m) GaAs and 150Å(10^{-8} m) InGaAs, forming the device's channel layers. At to the bottom are 5000Å(10^{-8} m) undoped GaAs buffer and GaAs substrate(100).

Figure 2 shows the processing method of FET V-groove gate. After finishing the job of normal isolation of mega by wet etching and introducing ohmic contacts of source and draineen to mesas, spin-on a layer of photoresist on the water, as shown in Figure 2(a). Secondly, define the pattern of the gate strip with the gate length of 1 um along the direction of (011) on the photoresist by using conventional optical contact lithography, as shown in Figure(b). Thirdly, use anisotropic etching solutions (such as sulfuric acid-hydrogen peroxide-H2O solution) to etch on the patterned gate region. Slopped Ga{111} is exposed, as shown in Figure 2-(c), in the anisotropic etching solution because of zinc-blende structure. When the process of the anisotropic etching reaches the InGaP stop layer, it would automatically stop etching and the V-groove is formed as shown in 2-(d). Finally, use vacuum evaporation method to deposit Ti/Pt/Au or Cr/Au on the V-groove and define gate metal region by the lift-off process, as shown in (e). From Figure 2(e), one can clearly see the effective gate length (which is the length of the contacting parts of the gate metal and InGaP) of the V-groove gate is significantly smaller than that of the photoresist layer defined by lithography. If however right from the very beginning, we have chosen the suitable thickness and etch solutions for the undoped GaAs located on the uppermost layer, the effective gate length of the V-groove gate will be close to 0. In addition to shortening the gate lengths, the V-groove gate structure still has the following features: (1) V-groove etching can contribute to close to 100% successful rate of lifting-off the gate material; (2) V-groove etching help increase thickness of the gate metal and lower gate resistance; (3) V-groove gate, like T-type or mushroom-like gate, can have upper part broader and lower part narrower configuration in cross section, which is suitable for the realization of self-aligned gates and can lower gate-to-source and gate-to-drain resistance.

As to formation of air-bridge like gate feeder, please

refer to Figure 3. First, we spin-on a photoresist layer on the gate and, then, open up a window in the gate feeder region by using optical contact lithography. Then, we use sulfuric acid-hydrogen peroxide-H2O solution and hydrochloric acid-phosphoric acid solution to do surface micromatching and etch away the semiconductor materials beneath the gate feeder. Whereas hydrochloric acid-phosphoric acid solution is used to etch InGaP, sulfuric acid-hydrogen peroxide-H2O solution is for GaAs and InGaAs etching. Figure 4(a) and 4(b) show respectively traditional gate structure's top view and cross-section view; while Figure 5(a) and (b) show respectively air-bridge gate structure's top view and cross-section view; the two different pictures show the different gate structures.

Figure 6 shows the cross-section view of the finished V-groove gate structure. From Figure 6(a), it clearly demonstrates that a gate length of 0.6 um has been successfully produced in the V-groove of the undoped GaAs and the bottom of the gate metal just touching the etch-stop layer of InGaP. The V-groove gate, however, is produced by 1.2 um line width of optical contact lithography process technique. While in Figure6(b) we use 1um line width of the same process technique to produce close to 0 um V-groove gate length(which means effective length) in the thicker undoped GaAs layer. It should be noted that because there is V-groove etch process taken place before the metal evaporation, the gate metal would be thicker than average plain gates as a result of the metal evaporation and the gate resistance can be further lower down. Furthermore, Figure 6 (b) also shows that even in the case of 1um thick gate metal, the lift-off process can still be performed successful.

The above example has illustrated and demonstrated that V-groove airbridge gate is an effective method of producing sub-um gate transistor. Compared with the other conventional methods, it costs less and has higher yield and uniformity, which makes it suitable for mass production in the industry. Anyone familiar with the above-mentioned innovative technique, can further develop the novel structure without restrictions if the basic principles and spirit of the invention are abided by. However, the claims by the invention, as shown below, shall be strictly adhered to.

WHAT IS CLAIMS IS:

1. A method of producing sub-um gate transistor using anisotropic wet etching, comprising the following steps:

(a) provide a semiconductor substrate

(b) grow device's channel layer(s) on the semiconductor substrate by epitaxial growth or ion implantating.

(c) grow etch-stop layer(s) on the channel layer.

(d) grow an undoped semiconductor on the etch-stop layer.

(e) define gate patterns on the undoped layer and use selective etching to etch away an anisotropic V-groove on the undoped semiconductor layer and let the etch-stop layer beneath the undoped layer be exposed to the bottom of the V-groove.

(f) put gate materials into V-groove to form gate strip.

(g) remove the semiconductor material under the gate feeder to form air-bridge gate structure.
The above steps are the method used for producing the novel V-groove gate structure.

2. With respect to the processing method described above in Claim 1, the semiconductor substrate can be any semiconductors upon which other III-V compound semiconductors can be grown.

3. With respect to the processing method described above in Claim 2, the semiconductor substrate is GaAs.

4. With respect to the processing method described above in Claim 1, the channel semiconductor has high etching rate of electrons.

5. With respect to the processing method described above in Claim 4, the channel layer is GaAs or InGaAs.

6. With respect to the processing method described above in Claim 1, the undoped semiconductor has low electrical conductivity.

7. With respect to the processing method described above in Claim 6, the undoped semiconductor is undoped GaAs

8. With respect to the processing method described above in Claim 1, the etch-stop layer uses semiconductors that have different etching rates from those of the semiconductors used in claim 6.

9. With respect to the processing method described above in Claim 8, the etch-stop layer is InGaP.

10. With respect to the processing method described above in Claim 1, the gate patterns are contained in the photosensitive layers on the surface of the gate substrate; the photosensitive layer was patterned by the process of exposure and developing.

11. With respect to the processing method described above in Claim 10, because some of the patterned photo sensitive layer are underneath, epitaxial layer is exposed to the air.

12. With respect to the processing method described above in Claim 10, because some of the patterned photo sensitive layer are underneath, epitaxial layer is exposed to the air while the other areas are not.

13. With respect to the processing method described above in Claim 10, only the parts that are exposed are being etched away in step (e).

14. With respect to the processing method described above in Claim 10, the photosensitive layer is essentially a photoresist layer which cannot be exposed unless through photo mask and ultraviolet rays.

15. With respect to the processing method described above in Claim 1, the chemical solutions used shall have different etching rates to undoped semiconductors and etch-stop layers.

16. With respect to the processing method described above in Claim 15, the chemical solutions can then etch away V-groove on the undoped semiconductor.

17. With respect to the processing method described above in Claim 15, the solutions used shall be sulfuric acid-hydrogen peroxide-H2O solutions and the like.

18. With respect to the processing method described above in Claim 1, the air-bridge structure would use any solutions that have different etching rates to the gate and the layers beneath it.

19. With respect to the processing method described above in Claim 18, the solution used for etching is either hydrochloric acid-phosphoric acid solution or sulfuric-hydrogen peroxide-H2O solution in this case.

Abstract

A novel gate structure called V-groove Airbridge Gate, as well as the processing method to fabricate it, are proposed here. The gate is formed by anisotropic wet etching of undoped semiconductor(e.g. GaAs, Si) layer grown on top of the device active layer(s), followed by standard metal evaporation and lift-off process. Owing to outward slope of the sidewalls of the V-groove, the effective gate length that is substantially smaller than the minimum feature size of available lithographic technology can always be obtained. However, the vertical location at the bottom of the gate metal is controlled by introducing a layer of etch-stop material between the uppermost undoped layer and device active layer(s). Gate strip and gate pad are connected by an airbridge-like gate feeder, which is fabricated by a surface micromatching technique that etches away the semiconductor materials beneath the gate feeder.

This kind of novel gate structure overcomes the limitations of the existing lithographic technology, can shorten the effective gate length without the penalty of increased gate resistance, and can achieve smaller parasitic gate capacitances. It has been applied to the fabrication of InGaP/GaAs/InGaAs heterojunction doped-channel FET's and relatively good results have also been achieved compared with traditional gate structure. The introduction of the etch-stop layer leads to high yield and uniformity, which is important in industrial mass-production applications.