Universal switch blocks for three-dimensional FPGA design

G.-M. Wu, M. Shyu and Y.-W. Chang

Abstract: The authors consider the switch-block design problem for three-dimensional FPGAs. A three-dimensional switch block M with W terminals on each face is said to be universal if every set of nets satisfying the dimension constraint (i.e. the number of nets on each face of M is at most W) is simultaneously routable through M. A class of universal switch blocks for three-dimensional FPGAs is presented. Each of the switch blocks has $15W$ switches and switch-block flexibility 5 (i.e. $F_S = 5$). It is proved that no switch block with less than $15W$ switches can be universal. The proposed switch blocks are compared with others of the topology associated with those used in the Xilinx XC4000 FPGAs. Experimental results demonstrate that the proposed universal switch blocks improve routabilty at the chip level. Further, the decomposition property of a universal switch block provides a key insight into its layout implementation with a smaller silicon area.

1 Introduction

A conventional field-programmable gate array (FPGA) (Fig. 1*a*) consists of an array of logic blocks that can be connected by routing resources [1]. The logic blocks contain circuits used to implement logic functions. The routing resources consist of wire segments and switch blocks. Figure 1*b* illustrates a switch block in which the programmable switches, denoted by dashed lines between terminals, are shown. There are many reports on four-sided switch blocks [2–8].

A three-dimensional FPGA architecture (Fig. 2*a*) is a generalisation based on the conventional 2-D FPGA; it stacks a number of 2-D FPAG blocks together by MCM fabrication techniques [9, 10], where each logic block has six adjacent neighbours, as opposed to four in the 2-D case [9]. The 3-D switch blocks are not the same as the conventional switch blocks (Fig. 2*b*). Each switch block is connected with six adjacent switch blocks. Therefore, they enable each channel segment to connect to some subset of the channel segments incident on the other five faces of the 3-D switch block. This unique architecture motivates our study of the 3-D switch blocks.

A three-dimensional switch block M with W terminals on each face is said to be universal if every set of nets satisfying the dimension constraint (i.e. the number of nets on each face of M is at most W) is simultaneously routable through M. This paper presents a class of universal switch blocks for three-dimensional FPGAs. Each switch block has $15W$ switches and switch-block flexibility 5 (i.e $F_S = 5$). We prove that no switch block with less than $15W$ switches can be universal. We also compare the proposed switch blocks with others of the topology associated with those used in the Xilinx XC4000 FPGAs. Experimental results demonstrate that the universal switch blocks improve routabilty at the chip level.

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2 Switch-block modelling

This Section presents the modelling for 3-D switch blocks and their routing. It is shown that the 3-D switch-block design problem can be transformed into the six-sided one. A three-dimensional switch block is a cubic block with W terminals on each face of the block. The size of the 3-D switch block is referred W. Some pairs of terminals, on different faces of the block, may have programmable switches and thus can be connected by programming the switches to be 'ON'. We represent a 3-D switch block by $M_{3d}(T, S)$, where T is the set of terminals, and S the set of switches. Let the faces F_1, F_2, F_3, F_4, F_5, and F_6 represent the front, rear, left, right, top, and bottom faces, respectively (Fig. 3). Label the terminals $t_{1,1}$, $t_{1,2},\ldots,t_{1,W}$, $t_{2,1}$, $t_{2,2},\ldots,t_{2,W},\ldots,t_{6,1}$, $t_{6,2}$, …, $t_{6,W}$ starting from the terminals on F_1 to those on F_6. Let $T(F) = \{t_{1,1}, \ldots, t_{1,W}\}$ (front terminals), $T(H) = \{t_{2,1},\ldots, t_{2,W}\}$ (rear terminals), $T(L) = \{t_{3,1}, \ldots, t_{3,W}\}$ (left terminals), $T(r) = \{t_{4,1}, \ldots, t_{4,W}\}$ (right terminals), $T(T) = \{t_{5,1},\ldots, t_{5,W}\}$ (top terminals), and $T(B) = \{t_{6,1}, \ldots, t_{6,W}\}$ (bottom terminals). Figure 3*b* shows the labelling of the terminals on F_i. Therefore, $S = \{(t_{i,j}, t_{p,q})|$ there exists a programmable switch between $t_{i,j}$ and $t_{p,q}\}$, and $T = \cup_{i\in\{F,H,L,R,T,B\}} T(i)$. For convenience, we often refer to a switch block $M_{3d}(T,S)$ simply as M_{3d}, omitting T and S, if there is no ambiguity about T and S, or T and S are not of concern in the context.

A hexagonal switch block (HSB) is a six-sided switch block with V terminals on each side of the block. We say that the HSB is of size V. We represent an HSB by $M_h(T_h,S_h)$, where T_h is the set of terminals and S_h the set of programming switches. Label the terminals $t_{1,1}$, $t_{1,2},\ldots$, $t_{1,V}$, $t_{2,1}$, $t_{2,2},\ldots$, $t_{2,V},\ldots$, $t_{6,1}$, $t_{6,2},\ldots,t_{6,V}$ starting from the rightmost terminal on the bottom side and proceeding clockwise (Fig. 3*c*). Let $T_h(i) = \{t_{i,1}, \ldots, t_{i,V}\}$,

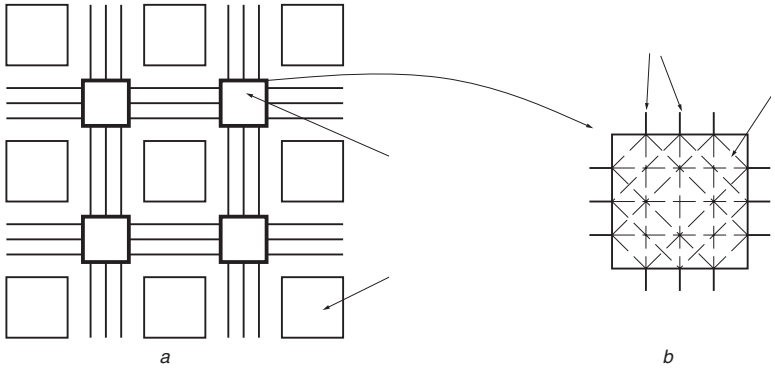

Fig. 1 *Conventional FPGA and its switch block*
a Conventional FPGA architecture
b Conventional four-sided switch block

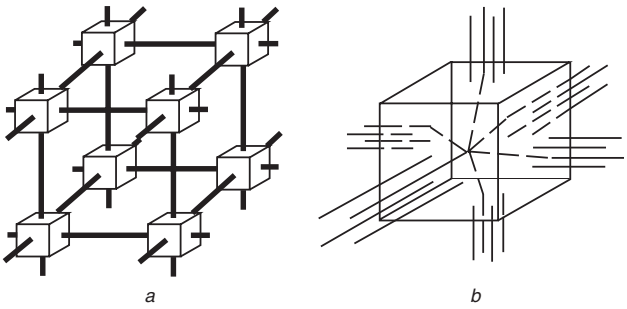

Fig. 2 *3-D FPGA and switch block*
a 3-D FPGA
b 3-D switch block

where $i = 1,2,3,4,5,$ or 6. Therefore, $S_h = \{(t_{m,n},t_{u,v})|$ there exists a programmable switch between terminal $t_{m,n}$ and terminal $t_{u,v}\}$, where $m \neq u$, $m,u = 1,2, \ldots, 6$, n, $v = 1,2, \ldots, V$, and $T_h = \cup T_h(i)$, where $i = 1, 2, \ldots, 6$. For convenience, we often refer to $M_h(T_h, S_h)$ simply as M_h, omitting T_h and S_h, if there is no ambiguity about T_h and S_h, or T_h and S_h are not of concern in the context.

In the following, we transform the design problem for the 3-D switch blocks into that for the HSBs. For convenience, we modify the terminology isomorphism used in [3] as follows. Let $M(T, S)$ $(M'(T', S'))$ be a 3-D or a hexagonal switch block. We have the following definition.

Definition 1: Two switch blocks $M(T, S)$ and $M'(T', S')$ are isomorphic if there exists a bijection $f: T \rightarrow T'$ such that $(t_{m,n},t_{u,v}) \in S$ if and only if $(f(t_{m,n}), f(t_{u,v})) \in S'$ and, for any two terminals $t_{m,n}$, and $t_{u,v}$, $t_{m,n}$, $t_{u,v} \in T$ if and only if $f(t_{m,n})$, $f(t_{u,v}) \in T'$.

In other words, $M(T,S)$ and $M'(T', S')$ are isomorphic if we can relabel the terminals of M to be the terminals of M', maintaining the corresponding switches in M and M'; and for terminals on the same side (face) of M, their corresponding terminals are also on the same side (face) of M'. For any two isomorphic switch blocks, we have the following theorems.

Theorem 1: [3] Any two isomorphic switch blocks have the same routing capacity.

Theorem 2: For any M_{3d} of size W, there exists an M_h of the same size such that M_{3d} and M_h are isomorphic, and vice versa.

Proof: For an $M_{3d}(S,T)$ of size W, we can construct an $M_h(S_h,T_h)$ of the same size such that $(t_{m,n},t_{u,v}) \in S_h$ if $(t_{m,n}, t_{u,v}) \in S$, where $m \neq u$, $m,u = 1,2, \ldots, 6$ and $n,v = 1,2, \ldots, W$. Let the mapping function $f: T \rightarrow T_h$ be $f(t_{m,n}) = t_{m,n}$. Obviously, $(t_{m,n}, t_{u,v}) \in S$ if and only if $(f(t_{m,n}), f(t_{u,v})) = (t_{m,n}, t_{u,v}) \in S_h$. Therefore, by definition 1, M_{3d} and M_h are isomorphic. For an $M_h(S_h, T_h)$ of size V, we can construct an $M_{3d}(S, T)$ of the same size such that $(t_{m,n}, t_{u,v}) \in S$ if $(t_{m,n}, T_{u,v}) \in S_h$ where $m \neq u, m,u = 1,2, \ldots, 6$ and $n,v = 1,2, \ldots, V$. Similarly, there exists the bijection $f': T_h \rightarrow T$ such that $f(t_{m,n}) = t_{m,n}$ and $(t_{m,n}, t_{u,v}) \in S_h$ and only if $(f(t_{m,n}), f(t_{u,v})) = (t_{m,n}, t_{u,v}) \in S$. Therefore, M_{3d} and M_h are isomorphic. □

By theorems 1 and 2, the design problem for the 3-D switch block is equivalent to that for the six-sided switch

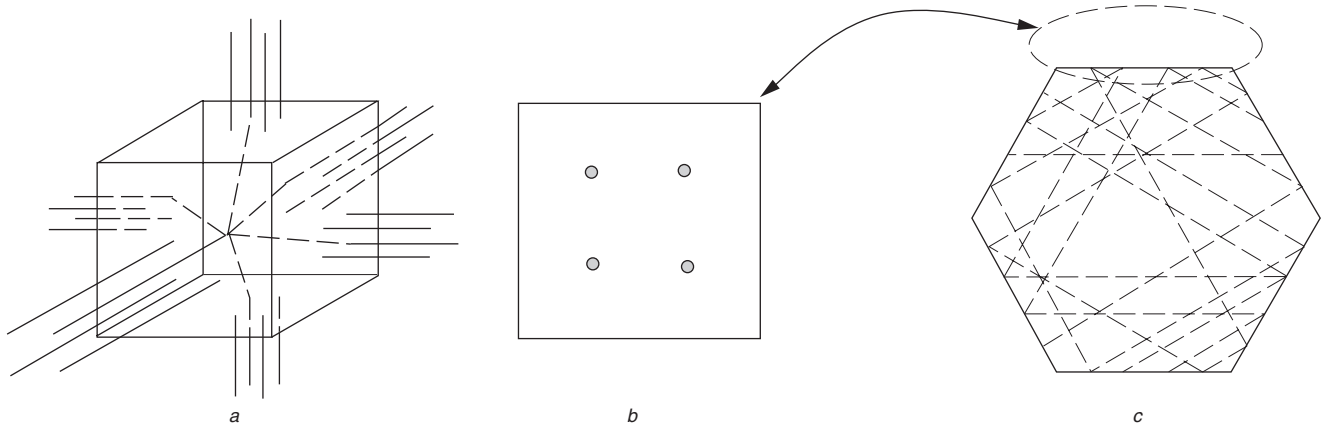

Fig. 3 *3-D switch block and corresponding six-sided switch block*
a Model of 3-D switch block
b One face of 3-D switch block and its terminals
c Corresponding six-sided switch block.

block. Therefore, we shall focus on the six-sided switch block in the rest of the paper. We can classify all connections passing through a switch block into a number of categories. For an HSB, connections can be of 15 types. See Fig. 4 for the type definition.

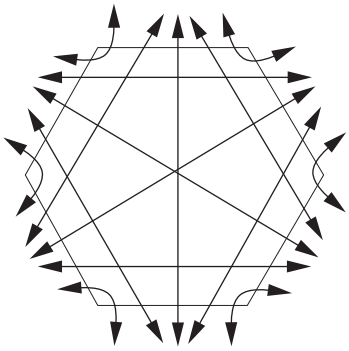

Fig. 4 *Fifteen types of connection in an HSB*

A routing requirement vector (RRV) $\boldsymbol{n}$ for an HSB is a 15-tuple ($n_{1,2}$, …, $n_{1,6}$, $n_{2,3}$, …, $n_{2,6}$, $n_{3,4}$, …, $n_{3,6}$, $n_{4,5}$, $n_{4,6}$, $n_{5,6}$), where $n_{i,j}$ is the number of type-(i, j) connections required to be routed through an HSB, $0 \leq n_{i,j} \leq V$, i, $j = 1,2, \ldots, 6$, $i \neq j$. An RRV $\boldsymbol{n}$ is said to be routable on an HSB M_h if there exists a routing for $\boldsymbol{n}$ on M_h.

The routing capacity of a switch block M is referred to as the number of distinct routable vectors on M; that is, the routing capacity of M is the cardinality $|\{\boldsymbol{n}|\boldsymbol{n}$ is routable on $M\}|$. A switch block M with V terminals on each side is called 'universal' if every set of nets satisfying the dimension constraint (i.e. the number of nets on each side of M is at most V) is simultaneously routable through M. We have the following definition.

Definition 2: An HSB M_h of size V is called universal if the following set of inequalities is the necessary and sufficient conditions for an RRV $\boldsymbol{n} = (n_{1,2}, \ldots, n_{1,6}, n_{2,3}, \ldots, n_{2,6}, n_{3,4}, \ldots, n_{3,6}, n_{4,5}, n_{4,6}, n_{5,6})$ to be routable on M_h:

$$n_{1,2} + n_{1,3} + n_{1,4} + n_{1,5} + n_{1,6} \leq V \quad (1)$$

$$n_{1,2} + n_{2,3} + n_{2,4} + n_{2,5} + n_{2,6} \leq V \quad (2)$$

$$n_{1,3} + n_{2,3} + n_{3,4} + n_{3,5} + n_{3,6} \leq V \quad (3)$$

$$n_{1,4} + n_{2,4} + n_{3,4} + n_{4,5} + n_{4,6} \leq V \quad (4)$$

$$n_{1,5} + n_{2,5} + n_{3,5} + n_{4,5} + n_{5,6} \leq V \quad (5)$$

$$n_{1,6} + n_{2,6} + n_{3,6} + n_{4,6} + n_{5,6} \leq V \quad (6)$$

We refer to the dimension constraint as the set of inequalities which characterises a six-sided universal switch block of size V. Therefore, the dimension constraint for an HSB is the set of (1)–(6) listed in definition 2. Note that the number of nets routed through each side of a switch block cannot exceed V; therefore, a universal switch block has the maximum routing capacity.

3 Universal switch blocks

In this Section, we present an algorithm for constructing symmetric HSBs and it is proved that symmetric HSBs are universal. The symmetric HSB of size V has only $15V$ switches. We prove that no HSB with less than $15V$ switches can be universal. Based on isomorphism operations (theorem 1), we can identify a whole class of universal switch blocks.

3.1 Symmetric switch blocks

Algorithm Symmetric_Switch_Block, shown in Fig. 5, constructs a six-sided switch block M_h of size V. We refer to the topology of the switch block constructed by the algorithm as the 'symmetric topology' and the switch block

Algorithm: Symmetric_Switch_Block(V)
Input: V size of the hexagonal switch block.
Output: $M_h(T_h, S_h)$ the hexagonal switch block of size V;
T_h: set of terminals; S_h: set of switches.
/* See Fig. 3*c* for the terminal labeling. */

1 $T_h \leftarrow t_{i,j}, \quad \forall i = 1,2,\ldots,6, \quad \forall j = 1,2,\ldots,V;$
2 $S_h \leftarrow \emptyset;$
3 **for** $k = 1$ **to** $\lfloor \frac{V}{2} \rfloor$ **do**
4 **for** $i = 1$ **to** 6 **do**
5 **for** $j = 1$ **to** 6 **do**
6 $S_h \leftarrow S_h \cup \{(t_{i,k}, t_{j,V-k+1})\}, i \neq j;$
7 **if** V is odd
8 **for** $i = 1$ **to** 6 **do**
9 **for** $j = 1$ **to** 6 **do**
10 $S_h \leftarrow S_h \cup \{(t_{i,\lceil \frac{V}{2} \rceil}, t_{j,\lceil \frac{V}{2} \rceil})\}, i \neq j;$
11 **Output** $M_h(T_h, S_h)$.

Fig. 5 *Algorithm for constructing a six-sided symmetric switch block of size V*

as the 'symmetric switch block'. Figure 6 shows two examples of symmetric switch blocks. For a symmetric switch block, it has the flexibility (F_S) of 5; thus, the total number of switches in the symmetric switch block size V is

$$\frac{6 \times V \times F_s}{2} = 3 \times V \times F_s = 15V$$

For a symmetric switch block with an even V terminals on each side, it can be partitioned into $V/2$ sub-blocks of size two; and for an odd V, it can be partitioned into $\lfloor V/2 \rfloor$ sub-blocks of size two and one sub-block of size one. Thus, we have the following property. A symmetric switch block of size V can be partitioned into $\lfloor V/2 \rfloor$ symmetric sub-blocks of size two and (V mod 2) symmetric sub-block of size one. (We call this property the decomposition property.)

Note that these sub-blocks are not interacting with each other; thus, each sub-block can be considered independently.

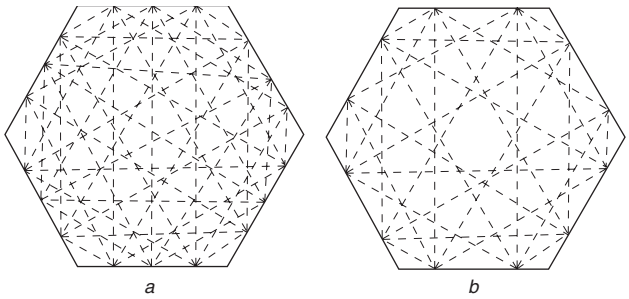

Fig. 6 *Two symmetric hexagonal switch blocks*
a Symmetric HSB of $V = 3$
b Symmetric HSB of $V = 2$

3.2 Proof of universality

In this subsection, it is proved that the symmetric switch blocks constructed by algorithm Symmetric_Switch_Block are universal. To show that the symmetric switch blocks are universal, we first prove that the symmetric HSBs of size two are universal.

Lemma 1: The HSB M_h of size two constructed by algorithm Symmetric_Switch_Block is universal.

Proof: By definition 2, we must prove that $\boldsymbol{n}$ is routable on M_h if and only if the following inequalities are simultaneously satisfied:

$$n_{1,2} + n_{1,3} + n_{1,4} + n_{1,5} + n_{1,6} \leq 2 \quad (7)$$

$$n_{1,2} + n_{2,3} + n_{2,4} + n_{2,5} + n_{2,6} \leq 2 \quad (8)$$

$$n_{1,3} + n_{2,3} + n_{3,4} + n_{3,5} + n_{3,6} \leq 2 \quad (9)$$

$$n_{1,4} + n_{2,4} + n_{3,4} + n_{4,5} + n_{4,6} \leq 2 \quad (10)$$

$$n_{1,5} + n_{2,5} + n_{3,5} + n_{4,5} + n_{5,6} \leq 2 \quad (11)$$

$$n_{1,6} + n_{2,6} + n_{3,6} + n_{4,6} + n_{5,6} \leq 2 \quad (12)$$

(If) It is not difficult to identify all of the RRVs satisfying (7)–(12). (In fact, there are 2578 such RRVs.) We verify the RRVs and conclude that they can all successfully be routed on the HSB of size two constructed by algorithm Symmetric_Switch_Block. In fact, based on the work in [11], we need to check only the RRVs in the corresponding dominating set (see [11] for the definition of dominating sets). The key insight is that the two terminals, say terminals b and c, which connect to a terminal, say a, do not share any switch (Fig. 7*b*); thus the connections associated with them are non-interacting, except those associated with a.

(Only if) For an HSB M_h of size two, the total number of connections routed through each side of M_h cannot exceed two. Hence, if $\boldsymbol{n}$ is routable on M_h, the six inequalities must be satisfied. □

Let U_V denote the set of RRVs which satisfy the dimension constraint for an HSB of size V. An RRV$\boldsymbol{\gamma} \in U_V$ is called a maximal RRV (MRRV) if there exists no other RRV in U_V that dominates $\boldsymbol{\gamma}$. In the following, we show that all RRVs in U_V can be decomposed into U_{V-2} and U_2. Similarly, we need to check only the RRVs in the corresponding dominating set (i.e. MRRVs). We have the following lemma.

Lemma 2: When an MRRV $\boldsymbol{\gamma} \in U_V$ is routed on an HSB, all unused terminals, if any, must be on the same side and the number of unused terminals $\phi_{unused} = 2c$, $0 \leq c \leq \lfloor V/2 \rfloor$, $c \in Z$.

Proof: If there are two unused terminals on different sides (say sides i and j, $i<j$), we can increase $\gamma_{i,j}$ by one without violating the dimension constraint, implying that $\boldsymbol{\gamma}$ is not maximal: a contradiction. Hence, all unused terminals, if any, must be on the same side. Note that the total number of terminals is $\phi_{total} = 6V$, an even number. Assume that there are ϕ_{used} used terminals. Obviously, ϕ_{used} is even since each switch is incident on two terminals. Also, $\phi_{unused} = \phi_{total} - \phi_{used} \leq V$ since all unused terminals, if any, must be on the same side. Since ϕ_{total} and ϕ_{used} are even numbers and $0 \leq \phi_{unused} \leq V$, $\phi_{unused} = \phi_{total} - \phi_{used} = 2c$, $0 \leq c \leq \lfloor V/2 \rfloor$, $c \in Z$. □

Consider the MRRVs in U_V. By lemma 2, we can classify the MRRVs into two types. One is that all terminals are used (i.e. $\phi_{unused} = 0$), and we call an MRRV of this type a 'complete MRRV'. The other is that an even number of terminals on the same side are unused (i.e. $\phi_{unused} = 2c$, $c \in Z^+$), and we call an MRRV of this type a 'degenerate complete MRRV'.

To show that an MRRV in U_V can be decomposed into U_{V-2} and U_2, we first construct a multiple graph and a weighted graph for the MRRV as follows: for any MRRV we construct a multiple graph $G_m(V_m, E_m)$, where $V_m = \{v_1, v_2 \ldots, v_6\}$. If $n_{i,j} = 1$, construct an edge between v_i and v_j with weight 1; if $n_{i,j} \geq 2$, construct two edges between v_i, and v_j with total weights equal to $n_{i,j}$. (We call the two edges a 'multi-edge'.) We induce a weighted graph $G_w(V_w, E_w)$ from $G_m(V_m, E_m)$ by substituting a weighted edge for a multi-edge. Figures 8*b* and 8*c* show a multiple graph G_{m1} for

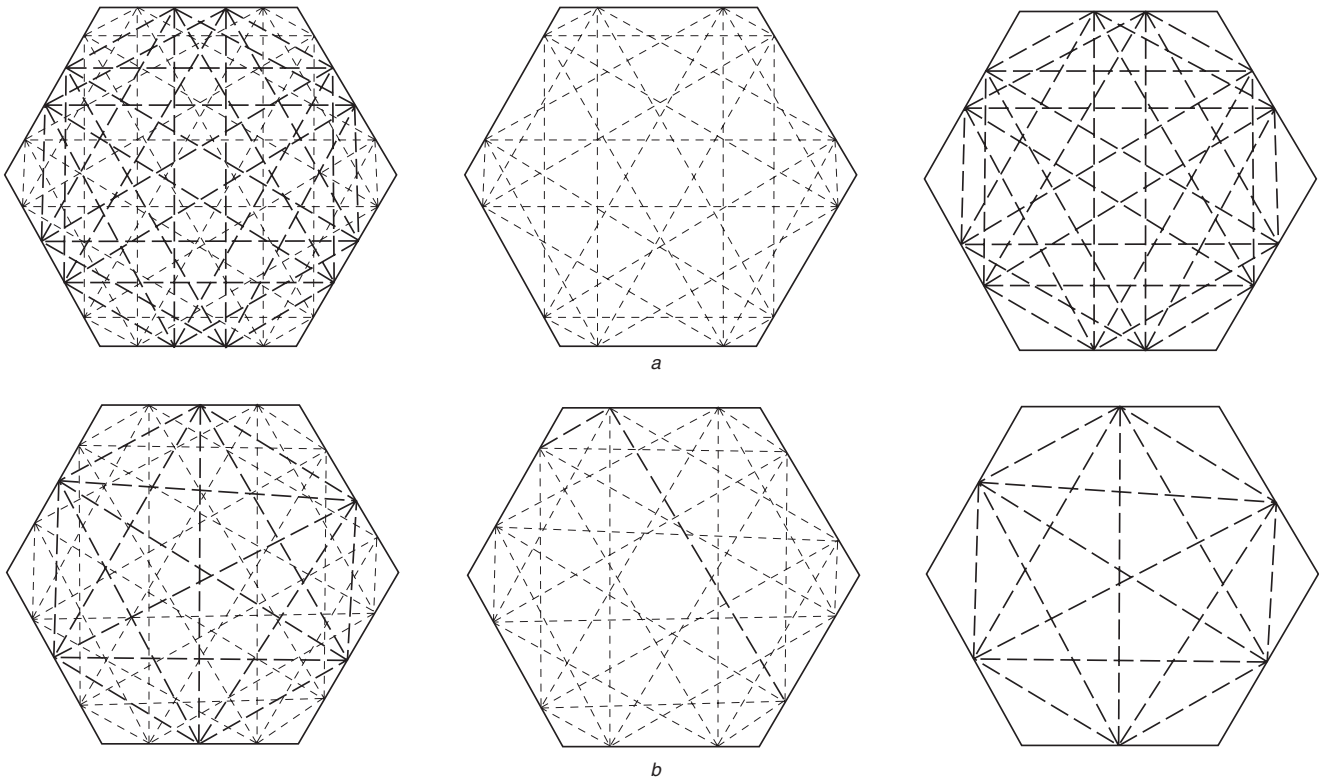

Fig. 7 *Two symmetric HSBs and their sub-blocks*
a Decomposition of symmetric HSB of $V = 4$
b Decomposition of symmetric HSB of $V = 3$

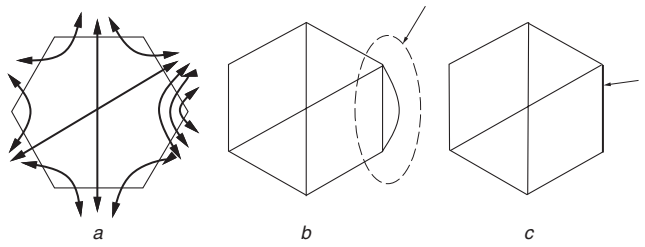

Fig. 8 *Routing instance and corresponding multiple and weighted graphs*
a Routing instance $n = (1, 0, 1, 0, 1, 1, 0, 1, 0, 1, 0, 0, 1, 0, 3)$
b Multiple graph G_{m_1} associated with RRV $\boldsymbol{n}$
c Weighted graph G_{w_1} of *b*

$\boldsymbol{n} = (1, 0, 1, 0, 1, 1, 0, 1, 0, 1, 0, 0, 1, 0, 3)$ and its corresponding weighted graph G_{w1}, respectively. In G_{m1}, there are two edges between v_5 and v_6 because $n_{5,6} = 3$; thus, we introduce the weighted edge (v_5, v_6) in G_{w1}. In a weighted graph $G_w(V_w, E_w)$, a vertex $v \in V_w$ represents one side of an HSB, an edge $e \in E_h$ represents a type of connection between two sides of the HSB, and *weight*(e) denotes the number of connections of the type associated with e.

Let C_k denote a connected component of k vertices in G_w. We have the following lemma.

Lemma 3: For a weighted graph G_w associated with a complete MRRV, there exists no isolated vertex in G_w and for $k \geq 3$, C_k contains no degree-one vertex.

Proof: There exists no isolated vertex in G_w, since the total connections associated with a complete MRRV for a side of HSB must be equal to V. Suppose there exists a $G_w(V_w, E_W)$ (associated with a complete MRRV) for an HSB of size V with a connected component C_k and, for $k \geq 3$, C_k contains a degree-one vertex v_i. Let v_i connect to a vertex v_j by an edge $e_{i,j} = (v_i, v_j)$. Since G_w is associated with a complete MRRV and v_i is a degree-one vertex. The total number of connections associated with v_i, weight $(e_{i,j})$, is equal to the dimension constraint V. Further, the total number of connections associated with a vertex can be V at most; since weight $(e_{i,j}) = V$, v_j only connects to v_i. Hence, the degree of v_j must also equal one, and v_i and v_j form a C_2. A contradiction. Therefore, there exists no C_k $(k \geq 3)$ with degree-one vertex in G_w. □

A hamiltonian subcycle of a multiple graph $G_m(V_m, E_m)$ is a simple cycle that contains a subset of vertices in V_m. Two hamiltonian subcycles in a multiple graph are called 'independent' if no vertex is shared by two subcycles. A multiple graph $G_m(V_m, E_m)$ is said to be sub-hamiltonian if it contains a set of independent hamiltonian subcycles and all vertices in V_m are on the subcycles; otherwise, it is non-sub-hamiltonian. Also, we call a weighted graph sub-hamiltonian if its associated multiple graph is sub-hamiltonian. For three RRVs $\boldsymbol{u}$, $\boldsymbol{v}$, and $\boldsymbol{x}$, we say $\boldsymbol{u}$ is a sub-RRV of $\boldsymbol{v}$ if there exists an $\boldsymbol{x}$ such that $\boldsymbol{v} = \boldsymbol{u} + \boldsymbol{x}$. Let $\boldsymbol{n}_i$ be a sub-RRV of $\boldsymbol{n}$. We define Ω and Ω' as follows:

$$\Omega = \{\boldsymbol{n} | \boldsymbol{n} \in U_V\}$$
$$\Omega' = \{\boldsymbol{n} | \boldsymbol{n} = \boldsymbol{n}_1 + \boldsymbol{n}_2,\ \boldsymbol{n}_1 \in U_{V-2} \text{and}\ \boldsymbol{n}_2 \in U_2\},\ \text{where } V \geq 2$$

We have the following lemmas.

Lemma 4: If the multiple graph of an MRRV $\boldsymbol{n}$ is sub-hamiltonian, $\boldsymbol{n}$ has a complete sub-RRV $\boldsymbol{n}_2 \in U_2$.

Proof: Let G_m be a sub-hamiltonian graph associated with an MRRV $\boldsymbol{n}$. G_m has a set of independent hamiltonian subcycles $S = \{c_1, c_2, \ldots, c_k\}$ that covers all vertices in G_m. We can choose a sub-RRV $\boldsymbol{n}_2$ of $\boldsymbol{n}$ as follows. For any cycle $c_i \in S, c_i = < v_{i_1}, v_{i_2}, \ldots, v_{i_k}, v_{i_j} >$. If $k = 2$, let $n_{2,(v_{i_1}, v_{i_2})} = 2$; otherwise, let $n_{2,(v_{i_1}, v_{i_2})} = n_{2,(v_{i_2}, v_{i_3})} = \ldots = n_{2,(v_{i_k}, v_{i_1})} = 1$. We traverse G_m based on S. S includes independent hamiltonian subcycles which contain all vertices in G_m. All vertices will be visited one time. A vertex in G_m corresponds to one side of an HSB associated with $\boldsymbol{n}$. Every vertex contributes two degrees in S. Thus, the number of connections with one side of the HSB is equal to 2. $\boldsymbol{n}_2$ satisfies the following inequalities:

$$n_{2,(1,2)} + n_{2,(1,3)} + n_{2,(1,4)} + n_{2,(1,5)} + n_{2,(1,6)} = 2$$
$$n_{2,(1,2)} + n_{2,(2,3)} + n_{2,(2,4)} + n_{2,(2,5)} + n_{2,(2,6)} = 2$$
$$n_{2,(1,3)} + n_{2,(2,3)} + n_{2,(3,4)} + n_{2,(3,5)} + n_{2,(3,6)} = 2$$
$$n_{2,(1,4)} + n_{2,(2,4)} + n_{2,(3,4)} + n_{2,(4,5)} + n_{2,(4,6)} = 2$$
$$n_{2,(1,5)} + n_{2,(2,5)} + n_{2,(3,5)} + n_{2,(4,5)} + n_{2,(5,6)} = 2$$
$$n_{2,(1,6)} + n_{2,(2,6)} + n_{2,(3,6)} + n_{2,(4,6)} + n_{2,(5,6)} = 2$$

Thus $\boldsymbol{n}_2 \in U_2$ and it is a complete MRRV. □

Lemma 5: (RRV decomposition property) $\Omega = \Omega'$.

Proof: First, we show that $\Omega' \subseteq \Omega$. By definition 2, an RRV $\boldsymbol{n}_1 \in U_{V-2}$ if and only if the following inequalities are simultaneously satisfied:

$$n_{1,(1,2)} + n_{1,(1,3)} + n_{1,(1,4)} + n_{1,(1,5)} + n_{1,(1,6)} \leq V - 2 \quad (13)$$
$$n_{1,(1,2)} + n_{1,(2,3)} + n_{1,(2,4)} + n_{1,(2,5)} + n_{1,(2,6)} \leq V - 2 \quad (14)$$
$$n_{1,(1,3)} + n_{1,(2,3)} + n_{1,(3,4)} + n_{1,(3,5)} + n_{1,(3,6)} \leq V - 2 \quad (15)$$
$$n_{1,(1,4)} + n_{1,(2,4)} + n_{1,(3,4)} + n_{1,(4,5)} + n_{1,(4,6)} \leq V - 2 \quad (16)$$
$$n_{1,(1,5)} + n_{1,(2,5)} + n_{1,(3,5)} + n_{1,(4,5)} + n_{1,(5,6)} \leq V - 2 \quad (17)$$
$$n_{1,(1,6)} + n_{1,(2,6)} + n_{1,(3,6)} + n_{1,(4,6)} + n_{1,(5,6)} \leq V - 2 \quad (18)$$

and for an RRV $\boldsymbol{n}_2 \in U_2$, the following inequalities are simultaneously satisfied:

$$n_{2,(1,2)} + n_{2,(1,3)} + n_{2,(1,4)} + n_{2,(1,5)} + n_{2,(1,6)} \leq 2 \quad (19)$$
$$n_{2,(1,2)} + n_{2,(2,3)} + n_{2,(2,4)} + n_{2,(2,5)} + n_{2,(2,6)} \leq 2 \quad (20)$$
$$n_{2,(1,3)} + n_{2,(2,3)} + n_{2,(3,4)} + n_{2,(3,5)} + n_{2,(3,6)} \leq 2 \quad (21)$$
$$n_{2,(1,4)} + n_{2,(2,4)} + n_{2,(3,4)} + n_{2,(4,5)} + n_{2,(4,6)} \leq 2 \quad (22)$$
$$n_{2,(1,5)} + n_{2,(2,5)} + n_{2,(3,5)} + n_{2,(4,5)} + n_{2,(5,6)} \leq 2 \quad (23)$$
$$n_{2,(1,6)} + n_{2,(2,6)} + n_{2,(3,6)} + n_{2,(4,6)} + n_{2,(5,6)} \leq 2 \quad (24)$$

Let $\boldsymbol{n} = \boldsymbol{n}_1 + \boldsymbol{n}_2$, $n_{1,2} = n_{1,(1,2)} + n_{2,(1,2)}$, $n_{1,3} = n_{1,(1,3)} + n_{2,(1,3)}$, …, $n_{5,6} = n_{1,(5,6)} + n_{2,(5,6)}$. Combining (13) and (19), (14) and (20), (15) and (21), (16) and (22), (17) and (23), and (18) and (24), we obtain (25)–(30)

$$n_{1,2} + n_{1,3} + n_{1,4} + n_{1,5} + n_{1,6} \leq V \quad (25)$$
$$n_{1,2} + n_{2,3} + n_{2,4} + n_{2,5} + n_{2,6} \leq V \quad (26)$$
$$n_{1,3} + n_{2,3} + n_{3,4} + n_{3,5} + n_{3,6} \leq V \quad (27)$$
$$n_{1,4} + n_{2,4} + n_{3,4} + n_{4,5} + n_{4,6} \leq V \quad (28)$$
$$n_{1,5} + n_{2,5} + n_{3,5} + n_{4,5} + n_{5,6} \leq V \quad (29)$$
$$n_{1,6} + n_{2,6} + n_{3,6} + n_{4,6} + n_{5,6} \leq V \quad (30)$$

Thus, $\boldsymbol{n} \in U_V$, and we have $\Omega' \subseteq \Omega$.

Next, we show that $\Omega \subseteq \Omega'$. It suffices to show that each MRRV $\boldsymbol{n} \in \Omega$ is in Ω'. By lemma 2, all unused terminals for routing an MRRV on an HSB are on the same side, and the number of unused terminals is even. Without loss of

generality, assume that all unused terminals, if any, are on side 1 and the number of unused terminals is equal to c_1, $0 \le c_1 \le \lfloor V/2 \rfloor$. By definition 2, an MRRV $\boldsymbol{n} \in \Omega$ if and only if the following equalities are simultaneously satisfied:

$$n_{1,2} + n_{1,3} + n_{1,4} + n_{1,5} + n_{1,6} = V - 2c_1 \quad (31)$$

$$n_{1,2} + n_{2,3} + n_{2,4} + n_{2,5} + n_{2,6} = V \quad (32)$$

$$n_{1,3} + n_{2,3} + n_{3,4} + n_{3,5} + n_{3,6} = V \quad (33)$$

$$n_{1,4} + n_{2,4} + n_{3,4} + n_{4,5} + n_{4,6} = V \quad (34)$$

$$n_{1,5} + n_{2,5} + n_{3,5} + n_{4,5} + n_{5,6} = V \quad (35)$$

$$n_{1,6} + n_{2,6} + n_{3,6} + n_{4,6} + n_{5,6} = V \quad (36)$$

Algorithm RRV-Decomposition listed in Fig. 9 shows a method to decompose $\boldsymbol{n} \in Uv$ into $\boldsymbol{n}_1$ and $\boldsymbol{n}_2$, where $\boldsymbol{n}_1 \in U_{V-2}$ and $\boldsymbol{n}_2 \in U_2$. It derives $\boldsymbol{n}$ based on the two cases: (i) $\boldsymbol{n}$ is a complete MRRV, and (ii) $\boldsymbol{n}$ is a degenerate complete MRRV.

Algorithm: RRV-Decomposition ($\boldsymbol{n}$)
Input: $\boldsymbol{n}$ An MRRV in U_V.
Output: $\boldsymbol{n}_1, \boldsymbol{n}_2$—MRRVs such that $\boldsymbol{n} = \boldsymbol{n}_1 + \boldsymbol{n}_2$, $\boldsymbol{n}_1 \in U_{V-2}$ and $\boldsymbol{n}_2 \in U_2$.
/* Lines 1–7 construct a multiple graph $G_m(V_m, E_m)$*/
/* $\uplus$ denotes the special 'union' operation by keeping duplicate elements; e.g., $\{a, b\} \uplus \{a, c\} = \{a, a, b, c\}$.*/
1 $V_m = \{v_1, v_2, \ldots, v_6\}$;
2 $C_1 = \left(V - \sum_{i=1}^{6} n_{1,i}\right)/2$;
3 **if** $c_1 \neq 0$ **then** /* degenerate complete MRRV */
4 let $n_{2,(1,2)} \leftarrow n_{2,(1,3)} \leftarrow \ldots \leftarrow n_{2,(1,6)} \leftarrow 0$;
5 $V_m \leftarrow V_m - \{v_1\}$;
6 $E_m = \{(v_i, v_j) | n_{i,j} \neq 0\}$;
7 $E_m = E_m \uplus \{(v_i, v_j) | n_{i,j} \geq 2\}$;
8 $H \leftarrow$ all hamiltonian subcycles in $G_m(V_m, E_m)$;
9 $S \leftarrow$ set of independent hamiltonian subcycles which contain all V_m;
10 for each cycle $< v_{i_1}, v_{i_2}, \ldots, v_{i_k}, v_{i_1} > \in S$
11 **if** $k = 2$ **then**
12 $n_{2,(v_{i_1}, v_{i_2})} \leftarrow 2$;
13 **else**
14 $n_{2,(v_{i_1}, v_{i_2})} \leftarrow n_{2,(v_{i_1}, v_{i_2})} \leftarrow \ldots \leftarrow n_{2,(v_{i_k}, v_{i_1})} \leftarrow 1$;
15 $\boldsymbol{n}_1 \leftarrow \boldsymbol{n} - \boldsymbol{n}_2$;
16 output $\boldsymbol{n}_1$, $\boldsymbol{n}_2$.

Fig. 9 *Algorithm for RRV decomposition, assuming that all unused terminals, if any, are on side 1*

We first consider the case where $\boldsymbol{n}$ is a complete MRRV. Let G_w be a weighted graph of $\boldsymbol{n}$ and C_i be a connected component with i vertices in G_w. By lemma 3, there exists no isolated vertex or any C_k, $k \geq 3$, with a degree-one vertex in G_w. Thus, the number of vertices in C_k could only be 2, 3, 4, or 6.

We classify all weighted graphs for complete MRRVs into four categories α, β, γ, and δ, listed in Table 1. (Note that the weighted graphs, except C_2, contain no isolated vertex or degree-one vertex.) Categories α, β, γ, and δ represent the cases where G_w consists of three C_2s, one C_2 and one C_4, two C_3s, and one C_6, respectively. The total

Table 1: Number of weighted graphs for complete *MRRVs*

Category	Number of weighted graphs	Number of illegal graphs	Number of legal graphs
α	1	0	1
β	3	0	3
γ	1	0	1
δ	52	12	40
Total	56	12	44

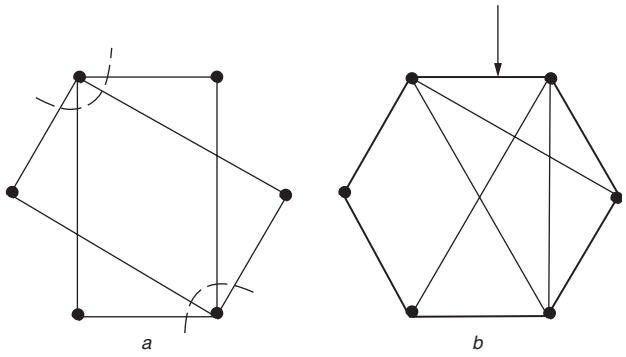

Fig. 10 *Weighted graphs for two complete MRRVs*
a Illegal weighted graph; its total weights is equal to $2V$
b Legal weighted graph with a hamiltonian subcycle $C_1 = <v_1, v_2, \ldots, v_6, v_1>$

number of weighted graphs with complete *MRRVs* are 56, and twelve of them are illegal, which can be verified by checking if the total edge weights of the graphs equal $3V$. (Note that all $6V$ terminals are used for a complete MRRV, and a connection is incident on two terminals.) For example, Fig. 10*a* shows an infeasible weighted graph G_w. Consider vertices v_1 and v_4. The total number of connections associated with v_1 must be equal to the dimension constraint V (i.e. all terminals on each side of the HSB are used); therefore, $|e_1| + |e_2| + |e_3| + |e_4| = V$. Similarly, there are V connections associated with v_4, and thus $|e_5| + |e_6| + |e_7| + |e_8| = V$. Therefore, the total number of connections associated with G_w is equal to $2V$. By (31)–(36), however, the total number of connections associated with a complete MRRV must be equal to $3V$. Therefore, G_w is illegal. We have the facts that the other 44 weighted graphs are sub-hamiltons. (Table 1 summarises the number of legal and illegal weighted graphs for complete MRRVs.) Figure 10*b* shows a sub-hamilton weighted graph associated with a complete MRRV. It has a hamiltonian subcycle $c_1 = <v_1, v_2, \ldots, v_6, v_1>$ that contains all vertices. By lemma 4, $\boldsymbol{n}$ has a complete sub-RRV $\boldsymbol{n}_2 \in U_2$. In other words, $\boldsymbol{n}_2$ satisfies the following equalities:

$$n_{2,(1,2)} + n_{2,(1,3)} + n_{2,(1,4)} + n_{2,(1,5)} + n_{2,(1,6)} = 2 \quad (37)$$

$$n_{2,(1,2)} + n_{2,(2,3)} + n_{2,(2,4)} + n_{2,(2,5)} + n_{2,(2,6)} = 2 \quad (38)$$

$$n_{2,(1,3)} + n_{2,(2,3)} + n_{2,(3,4)} + n_{2,(3,5)} + n_{2,(3,6)} = 2 \quad (39)$$

$$n_{2,(1,4)} + n_{2,(2,4)} + n_{2,(3,4)} + n_{2,(4,5)} + n_{2,(4,6)} = 2 \quad (40)$$

$$n_{2,(1,5)} + n_{2,(2,5)} + n_{2,(3,5)} + n_{2,(4,5)} + n_{2,(5,6)} = 2 \quad (41)$$

$$n_{2,(1,6)} + n_{2,(2,6)} + n_{2,(3,6)} + n_{2,(4,6)} + n_{2,(5,6)} = 2 \quad (42)$$

Let $\boldsymbol{n}_1 = \boldsymbol{n} - \boldsymbol{n}_2$. Since $\boldsymbol{n}$ is a complete MRRV, the constant c_1 in (31) equals zero. By (31)–(36) and (13)–(18), we have the following equalities:

$$n_{2(1,2)} + n_{2,(1,3)} + n_{2,(1,4)} + n_{2,(1,5)} + n_{2,(1,6)} = V - 2 \quad (43)$$

$$n_{2,(1,2)} + n_{2,(2,3)} + n_{2,(2,4)} + n_{2,(2,5)} + n_{2,(2,6)} = V - 2 \quad (44)$$

$$n_{2,(1,3)} + n_{2,(2,3)} + n_{2,(3,4)} + n_{2,(3,5)} + n_{2,(3,6)} = V - 2 \quad (45)$$

$$n_{2,(1,4)} + n_{2,(2,4)} + n_{2,(3,4)} + n_{2,(4,5)} + n_{2,(4,6)} = V - 2 \quad (46)$$

$$n_{2,(1,5)} + n_{2,(2,5)} + n_{2,(3,5)} + n_{2,(4,5)} + n_{2,(5,6)} = V - 2 \quad (47)$$

$$n_{2,(1,6)} + n_{2,(2,6)} + n_{2,(3,6)} + n_{2,(4,6)} + n_{2,(5,6)} = V - 2 \quad (48)$$

Obviously, $\boldsymbol{n}_1 \in U_{V-2}$. Applying similar techniques, we can show that all multiple graphs associated with degenerate complete MRRVs are sub-hamiltons. Thus, $\Omega \subseteq \Omega'$. Based on the above discussion, we have $\Omega' = \Omega$.

Two sub-blocks are said to be 'independent' if they do not share any terminals. By lemma 5, independent switch sub-blocks can be considered individually and merged to form a larger switch block, and the routable RRVs for the merged switch block are identical to those given by applying vector addition operations on the routable RRVs for the independent switch sub-blocks. With the decomposition properties of symmetric switch blocks and RRVs, we can prove the following theorem by using mathematical induction.

Theorem 3: The symmetric switch blocks are universal

Proof: Using definition 2, we shall show that, for an HSB M_h of size V constructed by algorithm Symmetric_Switch_Block, $\boldsymbol{n}$ is routable on M_h if and only if the following inequalities are simultaneously satisfied:

$$n_{1,2} + n_{1,3} + n_{1,4} + n_{1,5} + n_{1,6} \leq V$$

$$n_{1,2} + n_{2,3} + n_{2,4} + n_{2,5} + n_{2,6} \leq V$$

$$n_{1,3} + n_{2,3} + n_{3,4} + n_{3,5} + n_{3,6} \leq V$$

$$n_{1,4} + n_{2,4} + n_{3,4} + n_{4,5} + n_{4,6} \leq V$$

$$n_{1,5} + n_{2,5} + n_{3,5} + n_{4,5} + n_{5,6} \leq V$$

$$n_{1,6} + n_{2,6} + n_{3,6} + n_{4,6} + n_{5,6} \leq V$$

For the HSBs constructed by the algorithm, we have the following key observations (Fig. 7). For an HSB of an even V, we can partition it into $V/2$ non-interacting sub-blocks (shown in Fig. 7*a*); each sub-block has the same topology as that of β shown in Fig. 7*a*. For an HSB of an odd V, we can partition it into $[V/2]$ non-interacting sub-blocks, with each of the $[V/2]$ sub-blocks identical to β and one sub-block with a clique topology formed by the six terminals from the middle of each side (Fig. 7*b*). Because terminals in different sub-blocks are non-interacting, each sub-block can be considered independently (lemma 5). Therefore, each symmetric HSB consists of $[V/2]$ independent universal switch sub-blocks of size two, and additional one of size one if V is odd. Further, by lemma 1, an HSB of size two constructed by algorithm Symmetric_Switch_Block is universal. (If) For an even V, by lemma 5, we can decompose a vector $\boldsymbol{n} = (n_{1,2}, n_{1,3}, \ldots, n_{1,6}, n_{2,3}, \ldots, n_{2,6}, n_{3,4}, \ldots, n_{3,6}, n_{4,5}, n_{4,6}, n_{5,6})$ into V/2 sub-RRVs $n_i = (n_{i,(1,2)}, n_{i,(1,3)}, \ldots, n_{i,(1,6)}, n_{i,(2,3)}, \ldots, n_{i,(2,6)}, n_{i,(3,4)}, \ldots, n_{i,(3,6)}, n_{i,(4,5)}, n_{i,(4,6)}, n_{i,(5,6)})$, where $i = 1,2, \ldots, V/2$, such that each sub-RRV satisfies the following set of inequalities:

$$n_{i,(1,2)} + n_{i,(1,3)} + n_{i,(1,4)} + n_{i,(1,5)} + n_{i,(1,6)} \leq 2 \quad (49)$$

$$n_{i,(1,2)} + n_{i,(2,3)} + n_{i,(2,4)} + n_{i,(2,5)} + n_{i,(2,6)} \leq 2 \quad (50)$$

$$n_{i,(1,3)} + n_{i,(2,3)} + n_{i,(3,4)} + n_{i,(3,5)} + n_{i,(3,6)} \leq 2 \quad (51)$$

$$n_{i,(1,4)} + n_{i,(2,4)} + n_{i,(3,4)} + n_{i,(4,5)} + n_{i,(4,6)} \leq 2 \quad (52)$$

$$n_{i,(1,5)} + n_{i,(2,5)} + n_{i,(3,5)} + n_{i,(4,5)} + n_{i,(5,6)} \leq 2 \quad (53)$$

$$n_{i,(1,6)} + n_{i,(2,6)} + n_{i,(3,6)} + n_{i,(4,6)} + n_{i,(5,6)} \leq 2 \quad (54)$$

where

$$\boldsymbol{n} = \sum_{i=1}^{V/2} \boldsymbol{n}_i$$

By lemma 1, each RRV $\boldsymbol{n}_i$ satisfying (49)–(54) must be routable on the HSB of size two, and by lemma 5, $\boldsymbol{n}$ is also routable on the symmetric HSB of size V.

For an odd V, by lemma 5, we can decompose a vector $\boldsymbol{n}$ into $[V/2]$ sub-RRVs $\boldsymbol{n}_i$s, where $i = 1,2, \ldots, [V/2]$, such that each of the sub-RRVs $\boldsymbol{n}_i$, $i = 1,2, \ldots, [V/2]$ satisfies the set (49)–(54), and the remaining one $\boldsymbol{n}_{[V/2]}$ satisfies the following set of inequalities:

$$n_{[V/2],(1,2)} + n_{[V/2],(1,3)} + n_{[V/2],(1,4)} + n_{[V/2],(1,5)} + n_{[V/2],(1,6)} \leq 1 \quad (55)$$

$$n_{[V/2],(1,2)} + n_{[V/2],(2,3)} + n_{[V/2],(2,4)} + n_{[V/2],(2,5)} + n_{[V/2],(2,6)} \leq 1 \quad (56)$$

$$n_{[V/2],(1,3)} + n_{[V/2],(2,3)} + n_{[V/2],(3,4)} + n_{[V/2],(3,5)} + n_{[V/2],(3,6)} \leq 1 \quad (57)$$

$$n_{[V/2],(1,4)} + n_{[V/2],(2,4)} + n_{[V/2],(3,4)} + n_{[V/2],(4,5)} + n_{[V/2],(4,6)} \leq 1 \quad (58)$$

$$n_{[V/2],(1,5)} + n_{[V/2],(2,5)} + n_{[V/2],(3,5)} + n_{[V/2],(4,5)} + n_{[V/2],(5,6)} \leq 1 \quad (59)$$

$$n_{[V/2],(1,6)} + n_{[V/2],(2,6)} + n_{[V/2],(3,6)} + n_{[V/2],(4,6)} + n_{[V/2],(5,6)} \leq 1 \quad (60)$$

We have

$$\boldsymbol{n} = \sum_{i=1}^{[V/2]} \boldsymbol{n}_i$$

By lemma 1, each RRV $\boldsymbol{n}_i$ satisfying the set (49)–(54) must be routable on the symmetric HSB of size two. Further, the last RRV is also routable on an HSB of size one (a clique of six terminals). Hence, by lemma 5, $\boldsymbol{n}$ is also routable on the symmetric HSB of size V.

(Only if) For an HSB M_h of size V, the total number of connections routed through each side of M_h, cannot exceed V. Hence, if $\boldsymbol{n}$ is routable on M_h, (1)–(6) must be satisfied. □

Theorem 4: No HSBs with less than 15 V switches can be universal.

Proof: By definition 2, an RRV with only one non-zero component V such as (V, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0), (0, V, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0),…, (0, V, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, V) is routable on a universal HSB. Hence it needs at least V non-interacting switches for each type of connections to construct a universal HSB. Since there are 15 types of connections in an HSB, the smallest number of switches needed to construct a universal HSB is 15 V.

As mentioned in subsection 3.1, the total number of switches used in a six-sided symmetric switch block is 15 V. Thus, the symmetric HSBs are the 'cheapest' universal ones, i.e. it uses the minimum number of switches to construct a universal switch block. Note that the 15 V switches requirement is quite small, compared to a fully connected HSB which has $15V^2$ switches. By theorem 1, any two isomorphic switch blocks have the same routing capacity. Hence, we have following lemma.

Lemma 6: For any two isomorphic switch blocks $M_h(T, S)$ and $M'_h(T', S')$, $M_h(T, S)$ is universal if and only if $M'_h(T', S')$ is universal.

By lemma 6, we can obtain a whole class of universal switch blocks by performing isomorphism operations on a symmetric switch block.

4 Experimental results

To explore the effects of switch-block architectures on routing on a 3-D FPGA, we implemented a maze router in the C language and ran it on a SUN Ultra workstation. We tested the area performance of the router based on the CGE [2] and the SEGA [12] benchmark circuits. A logic-block pin was connected to any of the W tracks in the adjacent routing channel. These circuits were routed on a two-layer 3-D FPGA and randomly assigned the layer for each terminal of a net. The switch-block architectures used were the symmetric switch blocks and clique-based (Xilinx XC4000-like) switch blocks. The quality of a switch block was evaluated by the area performance of the detailed router. Table 2 shows the results. For the results listed in this table, we determined the minimum number of tracks W required for 100% routing completion for each circuit, using the two kinds of switch blocks. Because net ordering often affects the performance of a maze router, the benchmark circuits were routed by using the following three net-ordering schemes to avoid possible biases: (i) net order as given in the original benchmark circuits, (ii) shortest net first (non-decreasing order of net lengths), and (iii) longest net first (non-increasing order of net lengths). Also, since our main goal is to make fair comparisons for switch-block architectures, no optimisation such as rip-and-reroute phase, was incorporated in the maze router (optimisation might bias the comparison).

Results show that, between the two kinds of switch blocks, the symmetric switch blocks usually needed the minimum Ws for 100% routing completion, no matter what net order was used. The results show that the performed symmetric switch blocks improve routability at the chip level. (An average of 6% improvement in area performance was achieved.) Thus also performed experiments to explore the effects of net density on the area performance of switch blocks. Connections were randomly generated on a $15 \times 15 \times 3$ (number of logic blocks in the three layers) 3-D FPGA. For this purpose, it was assumed that the number of pins on each logic blocks was unlimited (so that we could test denser circuits). As shown in Fig. 11, no matter how dense the circuit is (numbers of connections ranging from 400 to 1600), the symmetric switch blocks consistently outperform the clique-based switch blocks. (An average of 10% improvement in the area performance was achieved.)

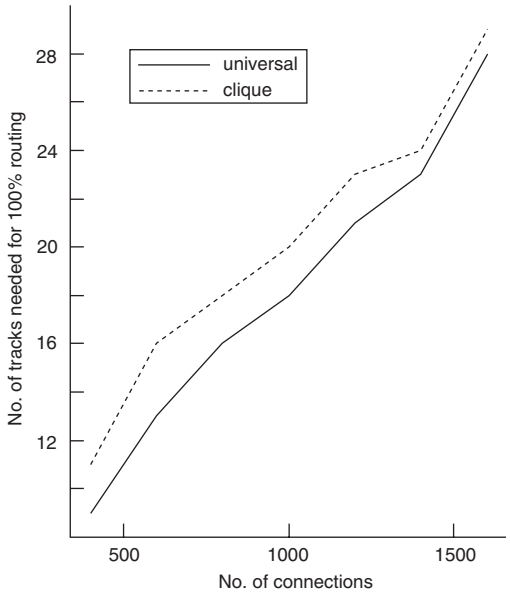

Fig. 11 *Comparison of area performance using the symmetric switch blocks and clique-based switch blocks for different numbers of connections on a $15 \times 15 \times 3$ 3D-FPGA*

5 Concluding remarks

We have proposed a class of the universal switch blocks for three-dimensional FPGAs. Each switch block has $15W$ switches and $F_S = 5$. It has been proved that no switch block with less than $15W$ switches can be universal. The proposed switch blocks have been compared with those of

Table 2: Minimum numbers of tracks needed for detailed-routing completion

Circuit	Number of logic blocks	Number of connections	Number of tracks needed for detailed-routing completion					
			Original order		Shortest net first		Longest net first	
			Symmetric	Clique	Sym.	Cliq.	Sym.	Cliq.
BUSC	$13 \times 12 \times 2$	392	7	9	7	7	8	8
DMA	$18 \times 16 \times 2$	771	9	9	8	8	10	10
BNRE	$22 \times 21 \times 2$	1257	9	9	8	9	10	10
DFSM	$23 \times 22 \times 2$	1422	9	9	8	8	9	9
Z03	$27 \times 26 \times 2$	2135	9	10	8	9	10	10
9symml	$11 \times 10 \times 2$	259	6	6	6	7	7	8
alu2	$15 \times 13 \times 2$	511	7	7	7	8	8	9
alu4	$19 \times 17 \times 2$	851	8	9	9	9	10	11
apex7	$12 \times 10 \times 2$	300	6	7	6	7	8	8
example2	$14 \times 12 \times 2$	444	8	8	8	8	9	10
k2	$22 \times 20 \times 2$	1256	11	11	10	11	12	12
term1	$10 \times 9 \times 2$	202	7	8	6	6	7	8
too_large	$15 \times 14 \times 2$	519	7	9	8	8	9	9
vda	$17 \times 16 \times 2$	722	7	9	8	9	9	10
Total	—	—	109	118	106	112	125	131
Comparison	—	—	1.00	1.08	1.00	1.06	1.00	1.05

Xilinx XC4000-like FPGAs. Experimental results have shown that the proposed universal switch blocks improve routabilty at the chip level.

There are several significant future research directions:

- Exploration of the universal switch blocks of 3-D FPGAs with respect to multi-terminal pins: in this paper, the theoretical analysis is based on two-pin nets. Nevertheless, the benchmark circuits also contain significant numbers of multi-pin nets. The experimental results based on circuits with multi-pin nets conform to the theoretical findings based on two-pin nets. The approach can be extended to the design of universal switch blocks with respect to multi-pin nets. For example, one may first model the types of a specified multi-pin net (say, $C(6, 3) = 20$ types of nets for three-pin nets). After the modelling is established, similar procedures may be applied for further analysis.
- Development of global/detailed routers that can consider the universal switch-block architectures: to develop an FPGA router considering the switch-block architecture, we shall first develop a congestion metric associated with the switch block, and then perform the routing based on congestion control of switch-block density as well as classical channel density.

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