Single-Wire Current-Share Paralleling of Current-Mode Controlled DC Power Supplies

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ABSTRACT

This paper presents a new single-wire autonomous current-share paralleling of current-mode controlled DC power supplies. The proposed control scheme makes use of the nature of fast response of the inner current loop and the share bus injected signal to improve the response of the power system. It reduces the unbalance of current distribution during the transient state and avoids the fault alarm for the current limit. Through the theoretical derivation, the design of the proposed control can be used by the multi-loop control method. A design example of a system of two 400V/48V 20A modules is set up and experimental recordings verify the performance of current sharing.

1. INTRODUCTION

In recent years, due to the rapid advance of computer and communication, the power supplies must provide high current up to hundreds of amperes, and still have high efficiency and reliability. Under such requirements, the multi-module paralleling is usually used and the load current is equally shared. In this way the current stress of the switching devices is reduced and the efficiency and reliability [1] are improved. About the current sharing control, a variety of schemes have been presented [2-10] over the years. The single-wire current-share method [7] is the simplest and most favorable. The configuration is shown in Fig. 1. The share bus carries the average current signal reference for every module. No central control unit is required and only a few operational amplifiers or comparators [10] are added in the modules.

In practical applications, some unnecessary minor alarms occur at the load rapidly changed or one module fails and shuts down. The output currents of the converter modules are not equally distributed during the load transient. The protection circuits limit the output current when they exceed the rated values and an alarm may be raised. To avoid the unfavorable situation, we try to use the current-mode control instead of the conventional voltage-mode control in the modules. The simplified circuit of conventional voltage-mode is shown in Fig. 2(a). The current share error signal is injected into the voltage loop to adjust the voltage command [2-5]. The response of current sharing is bounded by the low bandwidth of voltage loop due to bulk capacitors at the output. In current-mode control, the inner current loop has high bandwidth. It can be used to alleviate the unbalance problem during the transient. By the way, the current sensor is already used to sense the inductor current in current-mode control, it can be also used for current sharing.

The paralleled current-mode control had been investigated [11-14]. A simplified circuit of the paralleled current-mode control is shown in Fig. 2(b). Because the output current is proportional to the voltage error signal, the current command of every module is controlled by common voltage feedback. The common feedback circuit can not be modularized, the system may be shut down for the failure of the common part. The single-wire current sharing for current-mode control had been studied in the literature [5,7]. Commercialized control IC, such as UC1907, can be also used in current-mode controlled modules [5], but the share bus carry the maximum current information of paralleled modules. Another method proposed by K. T. Small in 1988 [7] is shown in Fig 2(c). The share bus carries the average current command signal, and the current sharing error is injected into the reference voltage. Bandwidth of the current sharing response is limited by the voltage loop. In this paper, a novel current sharing control is proposed, the simplified circuit is shown in Fig. 2(d). The share bus carries the average inductor current signal and the injected point of current sharing signal is on the inner current loop. Bandwidth of the current sharing control is not limited by the voltage loop.

In the following, the new current sharing circuit of current-mode controlled converters is described and analyzed. The design guidelines are listed and a design example of the average current-mode controlled modules is implemented. Finally, the experimental results verify the performance of the circuit.

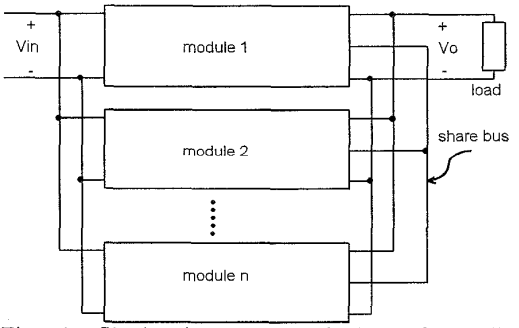

Fig. 1. Single-wire current sharing of paralleled converter modules.

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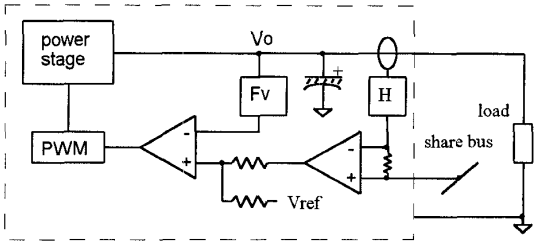
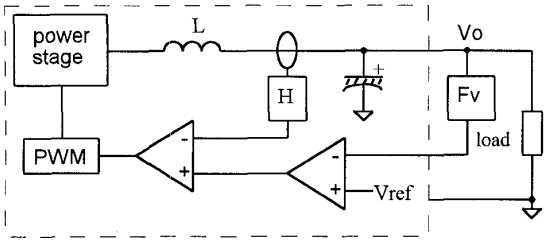
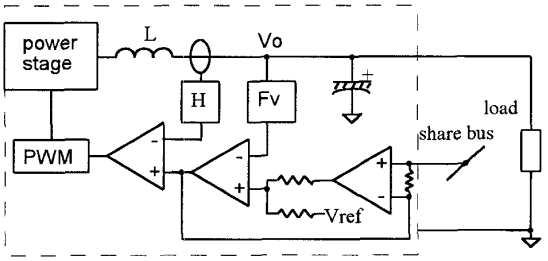


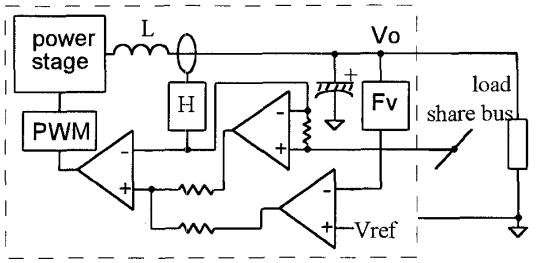
(a) Conventional voltage-mode.



(b) Current-mode with the common voltage feedback.



(c) Current-mode with the average current command share bus.



(d) Proposed control scheme: Current-mode with the average inductor current share bus.

Fig. 2. Comparison among the current sharing control schemes.

2. CIRCUIT DESCRIPTION

The circuit of a single module in the proposed control is depicted in Fig. 3. Three operational amplifiers form the control circuit. The functions of each portion are:

1) The share bus: It carries the instantaneous average current signal for the reference of the module current when paralleling. A share resistor R_S of high accuracy is connected between the share bus and the output of the current sensor H. When the values of R_S for every module are all the same, the output current of the modules are the same. If they are proportional, the output currents are also proportional.
2) The voltage error amplifier U_V: It amplifies the output voltage error signal as the current command. The current command is composed of the voltage error and the current sharing error.
3) The current sharing amplifier U_S: It amplifies the error signal of share bus and inductor current and injects into the current command.
4) The current amplifier U_C: It amplifies the current error signal between the inductor current and current command and sends the error to the modulator.
5) The pulse width modulator: Analog control signal is modulated into duty cycle.
6) The power stage: Include the power switches, switch drivers and output filters L_f and C_O.
7) The current sensor H: Hall effect sensor or other device to sense the inductor current.

3. CIRCUIT OPERATIONS

In this section, the circuit operations of a single module and multi-module paralleling are presented:

A. Single module: The current signal of the module is equal to the share bus because the input impedance of share amplifier is high enough and no current passes through R_S. Thus the sharing error signal is zero and the control is the same as a standard two-loop control.

B. Multi-module paralleling: Because the same value of the share resistor R_S, the share bus carries average current signal reference. The share error signal is the difference between the share bus and the individual output current. This error is injected into current command, by the PWM control and power circuits, the average inductor

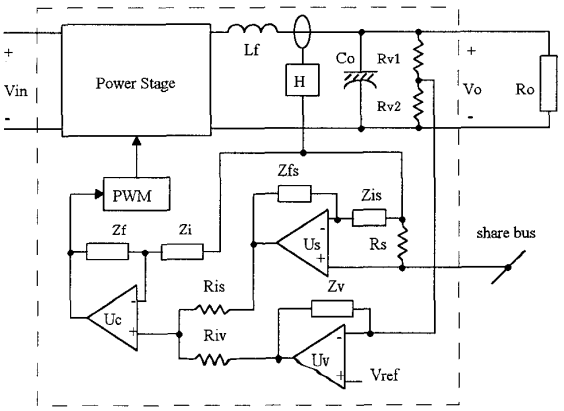


Fig. 3. Proposed control circuit for one current-mode controlled module.

current is adjusted. When the output current is lower than the signal, the injected error tends to increase the inductor current to reduce the error. This negative feedback mechanism will reduce the error within the tolerance. At the steady state the output current of every module is the same as the share bus indicated, the purpose of the current sharing is achieved.

4. ANALYSIS

There are three control loops in the presented circuit-the voltage loop, the sharing loop, and the current loop. A simplified circuit model for paralleled modules is set up and the control loop analysis is performed to derive the design rules of the proposed current sharing controller.

The circuit between share resistors and share bus is shown in Fig. 4. For n paralleled modules. v_{I1}... v_{In} are the instantaneous voltage signals derived by the current sensors from the inductor currents, v_{Ibus} is the

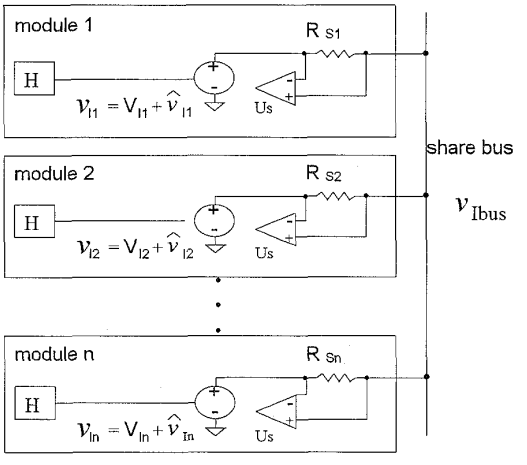


Fig. 4. The circuit between share bus and the share resistors.

instantaneous voltage signal on the share bus. If the share resistors RS1...RSn are equal, then

$$v_{Ibus} = \frac{1}{n}(v_{I1} + v_{I2} + \ldots + v_{In}) \quad (1)$$

In small-signal analysis,

$$\hat{v}_{Ibus} = \frac{1}{n}(\hat{v}_{I1} + \hat{v}_{I2} + \ldots + \hat{v}_{In}) \quad (2)$$

If the transfer function of the current sensor is H, then

$$\hat{v}_{Ibus} = \frac{H}{n}(\hat{i}_{L1} + \hat{i}_{L2} + \ldots + \hat{i}_{Ln}) \quad (3)$$

Where $\hat{i}_{L1}, \hat{i}_{L2}, \ldots, \hat{i}_{Ln}$ are the small-signal representations of the output inductor currents.

Neglecting the input voltage disturbance, the control block diagram for one of the paralleled module is shown in Fig. 5.

F_V : The voltage feedback transfer function.

H : The current to voltage signal transfer function.

Fm : The PWM modulator transfer function.

G_V : The duty cycle to output voltage transfer function.

G_i : The duty cycle to inductor current transfer function.

Gs : The transfer function of the current sharing amplifier.

G_{CC} : The current amplifier transfer function for current loop.

G_{CS} : The current amplifier transfer function for sharing loop.

G_{CV} : The current amplifier transfer function for voltage loop.

$\hat{v}_o$, $\hat{i}_L$ and $\hat{d}$ are the disturbances of output voltage, inductor current and duty cycle.

In Fig. 5, if the module n has a current sharing disturbance, the injected current sharing error signal

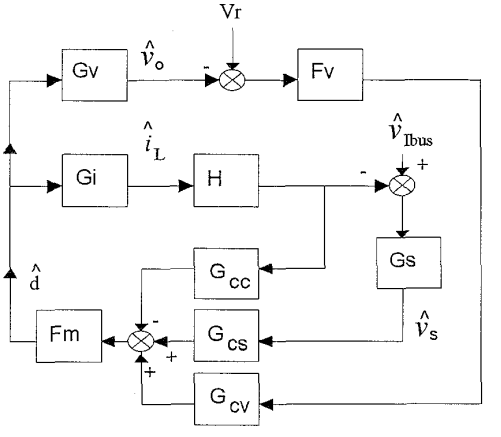


Fig. 5. Block diagram of the control circuits.

into the controller $\hat{v}_S$ is

$$\hat{v}_S = G_S(\hat{v}_{Ibus} - H\hat{i}_L) \quad (4)$$

Substitute (3) into (4) and $\hat{i}_L \equiv \hat{i}_{Ln}$,

$$\hat{v}_S = -\frac{n-1}{n}G_S H\hat{i}_{Ln} + G_S\frac{H}{n}(\hat{i}_{L1} + \hat{i}_{L2} + \ldots + \hat{i}_{Ln-1}) \quad (5)$$

The disturbances of the inductor currents of other modules can not form a local feedback loop in module n. The second term of (5) can be considered as an external disturbance to take into account the interactions among the modules. So

$$\hat{v}_S = -\frac{n-1}{n}G_S H\hat{i}_L \quad (6)$$

The open loop gains — the voltage loop T_V, the sharing loop T_S, and the current loop T_I can be derived from Fig. 5

$$T_I = F_m G_{cc} H G_i \quad (7)$$

$$T_V = F_m G_{cv} F_v G_v \quad (8)$$

$$T_S = \frac{n-1}{n} F_m G_{CS} G_S H G_i \quad (9)$$

When only one module is used, the loop gain of current sharing, T_S=0. And when an infinity number of modules paralleled, $T_S = F_m G_{CS} G_S H G_i$. Then, the three-loop control method [15] can be used to design the controller.

5. DESIGN CONSIDERATIONS

According to the analysis, the following design guidelines have been developed:

A. About the average current-mode control, the second pole of the error amplifier U_C must be placed after half the switching frequency. The zero of U_C must be placed at least one decade before half of the switching frequency. The external ramp setting is similar to the voltage-mode. Choose the gain of the error amplifier U_C that makes proper damping on the resonant peak at half of the switching frequency [16].

B. The design must base on the multi-module condition, because the overall loop gain is higher than the single module case. To identify the stability, the closed-loop gains which include the overall loop gain T_1 and the outer loop gain T_2 are [15]

$$T_1 = T_I + T_S + T_V \quad (10)$$

$$T_2 = \frac{T_V}{1 + T_I + T_S} \quad (11)$$

T_1 and T_2 can be experimentally measured or mathematically computed [6].

C. To obtain the benefits of current mode control, the crossover frequency of the current loop must be higher than that of the voltage loop. The high bandwidth of the current loop can improve the closed-loop response of the multi-loop control [17]. It is better to design the current loop as high as possible no matter in the single module or multi-module case.

D. To avoid the dip [16] in the overall loop gain which cause the system unstable, do not make the phase of the two loops are in opposite direction when the two loops cross over. For example, the $|T_I|=|T_V|$ and $T_I(-90°)$ and $T_V(-270°)$ should not occur at the same frequency. The subtraction of the two loops will cause a dip which make the system unstable.

E. To simplify the design, the control of current sharing amplifier U_S is commonly used of proportional control [8]. The gain G_S of the current sharing amplifier must be as high as possible if the modules are stable. The accuracy of current sharing is determined by G_S for proportional control.

6. DESIGN EXAMPLE

A design example of the proposed current sharing control of paralleled DC power supplies is demonstrated in this section. The DC/DC converter is 400V/48V 20A output. For average current-mode control, the full bridge phase-shifted PWM ZVS topology is selected. The main transformer of the converter is not center-tapped but uses two independent inductor as the current doubler. The complete circuit of a single module is shown in Fig. 6.

The circuit parameters are listed as follows:

The switching frequency f_S	100kHz
Turn ratio of the main transformer	18:6
Power MOSFET Q_a-Q_d	500V/30A
Output inductor filter L_{f1}, L_{f2}	200uH
Fast recovery diodes D_1, D_2	600V/60A
The primary inductor L_{lk}	4uH
Output capacitor C_o	6900uF
Transfer ratio of the current sensor H	4V/100A
Phase shift PWM controller	UC3875N

The output voltage of the current doubler is half of the transfer voltage output and the filter inductance is the parallel of the two inductor filters. The turn ratio of the primary to secondary of the main transformer is m=0.5*(1/3)=1/6, and the output filter inductor $L_f = L_{f1} // L_{f2}$=100uH. The equivalent circuit is illustrated in Fig. 7. As the power stage parameters are given the controller and current sharing network can then be designed.

The parameters and the transfer functions are listed:

N : Number of modules be paralleled, n=1 to infinity.

R_o: The load resistance for a module. If n=2 and the output voltage and current is 48V/40A, the load current for every module is 20A, the load resistance Ro=2.4Ω.

Vin : The input voltage, Vin=400V.

$F_V = R_{Vf} / R_{V1} \cong 1$

Gs=10.

Fm=0.25.

L_{lk}=4uH.

m : The equivalent transfer turn ratio m=1/6.

L_f : The equivalent output filter inductor 100uH.

C_o : The output filter capacitor 6900uH.

R_i : The transfer ratio of the hall sensor, R_i=0.04V/A.

For modeling the current-mode control the sampling gain is inserted in the current sensing network [16], so the transfer function of current sensor is

$$H = R_i H_e(s) = R_i (1 + \frac{s}{\omega_s Q} + \frac{s^2}{\omega_s^2}) \quad (12)$$

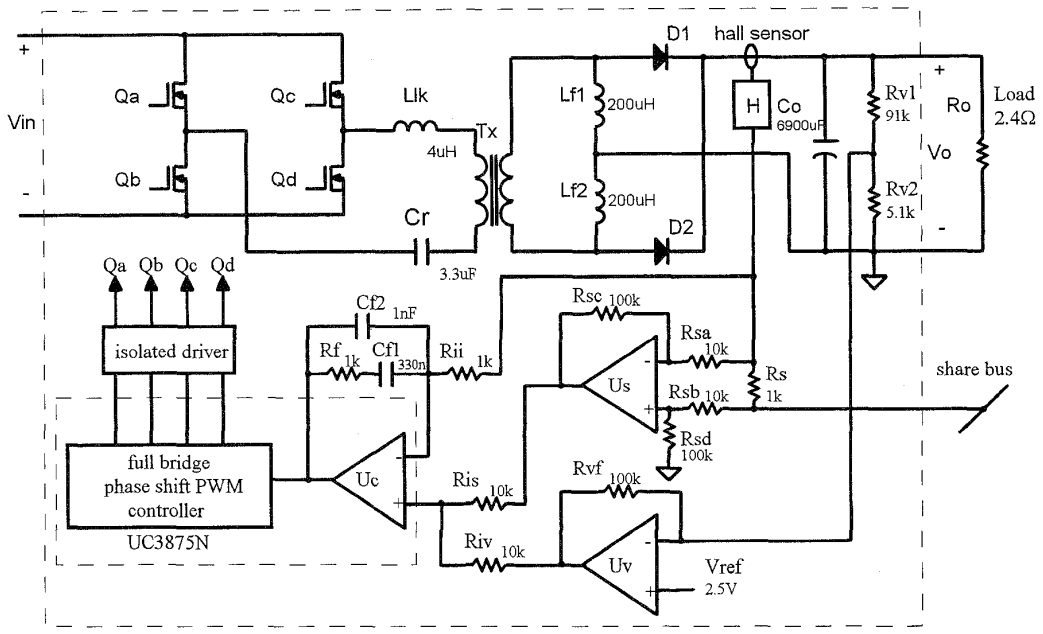


Fig. 6. Circuit diagram of the design example

He(s) is the sampling gain of the current-mode control, Q=-2/π, ωs=2πfs. The models of phase-shifted PWM converter are [18]

$$G_V = \frac{mV_{in}Z_f}{Z_f + R_d}\left(\frac{1}{\Delta f}\right) \tag{13}$$

$$G_I = \frac{mV_{in}}{Z_f + R_d} \tag{14}$$

Where

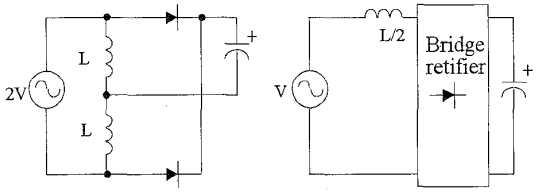
$$R_d = 4m^2 L_{lk} f_s \tag{15}$$

$$Z_f = \frac{R_O \Delta f}{1 + sR_O C_O} \tag{16}$$

$$\Delta f = s^2 L_f C_O + s\frac{L_f}{R_O} + 1 \tag{17}$$

The transfer functions of the current amplifier are

$$G_{CC} = \omega_t \frac{(s+\omega_z)}{s(s+\omega_p)} \tag{18}$$



(a) Current doubler (b) Equivalent circuit

Fig. 7. The equivalent circuit of the current doubler.

$$G_{CS} = \frac{R_{iv}}{R_{is} + R_{iv}}\left[1 + \omega_t \frac{(s+\omega_z)}{s(s+\omega_p)}\right] \tag{19}$$

$$G_{CV} = \frac{R_{is}}{R_{is} + R_{iv}}\left[1 + \omega_t \frac{(s+\omega_z)}{s(s+\omega_p)}\right] \tag{20}$$

Where

$$\omega_z = \frac{1}{R_f C_{f1}} \tag{21}$$

$$\omega_p = \frac{C_{f1} + C_{f2}}{R_f C_{f1} C_{f2}} \tag{22}$$

$$\omega_t = \frac{1}{R_{ii} C_{f2}} \tag{23}$$

The half of the switching frequency is 50kHz. The second pole of error amplifier is placed at 160kHz and the zero is place at 500Hz. The gain of the amplifier is set to make the bandwidth of the current loop high enough and the system is stable. The following equation can help to find the approximate value of R_{ii} [16]:

$$R_{ii} = \frac{(\frac{1}{2} + \frac{1}{\pi})F_m V_{in} R_i}{(C_{f1} + C_{f2}) L_f f_s \omega_z} \tag{24}$$

Because the current sharing signal is injected, the value of R_{ii} must be changed to make the bandwidth of the current loop suitable for single module or paralleled condition. The Bode diagram is used to find the optimum value of R_{ii}.

The gain of current loop can be adjusted by R_{ii} and the gain of current sharing loop and voltage loop

can be adjusted by R_{iS}, R_{iV} and G_S. For the circuit of Fig. 6, the simulated loop gains of light load (R_O=480Ω) condition are shown in Fig. 8 and Fig. 9. The simulated loop gains for full load (R_O=2.4Ω) condition are shown in Fig. 10 and Fig. 11. All the closed-loop gains show that the power supply system is stable.

7. EXPERIMENTAL RESULTS

Two 400V/48V, 20A output current DC/DC converter modules are implemented as shown in Fig. 6. To test the performance of the current sharing circuit, an experiment of changing the total load current from zero to 20A has been conducted. The transient response of the output currents and inductor currents for disconnected and connected share bus conditions are shown in Fig. 12. In Fig. 12(a), without the current sharing bus, the output current is not equally distributed because the inductor currents do not charge the output capacitors at the same time during the load transient. In Fig. 12(b), the share bus forces the output inductor currents charge the output capacitors almost simultaneously. The output currents of the two modules are very close. The over-current condition is then avoided. At the steady state, the output current is equal to the inductor current. The current sharing is always controlled by the proposed circuits in transient or steady state. The steady state test for current sharing accuracy is recorded in table I.

8. CONCLUSIONS

The proposed single-wire current sharing of current-mode controlled power supplies has the high-speed response to reduce the unbalance of the current distribution during the transient and avoids the minor alarm of the current limit. The current sensor for feedback control and current sharing is the same so that the cost is not higher than the voltage-mode control. It can be used in all modularized converters and the design of the modules can follow the multi-loop control method. Compared with the conventional voltage-mode control current sharing, the performance of the proposed current-mode power supply system is much improved.

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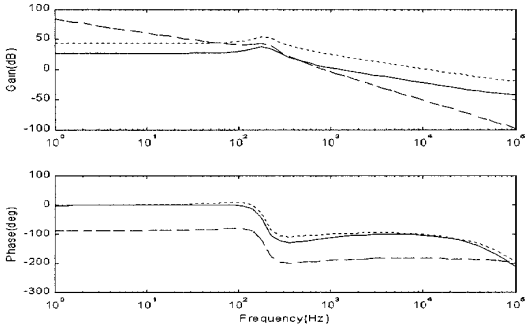


Fig. 8. Simulated open-loop gains T_I, T_S and T_V for light load case(Ro=480Ω). (T_I ——, T_S -----, T_V — —)

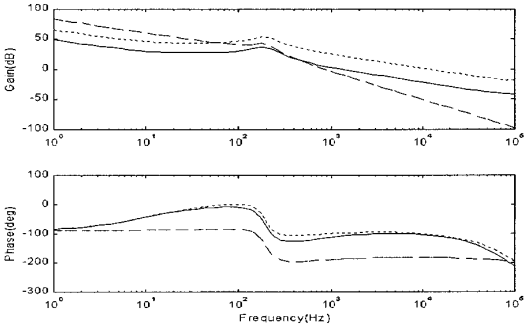


Fig. 10. Simulated open-loop gains T_I, T_S and T_V for full load case(Ro=2.4Ω). (T_I ——, T_S -----, T_V — —)

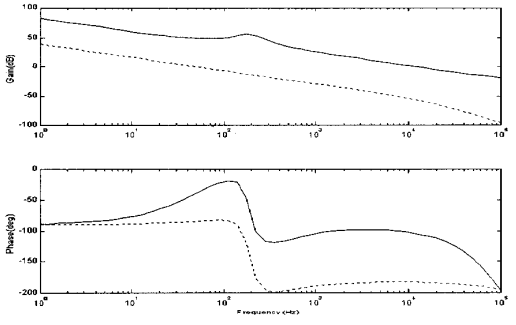


Fig. 9. Simulated close-loop gains $T_1$and T_2 for light load case(Ro=480Ω). (T_1 ——, T_2 -----)

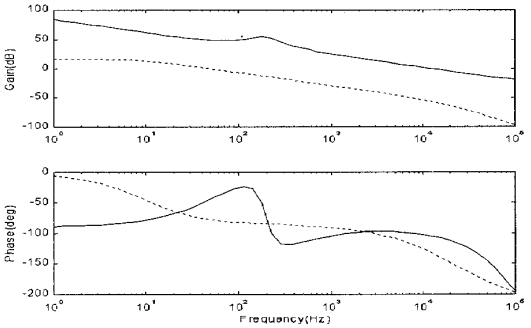
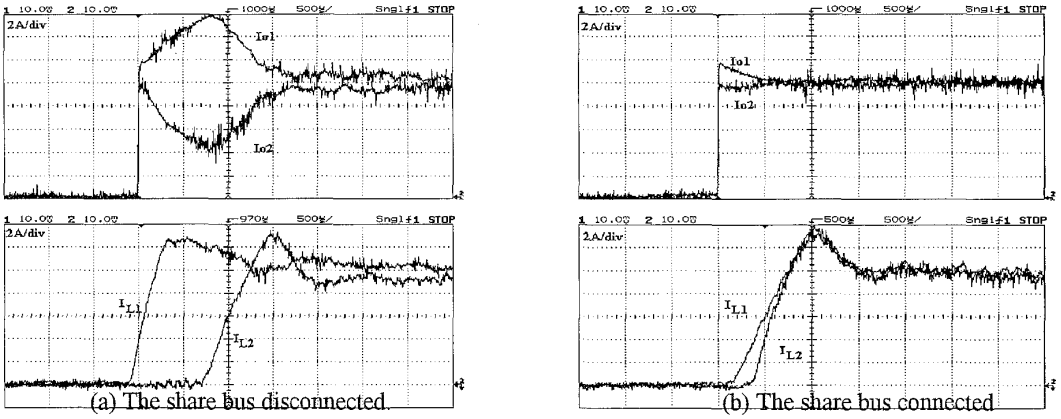


Fig. 11. Simulated close-loop gains $T_1$and T_2 for full load case(Ro=2.4Ω). (T_1 ——, T_2 -----)



(a) The share bus disconnected. (b) The share bus connected

Fig. 12. Transient responses of the output currents.

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Table I The current sharing test recordings.

I_{O1} (A)	I_{O2} (A)	I_{TOTAL} (A)	I_{AVG} (A)	I_{ERROR} (A)	ERROR (%)
2.54	2.61	5.15	2.58	0.07	2.72
5.04	4.95	9.99	5.00	0.09	1.80
7.48	7.25	14.73	7.37	0.23	3.12
9.94	9.70	19.64	9.82	0.24	2.44
12.53	12.05	24.58	12.29	0.48	3.91
14.86	14.29	29.15	14.58	0.57	3.91
17.76	17.11	34.87	17.44	0.65	3.73
19.87	19.45	39.32	19.66	0.42	2.14