2002 IEEE 信號系統研討會

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一、 參加會議過程

2002 年 IEEE 信號系統研討會（IEEE Workshop on Signal Systems－Design and Implementation ）於十月十六日至十八日在美國聖地牙哥舉行。今年共有八十八篇來自世界各國工業界及研究機構的投稿，經技術委員會仔細評選及審核後，共選出五十篇文章，並統一編於 Workshop Proceedings。今年的議程主題為「Signal Processing Microsystems for Broadband Communications」，而大會特邀請此方面之專家學者做一系列專題演講，茲分述如下：

- "System-on-a-Chip Design for Broadband Communications," by Dr. Henry Samueli, Co-Chairman and Chief Technical Officer, Broadcom Corporation, Irvine.
- "Shannon vs Moore: Driving the Evolution of Signal Processing Platforms in Wireless Communications," by Dr. Ravi Subramanian, President & Co-Founder Morphics Technology.
- "Design Approaches for MPEG Engines for Broadband and Mobile Applications," by Dr. Takao Nishitani and Ichiro Kuroda, NEC

演講者就信號處理的最新趨勢及演進，做一系列深入徹底的探討，讓與會者均有很大的收穫。除專題演講外，一般議程以下列主題分作口頭報告（Oral Section）及海報展示（Poster Section）兩種方式進行：

- Multimedia Processing (lecture session)

- DSP Architectures for Multimedia Applications (poster session)
- Wireless Systems (lecture session)
- Architectures and Algorithms for Communications (poster session)
- Arithmetic and Design Methodologies (poster session)
- Design and Synthesis Methodologies (lecture session)

口頭報告中，每位演講者以二十分鐘報告論文。比較特殊的是海報展示；在展示開始前，大會安排約一小時的時間讓每位演講者先行以四分鐘簡約報告其研究動機、研究方法及成果，使與會者得以了解 poster 全貌。接著再利用一個半小時做海報展示，讓與會者及發表論文的學者能面對面地研討技術細節。

二、 與會心得及建議

SiPS 的前身是 IEEE Workshop on VLSI Signal Processing，為從事 VLSI 信號處理研究的專家學者所積極參加的年度聚會。由於人數皆控制在百人左右，不但可使與會者容易彼此認識，並可做詳盡討論，為筆者主要參加的國際研討會之一。

三、 攜回資料

「SiPS Workshop Proceeding CDROM」 乙片

HIGH-PERFORMANCE ADAPTIVE DECISION FEEDBACK EQUALIZER BASED ON PREDICTIVE PARALLEL BRANCH SLICER SCHEME

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Abstract- Among existing works of high-speed pipelined *Adaptive Decision Feedback Equalizer (ADFE)*, the pipelined ADFE using Relaxed Look-ahead technique results in a substantial hardware saving than the parallel processing or Look-ahead approaches. However, it suffers from both the SNR degradation and slow convergence rate. In this paper, we employ the *Predictive Parallel Branch Slicer (PPBS)* to eliminate the dependencies of the present and past decisions so as to reduce the iteration bound of Decision Feedback Loop of the ADFE. By adding negligible hardware complexity overheads, the proposed architecture can help to improve the output Mean-square-error (MSE) of the ADFE compared with the Relaxed Look-ahead ADFE architecture. Moreover, we show the superior performance of the proposed pipelined ADFE by theoretical derivations and computer simulation results.

I. Introduction

Adaptive Decision Feedback Equalizer (ADFE) using *Least Mean-Squared (LMS)* algorithm is a well-known equalization technique for magnetic storage and digital communication. However, the fine-grain pipelining of the ADFE is known to be a difficult problem for high-speed applications. This is due to the *Decision Feedback Loop (DFL)*. According to the Iteration Bound [1], the smallest clock period of ADFE is bounded by the DFL. Several approaches are proposed to solve aforementioned problems. For example, pipelining the ADFE can be achieved by precomputing all possible in DFL to open the DFL [2]. However, it results in a large hardware overhead as it transforms a serial algorithm into an equivalent (in the sense of input-output behavior) pipelined algorithm. Another algorithm is proposed in [3], which is referred as PIPEADFE1. It maintains the functionality instead of input-output behavior using the technique of *Relaxed Look-ahead*. Although the hardware overhead in this algorithm is small, it suffers from some performance degradation such as output SNR and convergence rate. Nevertheless, from VLSI implementation point of view, the second approach is suitable for low-cost VLSI designs.

PIPEADFE1 intends to cancel the first D_1 post-cursor ISI terms by the *Feedfoward filter (FFF)*. However, it is not necessary to force the first D_1 taps of *Feedback filter (FBF)* to zeros. In this paper, we employ the FFF to force the first D_1 coefficients of FBF to the more appropriate fixed coefficients instead of zeros. By doing so, we can significantly improve the output MSE in the slicer. Then, the *Predictive Parallel Branch Slicer (PPBS)* can be employed to eliminate the dependencies of the present and past decisions in order to reduce the iteration bound of DFL. Finally, the MSE performance of the proposed architecture is analyzed mathematically. The theoretical results and computer simulation results show that the output MSE of our proposed architecture is superior to PIPEADFE1.

II. Review of Pipelined ADFE Architecture (PIPEADFE1)

In [3], the *Delayed LMS* [6] and the technique of *Transfer Delay Relaxation* [7] are employed to develop the PIPEADFE1. Then, *Sum Relaxation* is applied to pipeline the updating circuit of ADFE. The equations describing the PIPEADFE1 (see Fig. 1) are summarized below:

$$\tilde{x}(n) = \mathbf{F}^{\mathrm{T}}(n - D_4)\mathbf{Y}(n) + \mathbf{B}^{\mathrm{T}}(n - D_4)\mathbf{D}(n)\ , \quad (1a)$$

$$e(n) = x(n) - \tilde{x}(n), \quad (1b)$$

$$x(n) = \mathrm{Q}[\tilde{x}(n)], \quad (1c)$$

$$\mathbf{F}(n) = \mathbf{F}(n - D_4) + \mu \sum_{i=0}^{LA-1} e(n - D_2 - i)\mathbf{Y}(n - D_2 - i), \quad (1d)$$

$$\mathbf{B}(n) = \mathbf{B}(n - D_4) + \mu \sum_{i=0}^{LA-1} e(n - D_3 - i)\mathbf{D}(n - D_3 - i), \quad (1e)$$

where $\mathbf{Y}(n) = [y(n), y(n-1), \ldots\ldots, y(n-N_f+1)]^T$, is the vector of the received samples, $\mathbf{D}(n) = [x(n-1-D_1) \ldots\ldots\ldots\ldots x(n-D_1-N_b)\ ]^T$, is the vector of detected symbols, $\tilde{x}(n)$ is the input to $Q(\bullet)$, and $x(n)$ is the quantizer decision.

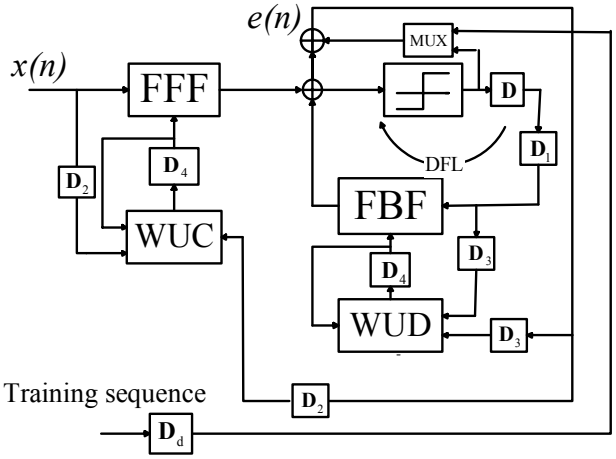


Fig. 1. PIPEADFE1 architecture.

III. New Architecture of Pipelined Adaptive DFE (PIPEADFE2)

In this section, we will introduce the new architecture of pipelined ADFE, which is referred as PIPEADFE2. . For clarity, we will demonstrate the basic concept of PIPEADFE2 by a simple example. In this example, we assume that the transmitted *Binary Phase-Shift Keying (BPSK)* signals are passed through the ISI channel, and the number of taps in FFF and FBF are N_f and N_b, respectively. In the most wireline communication systems, the channel impulse response can be roughly estimated by the laboratory or field measurement. However, the practical channel impulse response is still different from the estimated channel impulse response. In this paper, we will exploit this feature to develop the PIPEADFE2. According to the roughly estimated channel response, we can calculate the optimal coefficients, $\mathbf{V}_e$, for the first D_1 taps of the FBF in PIPEADFE2, and fix these D_1 coefficients. Then, the decision of slicer at time instance n, $x(n)$, can be expressed as

$$\tilde{z}(n) = \mathbf{F}(n)^{\mathrm{T}}\mathbf{Y}(n) + \mathbf{V}_e{}^{\mathrm{T}}\mathbf{X}(n) + \mathbf{B}(n)^{\mathrm{T}}\mathbf{D}(n), \quad (2)$$

$$x(n) = Q[\tilde{z}(n)], \quad (3)$$

where $Q[\bullet]$ is a BPSK slicer, $\tilde{z}(n)$ is the input of slicer at time instance n, $x(n)$ is the decision of slicer at time instance n, $x(n) \in \{+1, -1\}$, $\mathbf{Y}(n)$ is the vector of receiver samples in the input of FFF, $\mathbf{X}(n) = [x(n-1),\ x(n-2)\ \cdots\ x(n-D_1)]^T$, is the input vector for the first D_1 coefficients in FBF, $\mathbf{D}(n) = [x(n-D_1-1),\ x(n-D_1-2),\ \cdots\ x(n-N_b)]^T$, is the input vector for the rest coefficients in FBF, $\mathbf{F}(n)$ is the vector of FFF coefficients, $\mathbf{V}_e$ is the vector of the first D_1 coefficients in FBF, $\mathbf{B}(n)$ is the vector of the rest coefficients in FBF. Hence, this algorithm can be considered as a constraint optimization problem. Mathematically, it can be expressed as follows.

$$Min\{\mathbf{E}(x(n) - \tilde{z}(n))^2\}, \text{subject to } \mathbf{V}(\mathrm{n}) = \mathbf{V}_{\mathrm{e}}, \quad (4)$$

where $\mathbf{E}(\bullet)$ represents the expectation operator.

By using the above settings, the *Predictive Parallel Branch Slicer (PPBS)*, which is similar to the *Look-ahead Computation* [2], can be employed to eliminate the dependencies between $\tilde{z}(n)$ and $\mathbf{X}(n)$ in order to pipeline the DFL. The inputs of PPBS, $b(n)$, can be written as

$$b(n) = \mathbf{F}(n)^{\mathrm{T}}\mathbf{Y}(n) + \mathbf{B}(n)^{\mathrm{T}}\mathbf{D}(n). \quad (5)$$

It also can be expressed as

$$b(n) = x(n) - \mathbf{V}_e{}^{T}\mathbf{X}(n) + \eta(n), \quad (6)$$

where $\eta(n)$ denotes the residual ISI and noise components.

According to (6), we still need to remove the first D_1 ISI terms in $b(n)$. There are 2^{D_1} branches inside the PPBS as shown in Fig. 2. In the PPBS, the past D_1 decisions, $\mathbf{X}(n)$, are not available. In the branch j, we assume the

past decisions are, $\mathbf{T}_j = [a_{1,j},\ a_{2,j},\ \cdots\ a_{D_1,j}]^T$, which is called the tentative past decision. For convenience, we define a mapping function, ϕ, as follows.

$$j = \phi(\mathbf{T}_j = [a_{1,j},\ a_{2,j}, \cdots, a_{D_1,j}]^T) = \sum_{i=1}^{D1} 2^{D_1 - i}[(a_{i,j} + 1)/2]. \quad (7)$$

This mapping function can be interpreted as a one-to-one mapping from the index of branch to its corresponding tentative past decisions. Hence, the tentative decisions in the branch j, d_j, are as follows.

$$d_j = Q[b(n) + \mathbf{V}_e^T \mathbf{T}_j]. \quad (8)$$

The tentative estimation error of each branch in the PPBS, $e_{t,j}$, is as follows.

$$e_{t,j} = d_j - (b(n) + \mathbf{V}_e^T \mathbf{T}_j). \quad (9)$$

Since $\mathbf{V}_e$ and $\mathbf{T}_j$ are fixed, $\mathbf{V}_e^T \mathbf{T}_j$ can be pre-computed in advance. The function in (8) and (9) can be implemented using a fixed coefficient adder. Hence, the hardware overhead and the critical path of PPBS are quite small. Finally, the actual decision of PPBS, $x(n)$, is one of these tentative decisions, and $x(n)$ depends on the past decisions of PPBS, $\mathbf{M} = [x(n-1)\quad x(n-2)\quad \cdots\quad x(n-D_1)]^T$. Thus, $x(n)$ can be expressed as

$$x(n) = d_S,\ S = \phi(\mathbf{M}). \quad (10)$$

In general, the above operations can be implemented by the 2^{D_1}-to-one multiplexer. Moreover, the PPBS also need to output the estimating error corresponding the final decision of PPBS, *x(n),* in order to update the FFF and the rest FBF coefficients. *e(n)* is shown as follows.

$$e(n) = e_{t,S},\ S = \phi(\mathbf{M}). \quad (11)$$

This operation also can be implemented by the 2^{D_1}-to-one multiplexer.

The architecture of PIPEADFE2 with D_1 =3 (Speedup factor=4) is shown in Fig. 2. In general, the updating circuits applied in PIPEADFE2, **WUF** and **WUB**, are similar to the PIPEADFE1 [3]. Since there are D_1 of extra delay elements in the DFL, the iteration bound of PIPEADFE2 can be reduced to $(T_m + 3T_a + T_s)/(D_1 + 1)$, where T_m is symbol multiplier delay, T_a is the adder delay, and T_s is the slicer delay. Then, the conventional retiming technique [1] can be applied to pipeline the DFL. Compared with the PIPEADFE1, the total overheads of hardware complexity in the PIPEADFE2 are merely 2^{D_1} adders and two 2^{D_1}-to-one multiplexer. Due to the inaccuracy of this roughly estimated channel impulse response, the output MSE of PIPEADFE2 will be degraded as the difference between the estimated and practical channel impulse response increases. The detailed relation between the output MSE and the inaccuracy of estimated channel impulse response will be analyzed mathematically in the next section. Moreover, it is obvious that the PIPEADFE2 becomes the PIPEADFE1 when the coefficients of the first D_1 taps, $\mathbf{V}_e$, in the FBF are zeros.

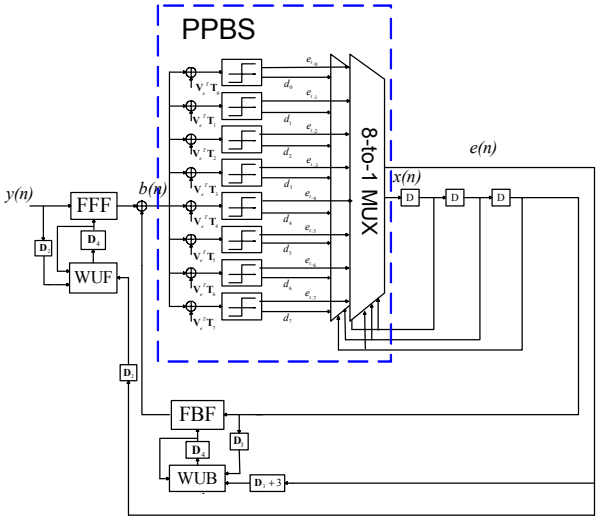


Fig. 2. The architecture of PIPEADFE2.

IV. Performance Analysis and Comparisons of PIPEADFE2

In this section, we will show the relationship between the output MSE of PIPEADFE2 and the inaccuracy of the roughly estimated channel impulse response by the mathematical analyses and computer simulations.

A. Performance Analysis of PIPEADFE2

In the following analysis, the optimal coefficients (Wiener solution) for the roughly estimated channel impulse response can be denoted as $\mathbf{W}_e^T = [\mathbf{F}_e^T\quad \mathbf{V}_e^T\quad \mathbf{B}_e^T]$, where $\mathbf{F}_e^T$ represents the optimal coefficients of FFF, $\mathbf{V}_e^T$ and $\mathbf{B}_e^T$ denote the optimal coefficients of the first D_1 taps and the rest coefficients

in FBF, respectively. $\mathbf{W}_p^T = [\mathbf{F}_p^T \quad \mathbf{V}_p^T \quad \mathbf{B}_p^T]$ denotes the optimal coefficients for the practical channel impulse response, where $\mathbf{F}_p^T$ represents the optimal coefficients of FFF; $\mathbf{V}_p^T$ and $\mathbf{B}_p^T$ denote the optimal coefficients of the first D_1 taps and the rest coefficients in FBF, respectively . Here, we define the *Inaccuracy Index*,

$$\Gamma = \frac{(\mathbf{V}_e - \mathbf{V}_p)^H (\mathbf{V}_e - \mathbf{V}_p)}{\mathbf{V}_p^H \mathbf{V}_p} \tag{12}$$

, to describe the inaccuracy of the first D_1 FBF coefficients in PIPEADFE2. Clearly, the *Minimum Mean-square Error (MMSE)* of PIPEADFE2 will be the same as the conventional (serial) ADFE when the fixed coefficients, $\mathbf{V}_e^T$, is equal to $\mathbf{V}_p^T$ ($\Gamma = 0$). Assume the autocorrelation of the transmitted data is $\sigma_x^2\mathbf{I}$, where σ_x^2 is the transmitted data variance. By apply the method in [4], the MSE of PIPEADFE2 given the first D_1 FBF coefficients, $\mathbf{W}^T = [\mathbf{F}^T \quad \mathbf{V}_e^T \quad \mathbf{B}^T]$, can be expressed as

$$\begin{aligned} J_e(\mathbf{W}) &= J_{\min,p} + (\mathbf{W} - \mathbf{W}_p)^T \mathbf{R}_p (\mathbf{W} - \mathbf{W}_p) \\ &= J_{\min,p} + (\mathbf{W} - \mathbf{W}_p)^T \begin{bmatrix} \mathbf{R}_{YY} & \mathbf{P}_{YX} & \mathbf{P}_{YD} \\ \mathbf{P}_{YX}^T & \sigma^2\mathbf{I} & 0 \\ \mathbf{P}_{YD}^T & 0 & \sigma^2\mathbf{I} \end{bmatrix} (\mathbf{W} - \mathbf{W}_p) \\ &= J_{\min,p} + \mathbf{k}^T \mathbf{R}_e \mathbf{k} + \mathbf{r}^T [\mathbf{P}_{YX}^T \quad 0]\mathbf{k} + \mathbf{k}^T \begin{bmatrix} \mathbf{P}_{YX} \\ 0 \end{bmatrix} \mathbf{r} + \sigma^2 \mathbf{r}^T \mathbf{r} \end{aligned} \tag{13}$$

,where

- $\mathbf{R}_e = \mathbf{E}\{\begin{bmatrix} \mathbf{Y}(n) \\ \mathbf{D}(n) \end{bmatrix} [\mathbf{Y}^T(n) \quad \mathbf{D}^T(n)]\}$ is the autocorrelation of the PIPEADFE2,
- $\mathbf{R}_{YY} = \mathbf{E}\{\mathbf{Y}(n)\mathbf{Y}^T(n)\}$ is the autocorrelation of FFF input samples,
- $\mathbf{P}_{YX} = \mathbf{E}\{\mathbf{Y}(n)\mathbf{X}^T(n)\}$ is the crosscorrelation of $\mathbf{Y}$(n) and $\mathbf{X}$(n) ,
- $\mathbf{P}_{YD} = \mathbf{E}\{\mathbf{Y}(n)\mathbf{D}^T(n)\}$ is the crosscorrelation of $\mathbf{Y}$(n) and $\mathbf{X}$(n)
- $\mathbf{k}^T = [(\mathbf{F} - \mathbf{F}_p)^T \quad (\mathbf{B} - \mathbf{B}_p)^T]$,
- $\mathbf{r}^T = (\mathbf{V}_e - \mathbf{V}_p)^T$.

Since $\mathbf{R}_e$ is the positive-definite matrix, the Cholesky factorization can be applied to factorize $\mathbf{R}_e$. That is, $\mathbf{R}_e = \mathbf{L}\mathbf{L}^T$, where $\mathbf{L}$ is the lower triangular matrix. Then, we can reformulate (13) as follows.

$$\begin{aligned} J_e(\mathbf{W}) &= J_e(\mathbf{k}) \\ &= J_{\min,p} + (\mathbf{k}^T\mathbf{L} + [\mathbf{r}^T\mathbf{P}_{YX}^T \quad \mathbf{0}](\mathbf{L}^T)^{-1})(\mathbf{L}^T\mathbf{k} + \mathbf{L}^{-1}\begin{bmatrix} \mathbf{P}_{YX}\mathbf{r} \\ \mathbf{0} \end{bmatrix}) \\ &\quad - \mathbf{r}^T[\mathbf{P}_{YX}^T \quad \mathbf{0}]\mathbf{R}_e^{-1}\begin{bmatrix} \mathbf{P}_{YX} \\ \mathbf{0} \end{bmatrix}\mathbf{r} + \sigma^2\mathbf{r}^T\mathbf{r} \\ &= J_{\min,p} + \mathbf{H}^T\mathbf{H} + \mathbf{r}^T(\sigma_x^2\mathbf{I} - [\mathbf{P}_{YX}^T \quad \mathbf{0}]\mathbf{R}_e^{-1}\begin{bmatrix} \mathbf{P}_{YX} \\ 0 \end{bmatrix})\mathbf{r} \\ &= J_{\min,p} + \mathbf{H}^T\mathbf{H} + \mathbf{r}^T\mathbf{G}\mathbf{r} \\ &= J_e(\mathbf{H}) \end{aligned} \tag{14}$$

,where $\mathbf{G} = (\sigma_x^2\mathbf{I} - [\mathbf{P}_{YX}^T \quad \mathbf{0}]\mathbf{R}_e^{-1}\begin{bmatrix} \mathbf{P}_{YX} \\ 0 \end{bmatrix}$,

$$\mathbf{H} = (\mathbf{L}^T\mathbf{k} + \mathbf{L}^{-1}\begin{bmatrix} \mathbf{P}_{YX}\mathbf{r} \\ \mathbf{0} \end{bmatrix}). \tag{15}$$

Because the $\mathbf{r}$ is fixed, the MMSE of the PIPEADFE2, $J_{e,\min}$, can be expressed.

$$J_{e,\min} = \underset{\mathbf{k}}{Min}\{J_e(\mathbf{W})\} = \underset{\mathbf{H}}{Min}\{J_e(\mathbf{H})\}, \tag{16}$$

Since $\mathbf{H}^T\mathbf{H} \geq 0$, $J_{e,\min} = J_e(\mathbf{H} = \mathbf{0}) = J_{\min,p} + J_{loss}$. Basically, J_{loss} can be interpreted as the MSE degradation of PIPEADFE2. Here, we define $S_i = \frac{J_{loss}}{\Gamma}$ in order to describe how the inaccuracy index of the estimated channel impulse response, Γ , affect J_{loss} . Since $\mathbf{G}$ is the Hermitian matrix. S_i can be reformulated into the following form.

$$S_i = (\frac{\mathbf{r}^T\mathbf{G}\mathbf{r}}{\mathbf{r}^T\mathbf{r}})\mathbf{V}_p^T\mathbf{V}_p = (\frac{\mathbf{r}^T\mathbf{Q}^T\mathbf{D}_e\mathbf{Q}\mathbf{r}}{\mathbf{r}^T\mathbf{r}})\mathbf{V}_p^T\mathbf{V}_p, \tag{17}$$

where $\mathbf{D}_e$ is the diagonal matrix, and $\mathbf{Q}^T\mathbf{Q} = \mathbf{I}$. From (17), it implies the PIPEADFE2 is most sensitive to the inaccuracy of the estimated channel impulse response when $\mathbf{r}$ =c $\mathbf{q}_{\mathbf{Max}}$, where $\mathbf{q}_{\mathbf{Max}}$ is the eigen-vector corresponding to the maximum eigen-value of $\mathbf{G}$, λ_{MAX} . Therefore, we have the bound of $J_{e,loss}$ as

$$S_{MAX} \cdot \Gamma = \lambda_{MAX} \cdot \Gamma \geq J_{e,\,loss} \geq S_{MIN} \cdot \Gamma = \lambda_{MIN} \cdot \Gamma . \tag{18}$$

S_i can be also interpreted as the sensitivity index of the PIPEADFE2. As long as Γ is under the tolerated range, the output MSE of PIPEADFE2 can be lower than PIPEADFE1. This tolerate range will be explained in the following simulations.

B. Simulation Results of PIPEADFE2

In this subsection, we will show that the output MSE of the proposed PIPEADFE2 can be lower than PIPEADFE1 by the simulation results when the estimated channel impulse response is accurate enough. In addition, we will show the requirement of Γ to grantee that the output MSE of PIPEADFE2 is lower than PIPEADFE1.

1. Simulation I

In the Simulation I, the practical channel impulse response we employ in our simulations is, h=[0.04, 0.05, 0.07, 0.21, 0.5, 0.72, 0.36, 0.21, 0.03, 0.07], which is obtained by the typical response of a good-quality telephone channel [5]. Assume the number of taps in FFF and FBF are N_f =12 and N_b =7, respectively, and the input SNR is equal to 18dB. Using the method in [4], we can calculate the optimal coefficients the first D_1 FBF coefficients for the conventional ADFE, $\mathbf{V}_p^T = [-1.1321, -0.9955, -0.4725]$. Hence, we assume that the first D_1 FBF coefficients of the PIPEADFE2 are $\mathbf{V}_e^T$=[-0.5661 -0.4978 -0.2362], which is obtained by the optimal solution of the roughly estimated channel impulse response in advance. From (12), the inaccuracy of $\mathbf{V}_e^T$, Γ, is equal to 0.25. The learning curves of conventional ADFE, PIPEADFE1, and PIPEADFE2 are depicted in Fig. 3(a), and the three horizontal lines show the theoretical MSE bounds of the conventional ADFE, PIPEADFE1, and PIPEADFE2, respectively. Next, we change the input SNR to 24dB and repeat the simulation, and its simulation results are shown in Fig. 3(b). Based on the simulation results shown in Fig. 3(a)(b), it illustrate the output MSE of the proposed PIPEADFE2 is lower than the PIPEADFE1 when **r**=[0.5661 0.4978 0.2362] in this example.

2.Sumulation II

In the Simulation II, we will show the requirement of Γ to grantee that the output MSE of PIPEADFE2 is lower than PIPEADFE1. From (17), we can see that, as long as $\Gamma \le J_{loss,PIPEADFE1}/S_{MAX}$, the output MSE of PIPEADFE2 is always superior to the PIPEADFE1. We will show this property by a simple example. Basically, we will apply the same parameters and the channel environment like the Simulation I except $\mathbf{r}$. In this example, we will consider the three type of $\mathbf{r}$, which are $\mathbf{r}_1$, $\mathbf{r}_2$, and $\mathbf{r}_3$. ($\mathbf{r}_1$, $\mathbf{r}_2$,and $\mathbf{r}_3$ are $c_1\mathbf{V}_p$, $c_2\mathbf{q}_{\mathbf{Max}}$, and $c_3\mathbf{q}_{\mathbf{Min}}$, respectively.) Then, we will observe their maximum achievable MSE at different Γ by the simulation results and the theoretical results. By the method in [4], the minimum achievable MSE of the PIPEADFE2 is

$$MSE_{\infty,PIPEADFE2} = \frac{J_{e.\min}}{1-\sum_{i=1}^{N_f+N_b-D_1}\mu\lambda_i/(2-\mu\lambda_i)} \tag{19}$$

, where μ is the step size, λ_i is the i-th eigen-value of $\mathbf{R}_e$. The simulation results (dash line) and the theoretical lower bounds (solid line) for each case are shown in Fig. 4. The PIPEADFE1 is the case when $c_1\mathbf{V}_p$ =*0*. Assume the MSE degradation of the PIPEADFE2, $J_{loss,PIPEADFE2} = S_i \cdot \Gamma$, is always lower than the MSE degradation of PIPEADFE1, $J_{loss,PIPEADFE1}$. Based on the simulation results shown in Fig. 4 and (17), the maximum inaccuracy index, Γ, must be smaller than $J_{loss,PIPEADFE1}/S_{MAX} = 0.1442$ in order to grantee that the output MSE of PIPEADFE2 is lower than PIPEADFE1. In other words, $|c_2\mathbf{q}_{\mathbf{Max}}|$ must small than $|0.6\cdot\mathbf{q}_{\mathbf{Max}}|$=|[-0.3751 0.4244 –0.1979]|. However, we may loosen the requirements in the practical situation since $\mathbf{V}_e$ is not always in the direction of $\mathbf{q}_{\mathbf{Max}}$. In practical, since $\mathbf{V}_e$ are often the combination of all orthogonal eigen-vector of $\mathbf{G}$, the designers can store more than one $\mathbf{V}_e$ in the ROM, and select one, that can achieve the lower output MSE.

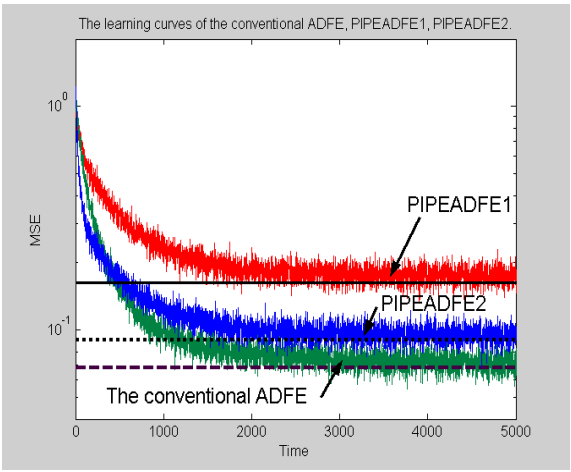
C. Comparisons of Hardware Complexity

Next, we consider the comparisons of hardware complexity between PIPEADFE1 and PIPEADFE2 under the same speedup factor, $N = D_1 + 1$. Since the fixed coefficient adders and slicers in the PPBS can be implemented using an adder, we treat these two components as one slicer. The comparisons between the PIPEADFE1 and PIPEADFE2 with speedup factor=*N* are listed in Table I.

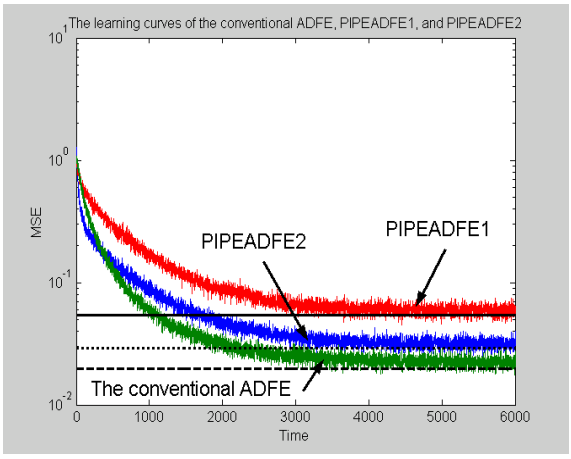
V. Conclusions

In this paper, a new pipelined PPBS-based ADFE using the roughly estimated channel impulse response is

presented. Compared with the algorithm in [3], we show the output MSE of the proposed algorithm can be improved by adding negligible overhead of hardware complexity. It provides an alternative approach for the design of high-seed pipelining ADFE when the output MSE is critical.



(a)



(b)

Fig. 3. The learning curves of the conventional ADFE, PIPEADFE1, and PIPEADFE2 with (a) the input SNR=18dB, (b) the input SNR=24dB.

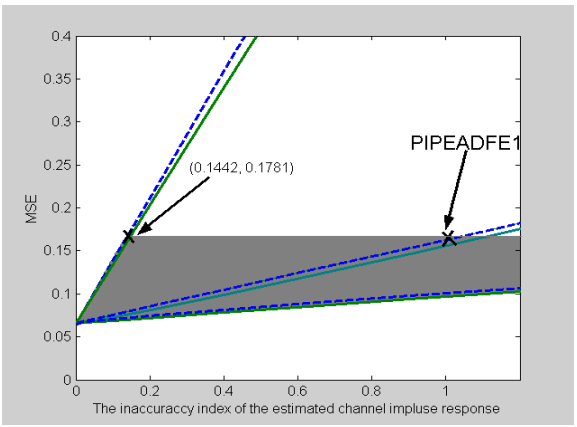


Fig. 4. The output MSE v.s. the inaccuracy index, Γ.

	PIPEADFE1	*PIPEADFE2*
Mult. in FFF	$2N_f$	$2N_f$
Mult. in FBF	$2(N_b - N + 1)$	$2(N_b - N + 1)$
Total adder	$2N_f + 2N_b - 2N$	$2N_f + 2N_b - 2N$
BPSK Slicer	*1*	2^{N-1}
2^{N-1}-to-1 MUX	*0*	2

Table I . Hardware complexity of PIPEADFE1 and PIPEADFE2.

References

[1]K. K. Parhi, VLSI Digital Signal Processing System, Wiley-Interscience, 1999.

[2]K. K. Parhi, "Pipelining in algorithm with quantizer loops," *IEEE Trans. Circ. Syst.*, vol. 38, pp.745-754, July 1991.

[3] Naresh R. Shanbhag and Keshab K. Parhi, "Pipelined adaptive DFE architectures using relaxed look-ahead," *IEEE Trans. Signal Processing,* vol. 43, No. 6, pp. 1368-1385,June 1995.

[4]S. Haykin, *Adaptive Filter Theory*, 2nd Edition, Englewood Cliffs, NJ: Prentice-Hall, 1991.

[5]J. G. Proakis, *Digital Communications*, 4nd Edition, New York: McGraw-Hill, 2001.

[6]G. Long, F. Ling, and J. G. Proakis, "The LMS algorithm with delayed coefficient adaptation," *IEEE Trans. Acoust. Speech Signal Processing,* vol. 37, pp. 1397-1405, Sept. 1989.

[7]B. Widrow and S. D. Stearns, *Adaptive Signal Processing*. Englewood Cliffs, NJ: Prentice-Hall, 1985