Realisation of analogue divider using current feedback amplifiers

S.-I. Liu
J.-J. Chen

Indexing terms: Analogue circuits, Divider circuits

Abstract: New analogue divider circuits using current feedback amplifiers (CFAs) are presented. Basically, they consist of two CFAs, two MOS transistors biased in the triode region, and a resistor. Furthermore, an integrable divider circuit is also presented. Experimental results are given to demonstrate the feasibility of the proposed circuits. The proposed divider will be useful in high-frequency analogue signal processing.

1 Introduction

An analogue divider is an important building block in analogue computation, fuzzy control and instrumentation, etc. [1–3]. Many analogue continuous-time and sampled-data divider circuits have been presented in the literature [4–8]. Most of them have used conventional operational amplifiers as building blocks to synthesise the division function. However, the finite-gain–bandwidth product of the operational amplifiers will limit the high-frequency operation and accuracy of the divider.

Current-mode circuits have been receiving significant attention in analogue signal processing circuits [9]. A new amplifier called the current feedback amplifier (CFA) [10, 11] has been realised to circumvent the finite-gain–bandwidth limitation of the conventional operational amplifier. It can provide not only constant bandwidth independent of the closed-loop gain but also high slew rate (i.e. 2000 V/μs) [11]. It can be also used as a second-generation current conveyor (CCII) [12] by using its compensation node [13]. Moreover, since a CFA was built with a voltage buffer, it can drive external loads easily. In this paper we propose new analogue division circuits using CFAs. Experimental results are also given to verify the theoretical analysis.

2 Circuit description

The simplified equivalent circuit and symbol for a current feedback amplifier (CFA) are shown in Fig. 1*a* and *b*, respectively. This circuit is equivalent to a CCII with a voltage buffer [12]. Its characteristics can be modelled as

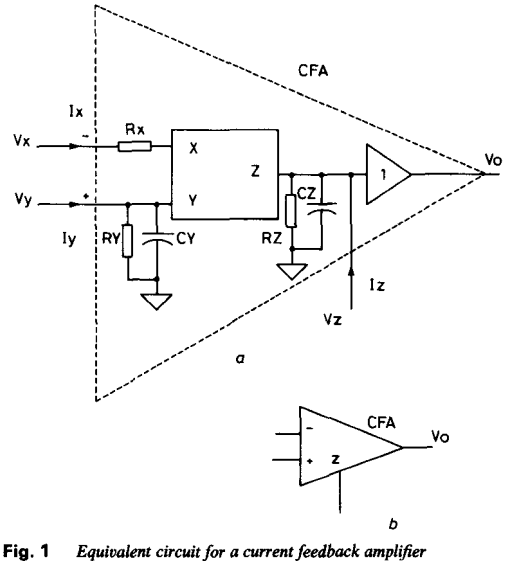


Fig. 1 *Equivalent circuit for a current feedback amplifier*

$$\begin{bmatrix} v_x \\ i_y \\ i_z \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} v_y \\ v_z \\ i_x \end{bmatrix} \quad \text{and} \quad v_o = v_z \tag{1}$$

The proposed analogue division circuit with two CFAs is shown in Fig. 2. It consists of two CFAs, two NMOS transistors biased in the triode region and a resistor. The drain current of an NMOS transistor biased in the triode region can be expressed by [14]

$$I_D = F(V_D, V_G) - F(V_S, V_G) \tag{2}$$

with

$$F(V_X, V_G) = 2K(V_G - V_B - V_{FB} - \phi_B)V_X - K(V_X - V_B)^2 - \tfrac{4}{3}K\gamma(V_X - V_B + \phi_B)^{3/2}$$

$$K = \frac{W}{2L}\mu C_{ox} \quad \gamma = \frac{\sqrt{(2qN_A\varepsilon_s)}}{C_{ox}} \quad V_X = V_D \text{ or } V_S$$

where I_D is the drain current in the triode region, W and L are the channel length and width, respectively, μ is the effective mobility, V_{FB} is the flatband voltage, N_A is the

Paper 1609G (E10), received 23rd February 1994

S.-I. Liu is with the Department of Electrical Engineering, National Taiwan University, Taipei, Taiwan 10664, Republic of China, on leave from the National Taiwan Institute of Technology
J.-J. Chen is with the Department of Electrical Engineering, National Taiwan University, Taipei, Taiwan 10664, Republic of China

substrate doping concentration, C_{ox} is the gate oxide capacitance per unit area, ϕ_B is the approximate surface potential in strong inversion, and V_G and V_B are the gate

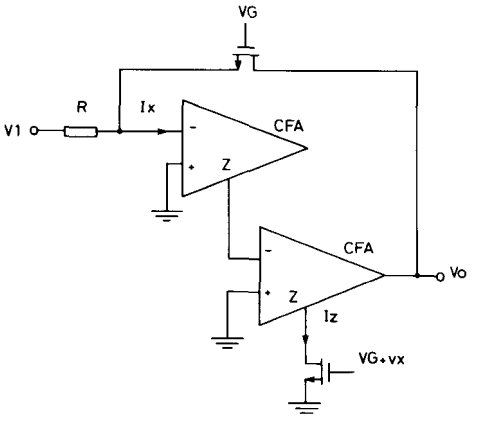


Fig. 2 *Proposed divider circuit*

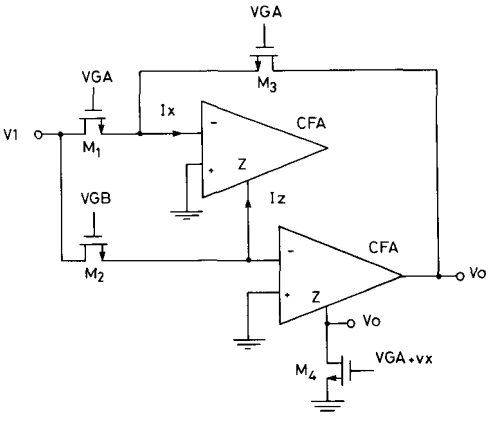


Fig. 3 *Integrable analogue divider circuit*

and substrate voltages, respectively. Let us examine the currents i_x and i_z in Fig. 2. Routine circuit analysis yields

$$i_x = \frac{v_1}{R} + F(v_o, V_G) - F(0, V_G) \tag{3a}$$

$$i_z = F(v_o, V_G + v_x) - F(0, V_G + v_x) \tag{3b}$$

Thus, the output voltage of this divider can be expressed as

$$v_o = \frac{v_1}{2KRv_X} \tag{4}$$

The even and odd nonlinearities of the MOS transistors have been cancelled. To keep the MOS transistor in the triode region, the following condition should be satisfied:

$$\min(V_G, V_G + v_X) > v_o + V_T \tag{5}$$

where V_T is the threshold voltage of the MOS transistor. To consider the stability of the proposed divider circuit, assume that there is a parasitic capacitor C_z at the compensation node Z of the CFA. One can rewrite eqn. 4 as

$$v_o = \frac{v_1}{R(2Kv_X + sC_Z)} \tag{6}$$

Hence, for the divider circuit to be stable, the pole of eqn. 6 should be in the left half-plane (LHP). That is,

$$v_X > 0 \tag{7}$$

Similarly, one can obtain another divider circuit by exchanging the gate voltages V_G and $V_G + v_x$ of Fig. 2. Furthermore we can use MOS transistors biased in the triode region to replace the passive resistor [4, 14, 15]. The proposed integrable divider was shown in Fig. 3. We can express the currents i_x and i_z in Fig. 3 as

$$i_x = F(v_1, V_{GA}) - F(0, V_{GA}) + F(v_o, V_{GA}) - F(0, V_{GA}) \tag{8}$$

$$i_z = F(v_1, V_{GB}) - F(0, V_{GB}) + F(v_o, V_{GA} + v_x) - F(0, V_{GA} + v_x) \tag{9}$$

Routine circuit analysis yields

$$v_o \cong \frac{K_I(V_{GA} - V_{GB})}{K_O v_X} v_1 \tag{10}$$

where K_I is the transconductance parameter of M_1 and M_2 and K_O is that of M_3 and M_4. Because all devices have been assumed to be in the triode region, eqn. 10 only holds when

$$v_1, v_o \leqslant \min[V_{GA} - V_T, V_{GB} - V_T, V_{GA} + v_x - V_T] \tag{11}$$

The proposed divider circuit will be suitable for monolithic integration.

3 Experimental results

The characteristics of a nonideal CFA with the high-impedance input grounded can be given by

$$i_z = \alpha i_x \tag{12}$$

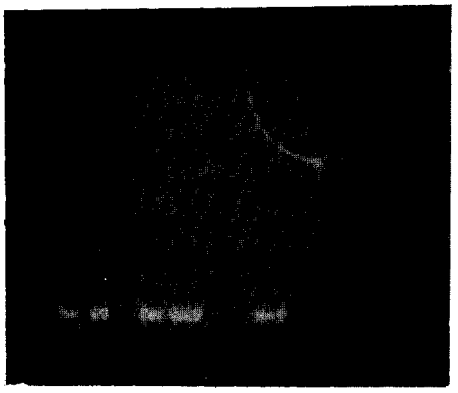
$$v_o = \beta v_z \tag{13}$$

where $\alpha = 1 - \varepsilon_1$ and ε_1 ($\varepsilon_1 \ll 1$) and $\beta = 1 - \varepsilon_2$ and ε_2 ($\varepsilon_2 \ll 1$) denote the current tracking error and voltage tracking error, respectively. Assume that the CFAs in Fig. 2 have the same current transfer ratio α. A detailed analysis for the transfer function of Fig. 2 yields

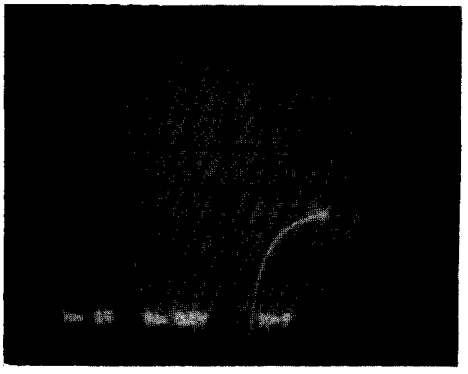
$$v_o \cong \frac{\alpha^2\beta \frac{v_1}{2KR}}{(V_G - V_T)(1 - \alpha^2\beta) + v_X} \tag{14}$$

The current and voltage tracking errors will result in the denominator v_x with an offset voltage in the interesting frequency range. To demonstrate the proposed circuits, we breadboard the circuits by using commercial CFAs (AD844) and CMOS transistor arrays (CD4007). The power supply is ± 12 V, $V_G = 7.8$ V and $R = 5.1$ kΩ. The DC transfer functions were measured and shown in Fig.

4*a* and *b*. The horizontal variable is v_x and the vertical one is v_o. Fig. 4*a* and *b* show the $v_o - v_x$ transfer curve with $v_1 = 1.1$ V and $v_1 = -1.1$ V, respectively. A ramp signal with a positive slope was applied to v_X, and Fig. 5 shows the time domain response of the proposed divider circuit. The frequency response of the proposed divider



a



b

Fig. 4 *Transfer functions*

a DC transfer function (v_o against v_x) of proposed divider circuit with $v_1 = 1.1$ V, $V_G = 7.8$ V and $R = 5.1$ kΩ. Horizontal scale is 1 V/div and vertical scale is 0.2 V/div

b DC transfer function (v_o against v_x) of proposed divider circuit with $v_1 = -1.1$ V, $V_G = 7.8$ V and $R = 5.1$ kΩ. Horizontal scale is 1 V/div and vertical scale is 0.2 V/div

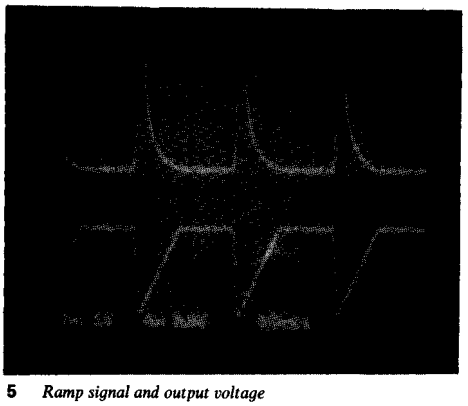
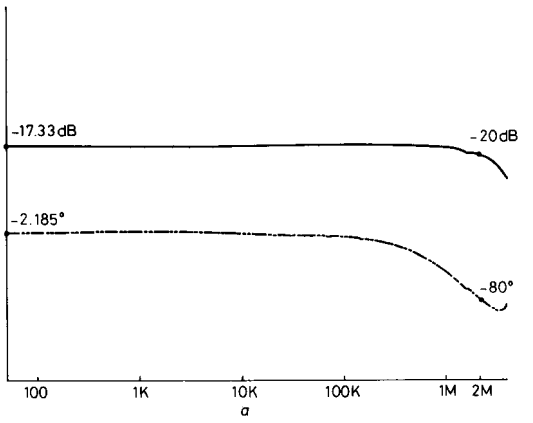
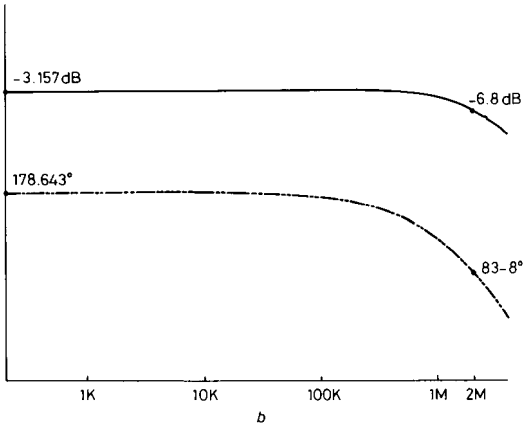


Fig. 5 *Ramp signal and output voltage*

Lower trace (1 V/div) is ramp signal of v_x and upper trace (0.2 V/div) is output voltage V_o of divider. Horizontal scale is 0.5 ms/div



a



b

Fig. 6 *Gain and phase responses*

a Gain (10 dB/div) and phase (45°/div) responses of proposed divider (v_o/v_1) with constant v_x(= 1.1 V). Upper trace is gain response and lower one is phase response

b Gain (10 dB/div) and phase (45°/div) responses of proposed divider (v_o/v_x) with constant v_1(= 1.1 V). Upper trace is gain response and lower one is phase response

circuit was also measured in Fig. 6*a* and *b*. Fig. 6*a* shows the frequency response of v_1 against v_o with $v_x = 1.1$ V. Its −3 dB bandwidth was about 2 MHz. Fig. 6*b* shows the frequency response of v_x against v_o with $v_1 = 1.1$ V. Its −3 dB bandwidth was about 1.8 MHz.

4 Conclusions

New analogue division circuits using CFAs have been proposed. Experimental results are given to demonstrate the feasibility of the proposed circuits. The divider circuit has a simple structure. Frequency responses show that the proposed divider will be useful in high-frequency analogue signal processing applications.

5 References

1 MEAD, C., and ISMAIL, M.: 'Analog VLSI implementation of neural systems' (Kluwer Academic, Boston, 1989)

2 SHEINGOLD, D.H. (Ed.): 'Nonlinear circuit handbook' (Analog Devices, Norwood, MA, 1974)
3 YAMAKAWA, T.: 'High-speed fuzzy controller hardware system: the Mega-FIPS machine', *Inf. Sci.*, 1988, **45**, pp. 113–128
4 KHACHAB, N.I., and ISMAIL, M.: 'A nonlinear CMOS analog cell for VLSI signal and information processing', *IEEE J. Solid-State Circuits*, 1991, **26**, pp. 1689–1698
5 GHOSH, D., and PATRANABIS, D.: 'A simple analog divider having independent control of sensitivity and design condition', *IEEE Trans.*, 1990, **IM-39**, pp. 522–526
6 LAOPPOULOS, TH. L., and KARYBAKAS, C.A.: 'A simple analog division scheme', *IEEE Trans.*, 1991, **IM-40**, pp. 779–782
7 ARONHIME, P., DESAI, M., and STEPHENS, J.: 'Quotient circuits employing VVR', *IEEE Trans.*, 1992, **IM-41**, pp. 679–684
8 LIU, S.I., WU, D.S., TSAO, H.W., WU, J., and TSAY, J.H.: 'Nonlinear circuit applications with current conveyors', *IEE Proc. G*, 1993, **140**, pp. 1–6
9 WILSON, B.: 'Recent developments in current conveyors and current-mode circuits', *IEE Proc. G*, 1990, **137**, (2), pp. 63–77
10 'Linear products data book' (Analog Devices, Norwood, MA, 1990)
11 'Designer's guide for 200 series op amp'. Application note 200-1 (Comlinear Corporation, 4800 Wheaton Drive, Ft. Collins, CO 80525, November 1984)
12 SEDRA, A., and SMITH, K.C.: 'A second generation current conveyor and its applications', *IEEE Trans.*, 1970, **CT-17**, pp. 132–134
13 SVOBODA, J.A., MCGORY, L., and WEBB, S.: 'Applications of a commercially available current conveyor', *Int. J. Electron.*, 1991, pp. 159–164
14 BANU, M., and TSIVIDIS, Y.: 'Detailed analysis of nonlinearities in MOS fully integrated active RC filters based on balanced networks', *IEE Proc. G*, 1984, **134**, pp. 190–196
15 ZARNUL, C.: 'Novel MOS resistive circuit for synthesis of fully integrated continuous-time filters', *IEEE Trans.*, 1986, **CAS-33**, pp. 718–721