Reduction in Leakage Current of Low-Temperature Thin-Gate Oxide by Repeated Spike Oxidation Technique

Chao-Chi Hong, Chang-Yun Chang, Chaung-Yuan Lee, and Jenn-Gwo Hwu, *Senior Member, IEEE*

***Abstract*—A novel repeated spike oxidation (RSO) technique had been used to grow low-temperature thin-gate oxide. Around the similar effective oxide thickness extracted from the capacitance-voltage *(C–V)* curves under quantum mechanical effect consideration, the leakage currents of RSO samples were near one order of magnitude lower than those of typical ones. Flat band voltage shift or electron trapping in RSO oxides during current-voltage *(I–V)* measurement had not been observed. The reduction of interface state densities and the improvement in oxide uniformity would be the possible reasons for the reduction in leakage currents of RSO samples.**

***Index Terms*—Leakage current density, low temperature oxidation, MOS device, repeated spike oxidation.**

I. Introduction

As the channel length of MOSFET is scaled down to deep sub-0.25 μm region, an effective gate oxide thickness below 3 nm is required. [1] It is well known that the leakage current of gate oxide had become a major problem. Leakage current that is too large can cause the device to operate improperly. Many researches had been explored to study the current transport physics [2]–[4]. Various methods had been proposed to reduce the leakage current, such as using H_2-baking[5] and oxynitride gate dielectric [6], etc.

For the purpose of minimizing dopant redistribution, rapid thermal processing (RTP) had been used widely because of its small thermal budget. However, temperature nonuniformity is the major problem in RTP and thus, leads to the gate oxide thickness to be nonuniform when RTP is used for oxidation. On the other hand, ultrathin gate oxide (< 2 nm) was hard to be achieved by RTP under conventional high temperature, e.g., >800 °C, due to the considerable high oxidation rate. Therefore, using a low temperature profile in RTP to grow uniform and good quality ultrathin gate oxide is of interest. We had proposed a new method called repeated spike oxidation (RSO) for RTP system to improve oxide thickness uniformity, which was characterized by setting the oxidation temperature to ramp up and down between two different temperatures, like a trapezoid wave [7]. In this work, the current-voltage *(I–V)* characteristics of RSO oxides were first studied. Surprisingly, the leakage currents of RSO oxides were lower in comparison with those of typical oxides. Possible reasons are also given in this work.

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The authors are with the Department of Electrical Engineering, National Taiwan University, Taipei, Taiwan, R.O.C. (e-mail:hwu@cc.ee.ntu.edu.tw).

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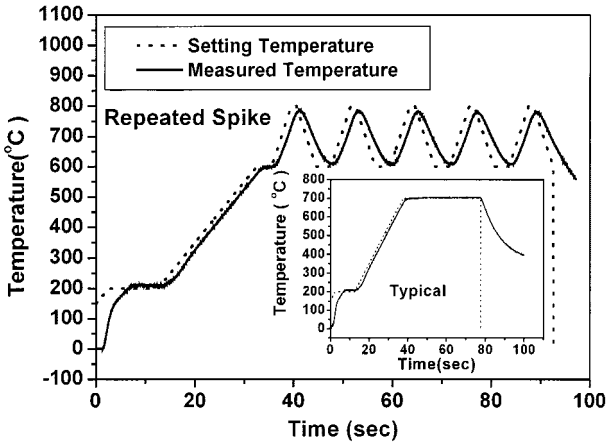

Fig. 1. Temperature setting and measured profiles for the repeated spike recipe and typical case.

II. Experimental

P-type, (100) silicon wafers with a resistivity of $1 \sim 10\,\Omega\cdot$cm were oxidized in RTP after standard RCA cleaning and HF dip. The temperature setting and measured profiles during oxidation for RSO and typical samples are shown in Fig. 1. In the high temperature segment, typical recipe was held at 700 °C and RSO case was set to ramp up and down between 600 ~800 °C. Since the duration of 600 °C was designed to be longer than that of 800 °C, one should notice that RSO had a relatively low average process temperature than that of typical case. The oxygen gas was set to be 80 torr in pressure and was neither purged in nor purged out during oxidation. The typical samples were oxidized using the profile indicated in the inset of Fig. 1 by keeping the temperature at 700 °C for 20, 40, 60, and 90 s. The RSO samples were prepared using the profile shown in Fig. 1 by setting the repeated spikes for three, five, and seven times. The average resulted oxide thickness on 3-in wafer of typical samples were 1.9, 2.3, 2.7, and 3.2 nm, correspondingly, while those of RSO samples were 2.1, 2.7, and 3.0 nm, respectively, which were determined with an ellipsometer by using a refraction index of 1.46. After Al film deposition, MOS capacitors with a size of 150 μm$\times$ 150 μm were formed by photolithography. *I–V* curves were measured with HP 4154 and *C–V* curves with HP 4286.

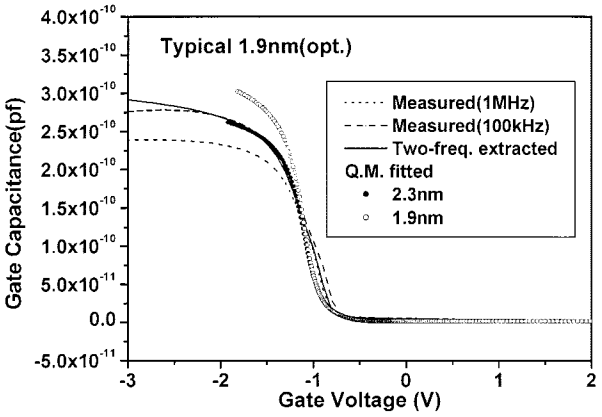

Fig. 2. *C–V* curves for the typical sample having 1.9-nm optical thickness. Measurements were carried out in 1-MHz and 100-kHz frequencies. The curves after two-frequencies extraction and theoretical prediction include quantum-mechanical effect are also shown for comparison.

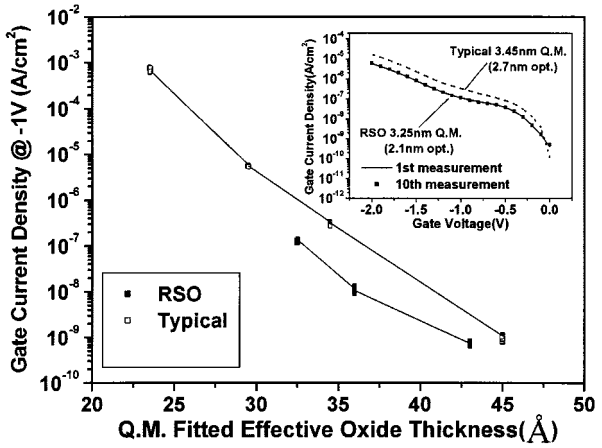

Fig. 3. Comparison of tunneling current densities under -IV bias versus QM fitted effective oxide thickness for RSO and typical samples. The *I–V* curves of 3.45-nm typical sample and those of 3.25-nm RSO samples for the first and tenth measurements are shown in the inset.

III. Results and Discussions

Fig. 2 demonstrates the *C–V* curves of a typical sample with 1.9-nm optical thickness determined with the ellipsometer. *C–V* curves of thin gate oxide exhibit stretch out and thus correction is needed. The two-frequency correction method was applied to our data measured at 1 MHz and 100 kHz by using the theory developed by Yang and Hu [8]. The theoretical curve included quantum-mechanical (QM) correction and was obtained from the program at Berkeley [9]. Although after two frequency correction, the *C–V* curve differs from that of 1.9-nm oxide with quantum mechanical correction prediction theoretically. It was suggested that oxide thickness determined by ellipsometer by setting the refraction index at 1.46 was questionable. The QM fitted effective oxide thickness of the typical sample with 1.9 nm in optical thickness was about 2.3 nm according to the data base obtained from[9]. In order to compare the tunneling current fairly, the ellipsometer measured (optical) thickness of each samples was converted to QM fitted effective oxide thickness using *C–V* curve extraction with quantum-mechanical correction.

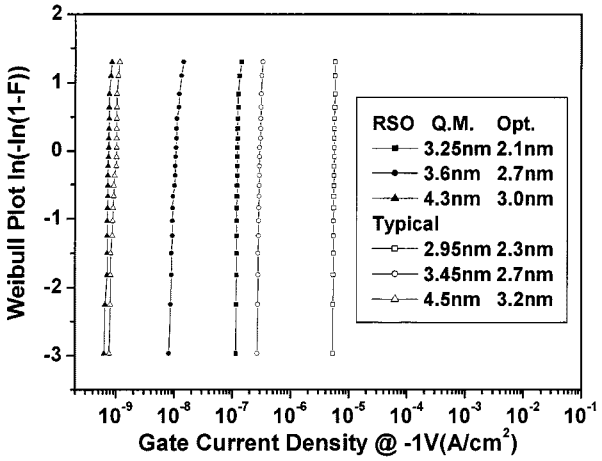

Fig. 4. Weibull plots of tunneling current densities under -IV bias for RSO and typical samples having various QM fitted effective oxide thicknesses.

Fig. 3 illustrates the comparison of tunneling currents between RSO and Typical samples in accumulation region. It was observed that around the similar QM fitted effective oxide thickness, the tunneling currents of RSO samples were near 1 order of magnitude lower than those of Typical samples. The representative *I–V* curves of RSO and Typical samples are shown in the inset of Fig. 3. It should be noted that, the RSO sample was measured for ten times on the same tested device. Since there was very little difference between the first and the tenth measurements, the reduction in tunneling current of RSO samples could not be due to the electron trapping in oxide during *I–V* measurements. The etching rate in 1:100 diluted HF for RSO and Typical samples were 0.16 Å/s and 0.14 Å/s , respectively. So the densities of both samples were about the same and thus, the difference in tunneling current would not be mainly due to intrinsic oxide quality. Fig. 4 shows the comparison of tunneling current in the manner of Weibull plot. The tunneling current magnitude of 3.25-nm RSO sample was even smaller than that of 3.45-nm typical sample, and that of 4.3-nm RSO sample and 4.5-nm typical samples were almost the same. This also led to the conclusion that RSO sample owned relatively lower leakage current.

One of the reasons for the reduction of leakage current in RSO samples might be oxide thickness uniformity. As discussed in our previous work, the radiation heat absorption in two different temperature regions on a wafer could be compensated by RSO technique[7]. Also, the tunneling current magnitude is very sensitive to oxide thickness[10], [11]. A more uniform oxide thickness should result in a smaller leakage for a MOS structure. If device had a local small region which owned a relatively thinner oxide, the magnitude of tunneling current would be increased dramatically [12].

Another reason for the reduction of leakage current in RSO sample could be due to its smaller interface state density. Fig. 5 depicts the *C–V* curves of a RSO and typical samples measured at various frequencies and were normalized by the curves at 1 MHz. First, it should be noticed that the flat band voltages of RSO and typical samples were almost the same. So the reduction of tunneling current of RSO samples was not due to the flat band voltage shift. By examining the *C–V* curves in the depletion region, it could be seen that RSO sample had a less interface

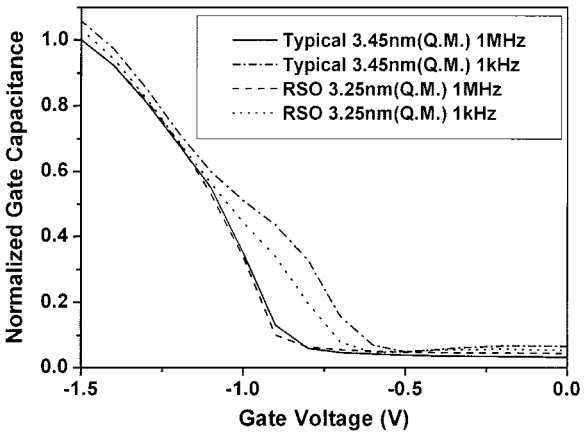

Fig. 5. Normalized *C–V* curves for RSO and typical samples measured at various frequencies.

state density than that of typical one qualitatively. According to the Deal-Grove model, the interface reaction is the rate limitation step during oxidation in thin oxide regime [13]. Besides, the wagging and stretching of Si-O bond are temperature dependent. So, it was possible that during the temperature ramping up and down in RSO recipe, the residual oxygen in oxide layer had more chance to fill the silicon dangling bonds and thus, better interface had been formed. It had been reported that interface state density affected the tunneling current magnitude strongly [14], [15]. The smaller interface state density of RSO sample may contribute to the reduction of it's tunneling current. The interface densities of all samples seemed to be large. This is mainly due to the low oxidation temperature employed in this work. [16], [17].

IV. Conclusion

Thin-gate oxide with low leakage could be prepared by RSO technique. With respect to the conventional one, this new technique had a relatively lower average process temperature. The reduction of tunneling current in RSO sample was not due to the flat band voltage shift or electron trapping during measurement. Experimental results indicated that it was possibly due to the reduction of interface states density. The improvement in oxide thickness uniformity might be another reason. The RSO technique is potential for the preparation of high-quality, low-temperature RTP oxides.

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