Japanese Journal of Applied Physics
Vol. 46, No. 4A, 2007, pp. 1803–1807

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HfO_2/HfAlO/HfO_2 Nanolaminate Charge Trapping Layers for High-Performance Nonvolatile Memory Device Applications

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(Received October 10, 2006; accepted December 26, 2006; published online April 5, 2007)

A high-κ HfO_2/HfAlO/HfO_2 nanolaminate charge trapping layer in a p-Si/SiO_2/[HfO_2/HfAlO/HfO_2 nanolaminate]/Al_2O_3/platinum memory capacitor has been investigated. High-κ HfO_2, Al_2O_3, and HfO_2/HfAlO/HfO_2 nanolaminate charge trapping layers are deposited by atomic layer deposition. Well-behaved counter clockwise capacitance–voltage hysteresis characteristics are observed for all memory capacitors. A large memory window of $\sim$10 V, a very low leakage current density of $\sim 5 \times 10^{-9}$ A/cm^2 at a gate voltage of -5 V, a high charge trapping density of $\sim 1.6 \times 10^{13}$/cm^2, and a low charge loss of $\sim$20% after 10 years of retention for the HfO_2/HfAlO/HfO_2 nanolaminate charge trapping layer are observed as compared with those of pure HfO_2 and pure Al_2O_3 charge trapping layers. Excellent memory characteristics of HfO_2/HfAlO/HfO_2 nanolaminate layers are obtained owing to the layer-by-layer charge storage. High-κ HfO_2/HfAlO/HfO_2 nanolaminate charge trapping layers can be used in future nanoscaled high-performance nonvolatile memory device applications.
[DOI: 10.1143/JJAP.46.1803]

KEYWORDS: high-κ, HfO_2, Al_2O_3, HfAlO, nanolaminate charge trapping, flash, nonvolatile memory

1. Introduction

High-κ dielectrics such as Al_2O_3, La_2O_3, ZrO_2, and HfO_2 are increasing interest for charge trapping nonvolatile memory (NVM) device applications.[1–13] Due to poor retention and scaling issues in polycrystalline silicon–oxide–silicon–nitride–oxide–silicon (SONOS) nonvolatile memory devices,[14] the high-κ charge trapping layer, such as HfO_2[6,7] films in a metal–oxide–high-κ-oxide–silicon structure, is in high demand for future nanoscaled NVM device applications. To further improve the scaling and to increase the program/erase speed, the high-κ dielectric with a large barrier height, such as Al_2O_3[12,13] can also act alternatively as a blocking oxide for high-speed flash memory applications. To obtain high-performance nonvolatile memory devices, HfO_2/HfAlO/HfO_2 nanolaminate charge trapping layers with Al_2O_3 as a blocking oxide in a metal–Al_2O_3–high-κ-SiO_2–Si structure formed by atomic layer deposition (ALD) are investigated for the first time. In this study, good electrical characteristics such as a large memory window, low leakage current, high charge trapping density, and good retention (charge loss $<$ 20% after 10 years of retention) of the HfO_2/HfAlO/HfO_2 nanolaminate charge trapping layer have been observed. Memory characteristics of pure Al_2O_3 and pure HfO_2 in a platinum/high-κ/SiO_2 structure are also investigated for comparison.

2. Experimental Procedure

A p-type silicon (100) wafer with a resistivity of 15–25 Ω·cm was cleaned by dipping in dilute HF for 1 min using the RCA process to remove native oxide from the surface. A high-quality tunneling oxide with a nominal thickness of 3.0 nm was grown using a rapid thermal oxide (RTO) system at a temperature of 1000 °C for 20 s. Then, a high-κ HfO_2 film or HfO_2 (2 nm)/Al_2O_3 (2 nm) nanolaminate charge trapping layers with three periods of HfO_2 ($\sim$2 nm) and two periods of Al_2O_3 ($\sim$2 nm) were deposited on the SiO_2 ($\sim$3 nm)/p-Si substrate by ALD. The total thickness of the pure HfO_2 charge trapping layer or the HfO_2/Al_2O_3 nanolaminate charge trapping layer was $\sim$10 nm. High-κ HfO_2 and Al_2O_3 films were deposited by ALD using hafnium tetrachloride ($HfCl_4$) and tri-methylaluminium [$Al(CH_3)_3$] precursors at a substrate temperature of 300 °C. Then, high-κ Al_2O_3 as a blocking oxide with a thickness of $\sim$10 nm was *in situ* deposited on HfO_2 and HfO_2/Al_2O_3 nanolaminate charge trapping layers. The precursor temperatures were $\sim$185 °C for $HfCl_4$ and $\sim$23 °C for $Al(CH_3)_3$. A pure Al_2O_3 film with a thickness of $\sim$20 nm was also deposited on the SiO_2 ($\sim$3 nm)/p-Si substrate by ALD for comparison. After the deposition of all high-κ films, the post-deposition annealing (PDA) condition was 900 °C for 1 min in N_2 ambient. A platinum (Pt) metal as a gate electrode (area: 1.12×10^{-4} cm^2) was deposited by sputtering using a shadow mask on a high-κ/p-Si substrate. The total thickness (tunneling oxide thickness + charge trapping layer thickness + blocking oxide thickness) of the insulator layer was kept the same ($\sim$23 nm) for all memory capacitors. After deposition of the Pt gate electrode, post-metal-deposition annealing at a temperature of 400 °C for 5 min was performed using N_2 (90%) and H_2 (10%) gases. To probe the thickness of the individual layers after the annealing process, high-resolution transmission electron microscopy (HRTEM) was carried out using a JEM 3000F field emission system at an operating voltage of 300 kV. Microstructural properties of layer-by-layer were characterized by energy-dispersive x-ray spectroscopy (EDS) using a high-angle annular dark-field (HAADF) detector. Electrical properties such as capacitance–voltage (C–V), current density–voltage (J–V), and retention for all memory capacitors were determined using HP 4284A LCR meter and HP4156B semiconductor analyzer systems.

3. Results and Discussion

Figure 1 shows a transmission electron microscopy image

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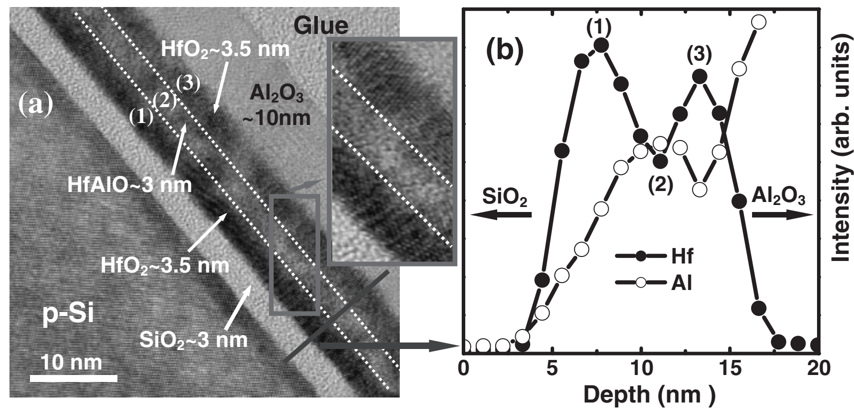

Fig. 1. (a) Typical TEM image of high-κ HfO_2/HfAlO/HfO_2 nanolaminate charge trapping layers with high-κ Al_2O_3 as blocking oxide. A line profile of Hf and Al elements measured by EDS using a HAADF detector shows a clear HfO_2/HfAlO/HfO_2 structure (b).

and an energy-dispersive X-ray spectroscopy line profile of HfO_2/HfAlO/HfO_2 nanolaminate charge trapping layers. An excellent interface of p-Si/SiO_2 or SiO_2/HfO_2 is observed. Both HfO_2 layers have the same thickness of ~3.5 nm, while the thickness of the HfAlO middle layer is ~3 nm. The thicknesses of the tunneling oxide (SiO_2) and blocking oxide (Al_2O_3) are found to be ~3 and ~10 nm, respectively, for pure HfO_2 (not shown here) or the HfO_2/HfAlO/HfO_2 nanolaminate charge trapping layer. The thicknesses of pure HfO_2 and Al_2O_3 charge trapping layers on the SiO_2 (~3 nm)/p-Si substrate are observed to be ~10 and ~20 nm, respectively, at investigated by TEM measurements (not shown here). The HfO_2 film is shown to be fully polycrystalline grain, while the Al_2O_3 film shows a partial crystalline grain. After the PDA treatment, the HfO_2 (~2 nm)/Al_2O_3 (~2 nm) nanolaminate layers show double HfO_2 charge trapping layers with a HfAlO film as a barrier layer [Fig. 1(a)]. It is observed that the Al_2O_3 (~2 nm)/HfO_2 (~2 nm)/Al_2O_3 (~2 nm) middle layers are mixed together after the annealing treatment, resulting in a partially crystalline of the HfAlO layer. Joo *et al.*[11] reported that ZrO_2/Al_2O_3 nanolaminate layers are mixed together after a subsequent thermal process. Figure 1(b) shows concentrations of Hf and Al elements measured by EDS. The numbers for the HfO_2 layers indicated on the curve in Fig. 1(b) correspond to the numbers shown in the TEM image [Fig. 1(a)]. The HfO_2/Al_2O_3 nanolaminate structure shows clear double layers of the HfO_2 films with the HfAlO middle layer after the subsequent thermal process.

Figure 2 shows a well behaved counter-clockwise *C–V* (1 MHz) hysteresis under a gate voltage sweep. A large memory window of ~10 V at $V_g = \pm 15$ V is observed for nanolaminate (HfO_2/HfAlO/HfO_2) memory capacitors due to the layer-by-layer charge storage. After PDA treatment at 900 °C for 1 min in N_2 ambient, the double layers of HfO_2 film have a polycrystalline grain and more charges can be stored on the grain boundary sites. Note that a small memory window of ~3.5 V at $V_g = \pm 15$ V is observed for as-deposited pure HfO_2 films due to the almost amorphous state of HfO_2 films (not shown here). To improve the memory window as well as retention characteristics, the double HfO_2 layers with HfAlO as a barrier layer have been used in this study. The quasi-neutral *C–V* curve (i.e., no charging up or discharging of the memory capacitors) is obtained with a small sweeping gate voltage application of $V_g < \pm 2$ V. The sweep gate voltage step and initial hold time were 0.1 V/s and 3 s, respectively, during the *C–V* measurement for all memory capacitors. A quasi-neutral flat-band voltage (V_{FBN}) is the flat-band voltage from the quasi-neutral *C–V* curve. The V_{FBN} values for Al_2O_3 film, HfO_2 film, and HfO_2/HfAlO/HfO_2 nanolaminate layers are found to be ~0.5, ~0.5, and ~0.8 V, respectively. The capacitance density of the nanolaminate charge trapping layer is very high (>5 fF/μm^2) due to high-κ HfO_2 ($\kappa_{HfO_2} \sim 18$) charge trapping layer and high-κ Al_2O_3 ($\kappa_{Al_2O_3} \sim 9$) blocking oxide. The capacitance equivalent thicknesses (CET) of the Al_2O_3, HfO_2, and HfO_2/HfAlO/HfO_2 nanolaminate charge trapping layers are found to be ~11, ~8, and ~8 nm, respectively. According to the ITRS roadmap, a thin CET of ~10 nm is needed in future nanoscaled SONOS nonvolatile memory device applications. It is indicated that our HfO_2/HfAlO/HfO_2 nanolaminate charge trapping layer can be useful in future nanoscaled high-performance NVM device applications.

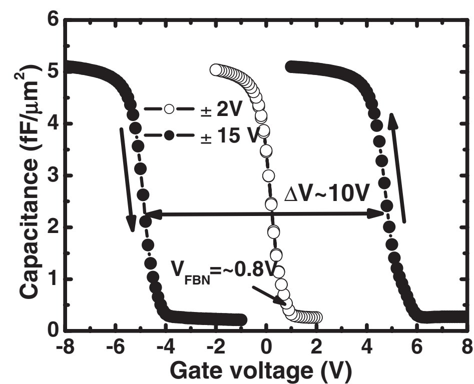

Fig. 2. *C–V* hysteresis memory window of HfO_2/HfAlO/HfO_2 nanolaminate capacitor. The measurement frequency was 1 MHz. The ramp rate was 0.1 V/s during *C–V* measurement.

Figure 3(a) shows the flat-band voltage (V_{FB}) shift versus the positive gate voltage sweep. The V_{FB} shift increases with increasing the positive gate voltage and saturates for all memory capacitors beyond the gate voltage of +12 V. To get at least a ~1 V memory window, a gate voltage of >5 V is

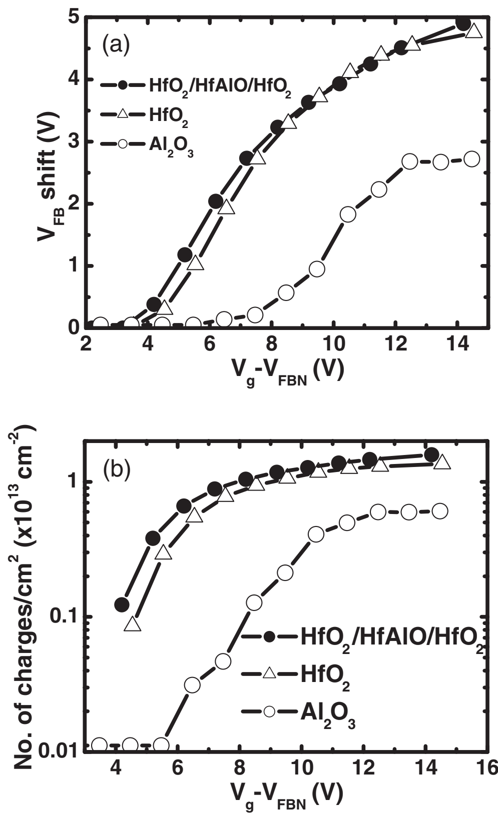

Fig. 3. (a) Flat-band voltage (V_{FB}) shift and (b) charge trapping density vs gate voltage ($V_g - V_{FBN}$) plots for all memory capacitors. The V_{FB} is extracted from C–V hysteresis characteristics.

needed for the pure HfO_2 or $HfO_2/HfAlO/HfO_2$ nanolaminate charge trapping layer, while a large gate voltage of >10 V is needed for the pure Al_2O_3 charge trapping memory capacitors. It can be explained that the conduction band offset of the HfO_2 film with respect to the Si substrate is smaller ($\Delta E_c \sim 1.7$ eV) than that of the Al_2O_3 film ($\Delta E_c \sim 2.8$ eV). The value of the valence band as well as the conduction band offset is confirmed by ultraviolet photoelectron spectroscopy (not shown here). Due to the small $\Delta E_c < 1.7$ eV, more electrons can be injected in the HfO_2 or the $HfO_2/HfAlO/HfO_2$ nanolaminate charge trapping layer from the Si substrate than in the Al_2O_3 charge trapping layer from the Si substrate, because the tunneling current is dominant at the same gate voltage. Maximum positive V_{FB} shifts of the HfO_2 and the $HfO_2/HfAlO/HfO_2$ nanolaminate charge trapping layer are observed to be $\sim$5 V for both capacitors, while a positive V_{FB} shift of the Al_2O_3 charge trapping layer is observed to be $\sim$2.5 V, due to the high density of trapped charges in the HfO_2 film and the $HfO_2/HfAlO/HfO_2$ nanolaminate charge trapping layer [Fig. 3(b)]. A maximum trapped charge density of $N_{charge} > 1.6 \times 10^{13}/cm^2$ is observed for the $HfO_2/HfAlO/HfO_2$ nanolaminate charge trapping layer. The trapped charge density is calculated using the equation: $N_{charge} = C_{ox} \times \Delta V_{FB}$, where C_{ox} is the capacitance at the accumulation region and ΔV_{FB} is the flat-band voltage shift under a positive gate voltage. The charge trapping density of $HfO_2/HfAlO/HfO_2$ nanolaminate layers is high due to the high charge trapping sites and charge storage in layer-by-layer.

Erasing characteristics for all memory capacitors are shown in Fig. 4. Erasing voltages are found to be -8.5 V for pure the HfO_2 or the $HfO_2/HfAlO/HfO_2$ nanolaminate charge trapping layer and -9.5 V for the pure Al_2O_3 charge trapping layer. The higher erasing voltage for the Al_2O_3 charge trapping layer is explained as follow. The valence band offset (ΔE_v) of the high-κ film with respect to the p-Si valence band is found to be $\sim$3.1 eV for the HfO_2 film and $\sim$4.9 eV for the Al_2O_3 film. Due to a small valence band offset of the HfO_2 film or the $HfO_2/HfAlO/HfO_2$ nanolaminate layer, more holes can be injected in the high-κ film than in large-valence-band-offset Al_2O_3 layer, resulting in a lower erasing voltage for the HfO_2 or the $HfO_2/HfAlO/HfO_2$ nanolaminate charge trapping layer. Hysteresis memory windows are found to be $\sim$7 V for the Al_2O_3, $\sim$8 V for the HfO_2 and $\sim$10 V for the $HfO_2/HfAlO/HfO_2$ nanolaminate charge trapping layers under $\pm$15 V gate voltage operation. Note that the erasing saturation of the HfO_2 charge trapping layers is observed after negative gate voltage of -12 V, and this is due to the higher leakage current of the HfO_2 charge trapping layer (Fig. 5). The leakage current and breakdown voltage (-16 V) of the HfO_2 charge trapping layer being higher and lower than those of the Al_2O_3 memory capacitor, respectively, are observed due to the small band gap energy (E_g) of the HfO_2 film [$E_{g(HfO_2)} \sim 5.9$ eV versus $E_{g(Al_2O_3)} \sim 8.8$ eV]. Joo et al.[11] reported that ZrO_2/Al_2O_3 nanolaminate layers have a lower leakage current than pure ZrO_2 films after the subsequent thermal process. The leakage current and breakdown voltage

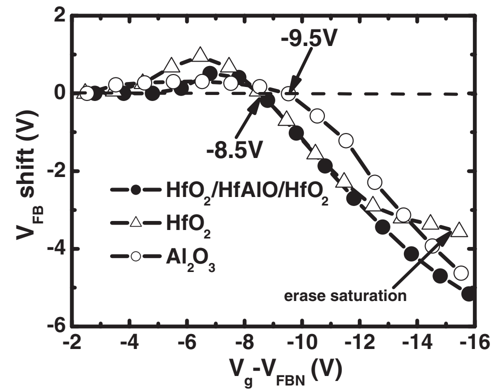

Fig. 4. Erasing characteristics for all memory capacitors.

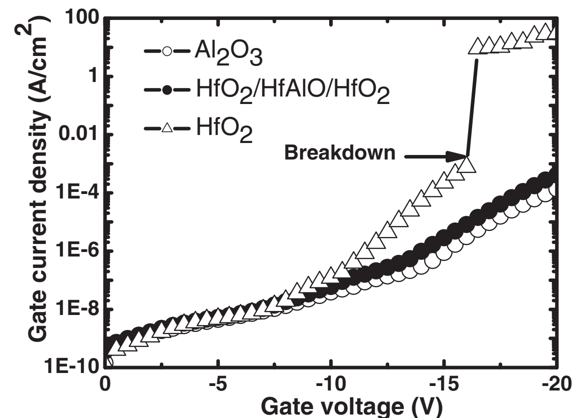

Fig. 5. Leakage current characteristics for all memory capacitors.

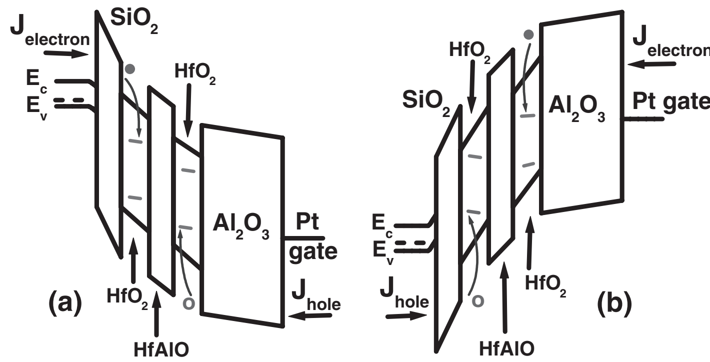

Fig. 6. Schematic energy band diagram of high-κ HfO_2/HfAlO/HfO_2 nanolaminate charge trapping layers with high-κ Al_2O_3 as blocking oxide and SiO_2 as a tunneling oxide under (a) program mode and (b) erase mode of HfO_2/HfAlO/HfO_2 nanolaminate memory capacitors.

(<-20 V) of HfO_2/HfAlO/HfO_2 nanolaminate layers are similar to those of the Al_2O_3 memory capacitors, due to the HfAlO barrier layer design. Therefore, the HfO_2/HfAlO/HfO_2 nanolaminate charge storage capacitor can be operated at a large gate voltage of up to 20 V.

A schematic band diagram of double HfO_2 charge storage layers under program/erase mode is shown in Fig. 6. Note that the difference of the injection current densities ($J_{electron} - J_{hole}$) must be higher to program/erase more easily. J_{hole} should be zero during program mode and $J_{electron}$ should be zero during erase mode. To reduce the leakage current and to improve the charge retention, the HfAlO barrier layer between the double HfO_2 charge trapping layers is designed. To investigate the charge loss characteristics, all memory capacitors are charged using $V_{FB} - V_{FBN} = +6$ V for 60 s. Then, the capacitance is measured under a gate voltage of $V_{FB} - V_{FBN} = -1.5$ V. A normalized capacitance versus time is shown in Fig. 7(a). The HfO_2/HfAlO/HfO_2 nanolaminate charge storage layer has similar charge loss compared with the Al_2O_3 layers. Figure 7(b) shows the retention characteristics for all memory capacitors. At first, all memory capacitors are programmed under a gate voltage of $+15$ V for 10 s. Then, the capacitance is measured with the sweeping voltage of $+5.5$ to $+3$ V for certain time intervals. The V_{FB} values are calculated from the C–V characteristics. Then, the V_{FB} values are plotted against time. Similarly, the capacitance is measured with the sweeping voltage of $+1$ to -1 V for certain time intervals after erasing the memory capacitors. The memory capacitor was grounded during the V_{FB} measurement. An excellent retention is observed for a 10 year projection of the HfO_2/HfAlO/HfO_2 nanolaminate memory capacitors. A large memory window is found to be $\sim$3.2 V after 10 years of retention (inset of Fig. 7). Due to the large memory window of the HfO_2/HfAlO/HfO_2 nanolaminate device, it can be used in multilevel charge (MLC) storage for high-density flash memory applications. The normalized memory window of the HfO_2 charge trapping layer decreases with time as compared with that of the Al_2O_3 charge trapping layer because the HfO_2 has shallow level traps and the Al_2O_3 film has deep level traps.[6] The HfO_2/HfAlO/HfO_2 memory devices have a charge loss ($\sim$20%) and a normalized memory window similar to those of the pure Al_2O_3 charge trapping memory devices due to the layer-by-layer charge storage.

4. Conclusions

Memory characteristics of the HfO_2/HfAlO/HfO_2 nanolaminate charge trapping layer have been investigated. A large memory window, high charge trapping density, and low charge loss are observed for the HfO_2/HfAlO/HfO_2 nanolaminate charge trapping layer. The HfO_2/HfAlO/HfO_2 nanolaminate charge trapping layer paves the way for future high-performance nonvolatile memory device applications.

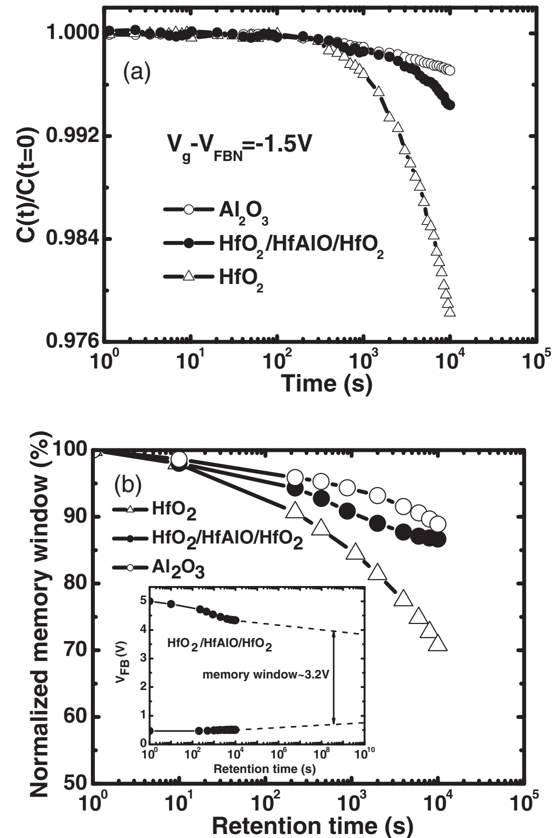

Fig. 7. (a) Discharge characteristics and (b) normalized memory windows of all memory devices. The retention of high-κ HfO_2/HfAlO/HfO_2 nanolaminate charge trapping layers is also shown in the inset of (b).

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