Early detection of successful decoding for dual-diagonal block-based LDPC codes

C.-Y. Lin and M.-K. Ku

A fast, successful decoding detection mechanism is proposed for dual-diagonal block-based low-density parity-check (LDPC) codes. The algorithm eliminates unnecessary parity check computation by exploiting the structure of dual-diagonal LDPC codes. The average number of decoding iterations can be reduced for both two-phase decoders and layered decoders with no performance degradation on the AWGN channel. Simulation results show that the proposed mechanism reduces average iterations by 10–15% at 10^{-5} bit error rate compared with standard parity-check equations.

Introduction: Low-density parity-check (LDPC) codes [1] have attracted much attention in the last decade owing to their capacity-approaching performance. LDPC codes with a dual-diagonal block-based structure can be encoded in linear time with lower encoder hardware complexity [2]. This class of LDPC codes is adopted by a number of standards such as wireless LAN (IEEE 802.11n) [3], wireless MAN (IEEE 802.16e, WiMAX) [4] and satellite TV (DVB-S2) [5]. LDPC codes are commonly decoded by the iterative belief-propagation (BP) algorithm. The decoder checks the parity-check equations to detect successful decoding at the end of the iteration. The Tanner graph of an irregular LDPC code consists of nodes with different degrees such that coded bits have unequal error protection [6]. Coded bits associated with higher degree nodes tend to converge to the correct answer more quickly. Hence, in order to give better protection to the transmitted data, data bits are always mapped to higher degree nodes whereas parity bits are mapped to lower degree nodes in the encoding process.

The commonly used parity-check equations $\boldsymbol{H}\boldsymbol{c}^t = 0^t$ will be satisfied after all the coded bits are correctly decoded. However, as discussed above, data bits converge to the correct answer much more quickly than parity bits, so some unnecessary iterations are wasted waiting for the parity bits to be decoded. In this Letter, a new set of low-complexity check equations are derived for dual-diagonal block-based LDPC codes. Early detection of successfully decoded data can be achieved by exploiting the structure and degree of distribution of the dual-diagonal parity check matrix. The decoder power, speed and complexity can be improved by adopting these equations. Simulation shows that the coding gain performance is little changed.

Dual-diagonal block-based LDPC codes: The dual-diagonal block-based matrix $\boldsymbol{H}$ of size $m \times n$ in IEEE 802.11n and 802.16e is defined as

$$\boldsymbol{H} = [(\boldsymbol{H}_s)_{m\times k}|(\boldsymbol{H}_p)_{m\times m}] = \begin{bmatrix} P_{0,0} & P_{0,1} & P_{0,2} & \cdots & P_{0,n_b-1} \\ P_{1,0} & P_{1,1} & P_{1,2} & \cdots & P_{1,n_b-1} \\ P_{2,0} & P_{2,1} & P_{2,2} & \cdots & P_{2,n_b-1} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ P_{m_b-1,0} & P_{m_b-1,1} & P_{m_b-1,2} & \cdots & P_{m_b-1,n_b-1} \end{bmatrix} \quad (1)$$

where $\boldsymbol{H}_s$ corresponds to data bits and $\boldsymbol{H}_p$ corresponds to parity bits. $\boldsymbol{P}_{i,j}$ is either a circulant permutation matrix or a zero matrix of size z. A circulant permutation matrix is formed by circularly shifting the rows of an identity matrix to the right by several times. The matrix $\boldsymbol{H}$ is expanded from a base matrix $\boldsymbol{H}_b$:

$$\boldsymbol{H}_b = [(\mathbf{H}_{b_s})_{m_b\times k_b}|(\boldsymbol{H}_{b_p})_{m_b\times m_b}] \quad (2)$$

where $m_b = m/z$ and $k_b = k/z$. Each element in $\boldsymbol{H}_b$ is a nonnegative number or -1 to represent the shift quantity of the permutation matrix or a zero matrix. The structure of $\boldsymbol{H}_{bp}$ is further defined as

$$\boldsymbol{H}_{b_p} = [(\boldsymbol{t})_{m_b\times 1}|(\boldsymbol{h})_{m_b\times(m_b-1)}] = \begin{bmatrix} 0 & & & & & & \\ d & 0 & 0 & & & & \\ & & 0 & \ddots & & & \\ 0 & & & \ddots & \ddots & & \\ & & & & \ddots & 0 & \\ & & & & & 0 & 0 \\ d & & & & & & 0 \end{bmatrix} \quad (3)$$

where $\boldsymbol{t}$ is a weight-3 column and $\boldsymbol{h}$ is a dual-diagonal structure (note that d is a positive number and all blank entries are elements of -1). By exploiting this structure, the codeword can be encoded recursively in linear time and the encoder complexity can be reduced significantly.

Proposed early detection mechanism for successful decoding: Let $\boldsymbol{s} = [a_0\ a_1 \cdots a_{k-1}]$ denote the data block and $\boldsymbol{s_i} = [a_{iz}\ a_{iz+1} \cdots a_{(i+1)z-1}]$ for $i = 0, 1, \ldots, k_b - 1$ denote the data sub-block. Also, let $\boldsymbol{p} = [b_0\ b_1 \cdots b_{m-1}]$ denote the parity block and $\boldsymbol{p_i} = [b_{iz}\ b_{iz+1} \cdots b_{(i+1)z-1}]$ for $i = 0, 1, \ldots, m_b - 1$ denote the parity sub-block. All operations discussed below are modulo-2 operations. By definition, a valid codeword $\boldsymbol{c} = [\boldsymbol{s}|\boldsymbol{p}]$ must satisfy the following equations:

$$\boldsymbol{H}\boldsymbol{c}^t = [(\boldsymbol{H}_s)_{m\times k}|(\boldsymbol{H}_p)_{m\times m}][s|p]^t = 0^t \quad (4)$$

Replacing $\boldsymbol{H}_s$ and $\boldsymbol{H}_p$ by the dual-diagonal matrix definition, we get

$$\begin{bmatrix} P_{0,0} & P_{0,1} & P_{0,2} & \cdots & P_{0,k_b-1} \\ P_{1,0} & P_{1,1} & P_{1,2} & \cdots & P_{1,k_b-1} \\ P_{2,0} & P_{2,1} & P_{2,2} & \cdots & P_{2,k_b-1} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ P_{m_b-1,0} & P_{m_b-1,1} & P_{m_b-1,2} & \cdots & P_{m_b-1,k_b-1} \end{bmatrix} \times \begin{bmatrix} s_0^t \\ s_1^t \\ s_2^t \\ \vdots \\ s_{k_b-1}^t \end{bmatrix} + \left[\begin{array}{c|ccccc} \boldsymbol{I_d} & I & & & & \\ & I & I & & & \\ & & I & \ddots & & \\ \boldsymbol{I} & & & \ddots & \ddots & \\ & & & & \ddots & I \\ & & & & & I \\ \boldsymbol{I_d} & & & & & I \end{array}\right] \begin{bmatrix} p_0^t \\ p_1^t \\ p_2^t \\ \vdots \\ p_{m_b-1}^t \end{bmatrix} = 0^t \quad (5)$$

where $\boldsymbol{I}$ is the identity matrix and $\boldsymbol{I_d}$ is the circulant permutation matrix with d-position right shifting. After submatrix and sub-block multiplication, we obtain

$$\begin{bmatrix} \sum_{j=0}^{k_b-1} \boldsymbol{P}_{0,j}\boldsymbol{s}_j^t \\ \sum_{j=0}^{k_b-1} \boldsymbol{P}_{1,j}\boldsymbol{s}_j^t \\ \vdots \\ \sum_{j=0}^{k_b-1} \boldsymbol{P}_{m_b-1,j}\boldsymbol{s}_j^t \end{bmatrix} + \begin{bmatrix} (p_0)_d^t + p_1^t \\ p_1^t + p_2^t \\ \vdots \\ p_{x-1}^t + p_x^t \\ p_0^t + p_x^t + p_{x+1}^t \\ p_{x+1}^t + p_{x+2}^t \\ \vdots \\ p_{k_b-2}^t + p_{k_b-1}^t \\ (p_0)_d^t + p_{k_b-1}^t \end{bmatrix} = 0^t \quad (6)$$

where $(\boldsymbol{p}_0)_d$ is $\boldsymbol{p}_0$ with d-position left shifting. By summing all m_b rows in (6), we obtain the following equations:

$$\sum_{i=0}^{m_b-1}\sum_{j=0}^{k_b-1} P_{i,j}s_j^t + p_0^t = 0^t \quad (7)$$

The z equations in (7) can be used to replace the standard parity-check equations to detect successful decoding with all data blocks and only one parity block participating in the check. All parity bits corresponding to degree-2 nodes in the Tanner graph (equivalently, weight-2 columns in $\boldsymbol{H}$) are excluded from the equations. Once all data bits are successfully decoded, the decoder can stop immediately without waiting for the remaining parity bits to converge. The proposed method requires a slightly lower number of shifting and XOR operations than the original parity-check equations to declare successful decoding. The mechanism can be applied to irregular repeat accumulate (IRA) codes, such as codes in the DVB-S2 standard [5] or OFDM-based UWB systems [7].

Results: A BP decoder combined with the proposed early detection method is compared with standard parity-check equations. Three codes defined in IEEE 802.16e with different code rates (1/2, 3/4) and block lengths (2304, 576) are used in the simulation. All results are simulated on the binary-input AWGN channel. Fig. 1 shows the results of layered BP decoding, which converges twice as fast as two-phase decoding [8], with a maximum of 15 iterations. As shown in

Fig. 1*a*, the proposed early detection mechanism achieves the same bit error rate (BER) performance as the standard parity-check equations. Fig. 1*b* compares the average number of iterations to declare a block successfully decoded. The proposed mechanism requires 10–15% fewer iterations than the standard parity-check equations at BER $= 10^{-5}$. The iteration reduction is greater for higher SNR situations. Simulation results show that applying our algorithm to two-phase decoding exhibits similar iteration reduction.

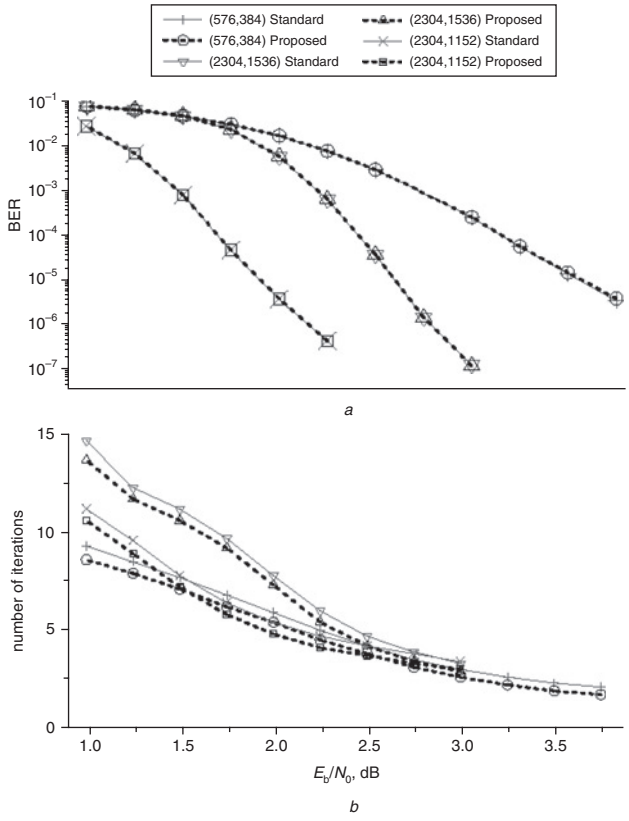

Fig. 1 *Performance of layered decoding algorithm*

a Bit error rate
b Average number of iterations to declare block successfully decoded

Conclusions: A novel stopping mechanism for dual-diagonal block-based LDPC codes is proposed for a standard iterative BP decoder. The proposed check equations exclude all parity bits corresponding to degree-2 nodes for the dual-diagonal portion in the matrix. Simulations show that the average number of iterations can be reduced by 10–15% at the operating point with no performance loss. The application of this mechanism reduces LDPC decoder power consumption at no coding gain and hardware complexity cost.

31 July 2008
Electronics Letters online no: 20082236
doi: 10.1049/el:20082236

C.-Y. Lin and M.-K. Ku (*Department of Computer Science and Information Engineering, National Taiwan University, Taipei, Taiwan 106, Republic of China*)

E-mail: f93084@csie.ntu.edu.tw

References

1 Gallager, R.G.: 'Low-density parity-check codes' (MIT Press, Cambridge, MA, USA, 1963)
2 Cai, Z., Hao, J., Tan, P.H., Sun, S., and Chin, P.S.: 'Efficient encoding of IEEE 802.11n LDPC codes', *Electron. Lett.*, 2006, **42**, (25), pp. 1471–1472
3 IEEE P802.11n/D2.00: 'Draft standard for local and metropolitan area networks, specific requirements Part 11: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) specifications: enhancements for higher throughput', February 2007
4 IEEE Std 802.16e-2005: 'IEEE standard for local and metropolitan area networks Part 16: Air interface for fixed and mobile broadband wireless access systems', February 2006
5 European Telecommunications Standards Institute (ETSI): 'Digital video broadcasting (DVB) second generation framing structure for broadband satellite applications; EN 302 307 V1.1.1', www.dvb.org
6 Li, Y., and Ryan, W.E.: 'Bit-reliability mapping in LDPC-coded modulation systems', *IEEE Commun. Lett.*, 2005, **9**, (1), pp. 1–3
7 Brack, T., Alles, M., Lehnigk-Emden, T., Kienle, F., Wehn, N., Berens, F., and Ruegg, A.: 'A survey on LDPC codes and decoders for OFDM-based UWB systems'. Proc. IEEE 65th Vehicular Technology Conf. (VTC2007-Spring), April 2007, pp. 1549–1553
8 Goldberger, J., and Kfir, H.: 'Serial schedules for belief-propagation: analysis of convergence time', *IEEE Trans. Inf. Theory*, 2008, **54**, (3), pp. 1316–1319