A BiCMOS Dynamic Divider Circuit Using a Non-Restoring Iterative Architecture with Carry Look Ahead for CPU VLSI

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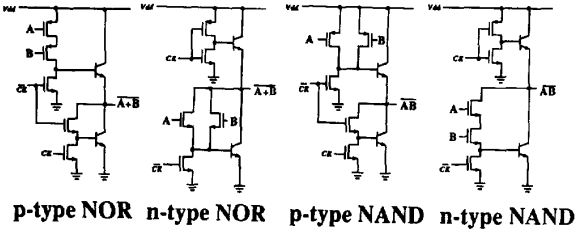
Abstract

This paper presents a race-free BiCMOS dynamic divider circuit using a non-restoring iterative architecture with carry look ahead. Using the BiCMOS dynamic circuit, an 8-bit÷ 4-bit divider test circuit, designed based on a $2\mu m$ BiCMOS technology, shows a more than 4.5 times improvement in speed as compared to the CMOS divider circuit. The speed advantage of the BiCMOS dynamic divider circuit is even greater in a 64-bit divider, which is helpful for CPU VLSI.

Summary

Division is an important function in a CPU arithmetic unit [1]. VLSI implementation of divider circuits using CMOS technologies has been reported [2]-[6]. However, as the size is large, CMOS divider circuits may suffer from long delays. Recently, BiCMOS technology is becoming a major tool for building microprocessors [7]-[10]. BiCMOS buffers have been used to provide a large driving capability to enhance speed performance. However, BiCMOS dynamic digital circuits are still difficult to design due to their serious race problems [11]. Recently, race-free BiCMOS dynamic circuits for a full adder and a multiplier using BiCMOS dynamic carry look ahead circuits have been reported [12]-[14]. In this paper, based on a non-restoring iterative architecture [15] and BiCMOS dynamic circuit techniques, a BiCMOS dynamic divider circuit is described.

Figs. 1 show the basic BiCMOS dynamic logic gates used in the divider circuit. As shown in Fig. 1, depending on the precharge or predischarge scheme, the BiCMOS dynamic logic gates are classified as n-type or p-type. For the p-type BiCMOS logic gates, initially, during the predischarge period, the clock signal is low (CK=0), and the output node is pulled down low by the lower bipolar device. During the predischarge period, the upper bipolar device is turned off by the NMOS device controlled by the signal $\overline{CK}$. After the predischarge period, it's the logic evaluation period. During the logic evaluation period, the lower bipolar device is turned off by the NMOS device controlled by the signal CK. During the logic evaluation period, the output may be pulled high by the upper bipolar device depending on the states of the input signals. Contrary to p-type gates, n-type BiCMOS dynamic logic gates have a complementary mechanism. During the precharge period, the output of them is pulled up to close to 5V. In the logic evaluation period, the output may be pulled down depending on the states of the inputs.



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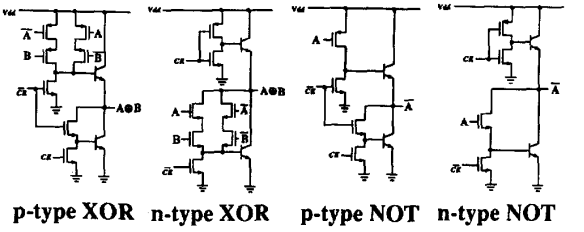
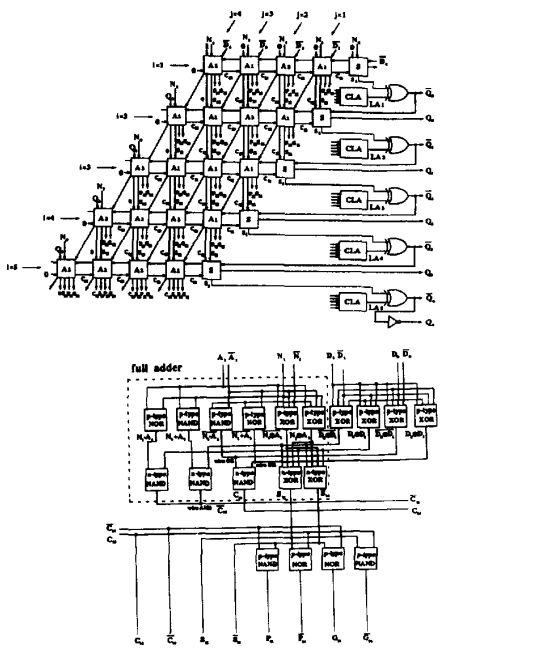


Fig. 1 P-type and n-type BiCMOS dynamic logic gates.
(a) p-type NOR (b) n-type NOR (c) p-type NAND (d) n-type NAND
(e) p-type XOR (f) n-type XOR (g) p-type NOT (h) n-type NOT.

Using the BiCMOS dynamic logic gates, an 8-bit÷4-bit divider circuit based on a non-restoring iterative architecture [15] with carry-look-ahead as shown in Fig. 2 has been designed. As shown in Fig. 2(a), different from the standard non-restoring divider structure, two types of A cells – A1, A2 are needed. Both A1 and A2 cells have an identical structure as shown in the upper portion of Figs. 2(b)&(c). However, in the lower portion, the propagate and generate signals are produced by different types of BiCMOS dynamic digital circuits. Specifically, in the A1 cell, the propagate and generate signals (P, $\bar{P}$, G, $\bar{G}$) are



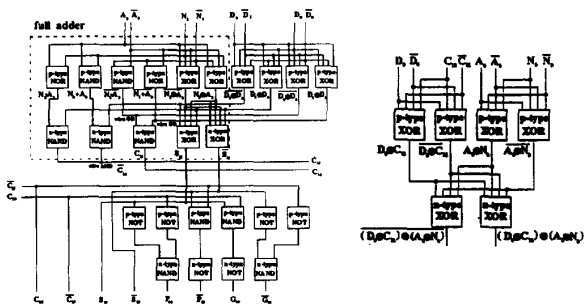
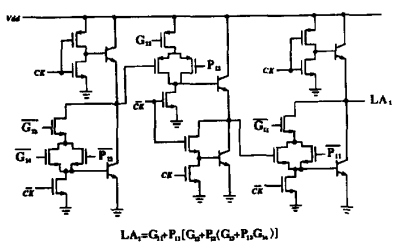


Fig. 2 The 8-bit÷4-bit BiCMOS dynamic divider circuit using a non-restoring architecture with carry-look-ahead. (a) block diagram. (b) A1 cell circuit. (c) A2 cell circuit. (d) S cell circuit.

produced by the p-type BiCMOS dynamic logic gates. On the other hand, in the A2 cell, they are from the n-type BiCMOS dynamic logic gates. Different types of BiCMOS dynamic logic gates used here are for the carry look ahead circuit. Fig. 3 shows the BiCMOS dynamic carry look ahead circuit used in the divider circuit. In the BiCMOS dynamic



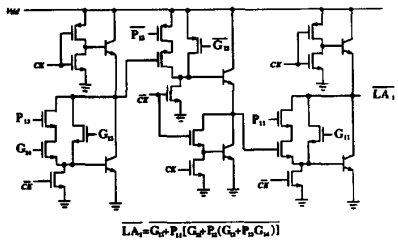


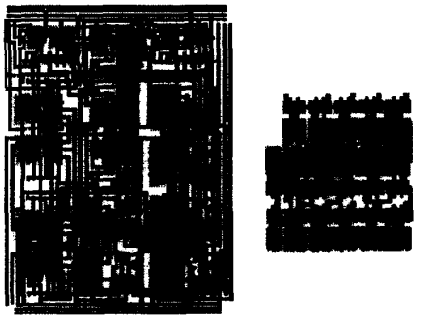
Fig. 3 The BiCMOS dynamic CLA circuit used in the divider circuit.

carry look ahead circuit, all pass transistors in the standard Manchester CLA circuit [16] are replaced by the cascading BiCMOS dynamic logic gates. Each BiCMOS dynamic logic gate's output - the carry signal, is taken as input to another logic gate. In order to shorten the precharge/predischarge time, BiCMOS precharge/predischarge circuits have been used in every cell. Using the BiCMOS dynamic Manchester CLA circuit, the speed performance has been greatly improved owing to the large driving capability of the bipolar device. In addition, no race problems exist in the circuit. Furthermore, it has a very nice expansion capability as the carry look ahead chain is long for a large size divider.

As in a pipelined system, cascading dynamic logic gates may have serious race problems [11]. In the new BiCMOS dynamic divider circuit, race problems have been avoided by placing the "complementary" BiCMOS dynamic cells as shown in Fig. 3 alternatively in the CLA circuit, where an n-p-n set of logic gates have been placed. In the n-type BiCMOS dynamic logic gate, one transition state is prohibited at the input. Specifically, in the n-type BiCMOS dynamic logic gate, inputs cannot have a transition state from $5V$ to $0V$ since the output may be accidentally switched to an incorrect state. Similarly, in the p-type logic gate, inputs cannot have a transition state from $0V$ to $5V$. Overall, the n-type and p-type logic gates are placed alternatively in the BiCMOS divider circuit such that the output of an(a) n(p)-type logic gate and is also the input to a(an) p(n)-type one. After the precharge/predischarge period, in the BiCMOS dynamic divider circuit, each internal output node is set high and low alternatively. In the BiCMOS divider circuit, the n-p-n-p arrangement rule has been observed in the CLA circuit. It's also honored in the A1, A2, and S cells. In addition, between the cells, in the vertical and lateral direction along the signal propagation path as shown in Fig. 2, it has been always observed. With this arrangement, race problems are successfully avoided in our circuit.

In designing the BiCMOS dynamic circuit, in order to honor the n-p-n-p arrangement rule to avoid race problems, a difficult situation has been encountered. The difficulty arises around the final p-type EXCLUSIVE-OR gate to produce the quotient bit in every row in Fig. 2. As shown in Fig. 1(a), to realize the dynamic EXCLUSIVE-OR gate,

two pairs of complementary signals from the CLA cell and the S cell are necessary. Specifically, two complementary signals LA and $\bar{LA}$ are needed at the output of the CLA circuit simultaneously. In order to abide by the n-p-n-p arrangement rule, the final stage of the CLA cells involved has to be n-type logic gates since the final EXCLUSIVE-OR gate is p-type. The inputs to the CLA cell are the propagate and generate signals from both the A1 and A2 cell in the same row as shown in Fig. 2. However, to have two complementary signals from the outputs of the same type of dynamic gate at the same time, observing the n-p-n-p arrangement rule, is very difficult. To overcome the difficulty, two n-p-n dynamic logic circuits have been placed in CLA circuit as shown in Fig. 3. In addition, appropriate complementary propagate and generate signals, which are generated from the same type of logic gates in the A1 and A2 cells have been used as inputs to their allowable inputs to the specific logic gates in the CLA. Furthermore, the A1 and A2 cells have been designed such that their associated propagate and generate signals connected to the same type of logic gate in the CLA cell are from their appropriate logic gates. Specifically, both sets of signals – $P_{13}\&\bar{P}_{13}\&$ $G_{13}\&\bar{G}_{13}$ and $P_{14}\&\ \bar{P}_{14}$, which are connected to the inputs to the first n-type logic gate in the CLA circuit, are from p-type logic gates in adjacent A1 and A2 cells. G_{12}, $\bar{G}_{12}$, P_{12}, $\bar{P}_{12}$, which are produced by the n-type logic gates in an A2 cell, are connected to the inputs to the middle p-type logic gate in the CLA circuit. $P_{11}, \bar{P}_{11}, G_{11}, \bar{G}_{11}$, which are produced by the p-type logic gates in the A1 cell, are used as inputs to the final n-type logic gate in the CLA circuit. By this arrangement for A1, A2, and CLA cells, complementary signals LA and $\bar{LA}$ have been successfully generated from the n-type logic gates simultaneously for the p-type final EXCLUSIVE-OR gate without race problems. Overall, following the n-p-n-p arrangement rule for the BiCMOS dynamic logic gates in all signal propagate direction in the divider circuit, either vertically from top to bottom, or from left to right, race problems have been smoothly avoided in the BiCMOS dynamic divider circuit.



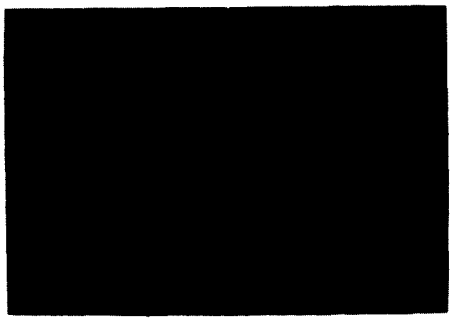


Fig. 4 (a) Layout of the BiCMOS dynamic A1 cell and the CMOS static A cell used in the divider circuit. The BiCMOS one occupies an area of $513\mu m \times 381\mu m$. The CMOS one has an area of $267\mu m \times 336\mu m$. (b) Layout of the 8-bit÷4-bit divider circuits based on a non-restoring architecture with carry-look-ahead using BiCMOS dynamic circuits and CMOS static circuits. The die area of the BiCMOS one is $3746\mu m \times 2890\mu m$. The CMOS static one has a die area of $1957\mu m \times 1794\mu m$.

In order to evaluate the performance of the BiCMOS dynamic divider circuit, a test chip including two 8-bit÷4-bit dividers using the BiCMOS dynamic and CMOS static circuits has been designed based on a $2\mu m$ BiCMOS technology. Fig. 4(a) shows the layout of the BiCMOS dynamic A1 cell and the CMOS static A cell used in the divider circuit. The BiCMOS one occupies an area of $513\mu m \times 381\mu m$. The CMOS one has an area of $267\mu m \times 336\mu m$. Fig. 4(b) shows the layout of two 8-bit÷ 4-bit divider circuits using CMOS static and BiCMOS dynamic circuits. The aspect ratios of all NMOS and PMOS devices used in both CLA circuits are $18\mu m/3\mu m$ and $32\mu m/3\mu m$, respectively. The BiCMOS dynamic divider circuit occupies an area of $3746\mu m \times 2890\mu m$, which is larger as compared to the CMOS static one, which has an area of $1957\mu m \times 1794\mu m$. Fig. 5 shows the transient waveforms of the quotient signals– Q_0, Q_1, Q_2 Q_3 and Q_4 in the 8-bit÷4-bit CMOS static and BiCMOS dynamic divider circuits with an output of $0.1pf$. As

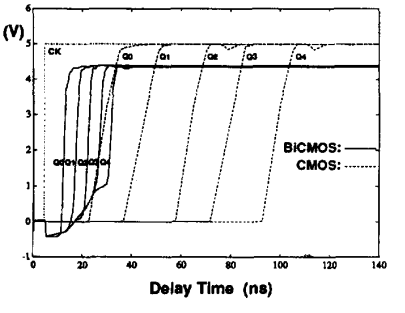


Fig. 5 Transient waveform at the internal nodes of the 8-bit÷4-bit divider using BiCMOS dynamic circuit and CMOS static circuits based on the non-restoring architecture with carry-look-ahead.

indicated in the figure, the propagation delay, Q_4, associated with the longest critical path in the BiCMOS dynamic divider circuit is less than $26ns$, which is more than 3.5 times the speed of the CMOS dynamic MCLA circuit ($93ns$). Fig. 6 shows the propagation delay in the longest critical path vs. quotient bit number of the CMOS static and BiCMOS dynamic divider circuits. In the CMOS static divider circuit, the propagation delay is linearly proportional to the quotient bit number. Specifically, in a CMOS static divider circuit, the propagation delay increases from 23ns at 1-bit to over 161 ns at 9-bit. On the other hand, in a BiCMOS MCLA circuit, the propagation delay increases more slowly as the quotient bit number increases. Specifically, in a BiCMOS dynamic divider circuit, the propagation delay increases from 6.6ns at 1-bit to 36ns at 9-bit. Although the integration size increases nine times, the propagation delay increases only 5 times in the BiCMOS divider circuit. The slow increase in the propagation delay as the bit number increases for the BiCMOS dynamic one can be attributed to the powerful driving capability of the two bipolar devices in each cell. In fact, for a large scale applications, the BiCMOS dynamic divider circuit shows an absolute advantage in speed performance.

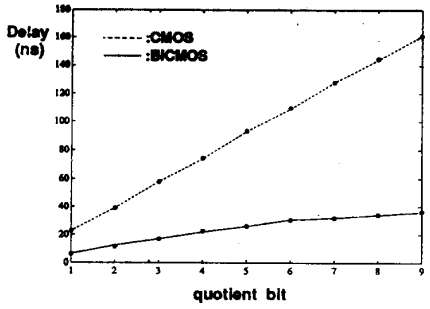


Fig. 6 The speed performance of CMOS static and BiCMOS dynamic dividers vs. quotient bit number.

The dynamic BiCMOS techniques described in this paper are applicable not just to the divider circuits. It can be used in any large scale pipelined system implemented by the CMOS dynamic circuits to enhance the speed performance at a cost of two extra bipolar transistors per stage- one bipolar transistor is for the precharge/predischarge and the other one is for the logic gate.

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