Device-Level Analysis of a BiPMOS Pull-down Device Structure for Low-Voltage Dynamic BiCMOS VLSI

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Abstract

This paper presents a device-level analysis of a BiPMOS pull-down structure for low-voltage dynamic BiCMOS logic gate circuit suitable for VLSI using sub-quarter-micron BiCMOS technology. Thanks to the BiPMOS pull-down structure, despite the slow turn-off of the bipolar device, the 1.5V full-swing BiCMOS dynamic logic gate circuit shows a more than 1.8 times improvement in speed as compared to the CMOS static one.

Introduction

BiCMOS dynamic circuits have used to enhance the speed performance of a digital circuits [1]-[3]. For advanced BiCMOS technologies, scaling power supplies is unavoidable [4][5]. For a deep sub-quarter-micron BiCMOS technology, a 1.5V supply is necessary. With a 1.5V power supply voltage, the BiCMOS dynamic circuit introduced before [1]-[3] cannot be used. By avoiding the difficulties associated with the BiPMOS pull-up and the BiNMOS pull-down structures as shown in Fig. 1 (a)&(b), a dynamic "BiPMOS pull-down" structure (Fig. 1(c)) has been reported to realize the BiCMOS dynamic logic gate circuit for an advanced BiCMOS technology using a power supply of 1.5V [6]. Using the BiPMOS pull-down structure, a 1.5V BiCMOS dynamic minimum circuit for VLSI implementation of fuzzy controllers has been reported [6]. In a conventional BiCMOS circuit, charge removal from the bipolar device is critical in determining the switching performance [7][8]. For a low-voltage BiCMOS circuit, charge removal from the bipolar device may be even more important. In this paper, a device-level analysis of the BiPMOS pull-down structure for low-voltage dynamic BiCMOS logic gate circuit is described. It will be shown that despite the slow charge removal process of the bipolar device, the BiPMOS pull-down structure provides a 1.5V full-swing BiCMOS dynamic logic logic gate circuit with a better performance. In the following sections, the 1.5V BiCMOS dynamic logic circuit using the "BiPMOS pull-down" structure is described first, followed by performance evaluation and discussion.

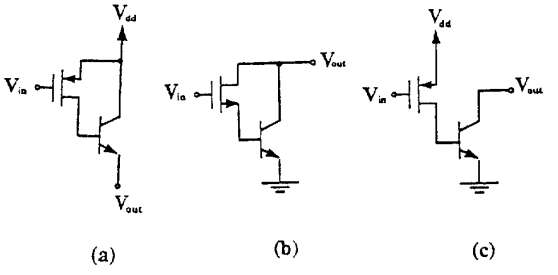

Figure 1: (a) pull-up BiPMOS device. (b) pull-down BiNMOS device. (c) The new pull-down BiPMOS device.

The BiPMOS Pull-down Structure

Fig. 2 shows a two-stage BiCMOS dynamic logic gate circuit using the non-inverting BiPMOS pull-down structure suitable for 1.5V operation. This BiCMOS dynamic logic circuit is made of the PMOS precharge switch MPC, two control switches $MN1$, $MP1$, the CMOS NAND gate as feedback and the BiPMOS pull-down structure containing two input PMOS devices $MP2$ and $MP3$. Different from the BiPMOS pull-up and the BiNMOS pull-down

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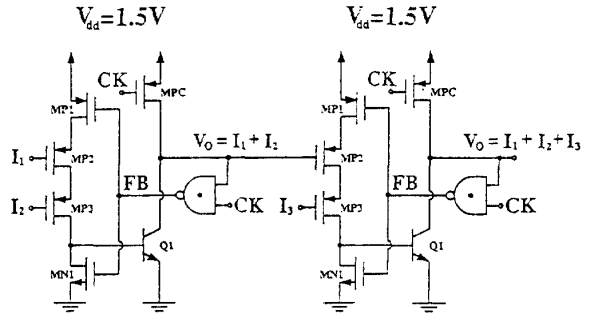

Figure 2: The two-stage 1.5V full-swing BiCMOS dynamic logic circuit using the new pull-down BiPMOS device.

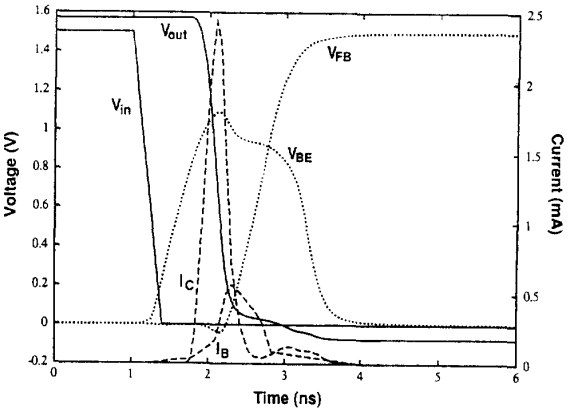

Figure 3: The collector and base currents (I_c, I_b) of the bipolar device Q_1 and the output voltage (V_o) of the BiCMOS dynamic logic circuit during switching.

structures, the BiPMOS pull-down structure is non-inverting. In contrast to the BiPMOS pull-up and the BiNMOS pull-down structures, in the BiPMOS pull-down structure, the input is referred to V_{dd} and the output is with respect to the ground level. Therefore, the output level can easily reach the ground level.

The operation of the BiCMOS dynamic logic circuit is divided into two periods – the precharge period and the logic evaluation period. During the precharge period, CK is low, the output is pulled high to V_{DD}. At this time, the bipolar device is turned off by $MN1$, which is controlled by FB coming from the CMOS NAND gate. In addition, $MP1$ is turned off. After the precharge period, during the logic evaluation period, both MPC and $MN1$ are turned off and $MP1$ is on. If both inputs (I_1, I_2) are low ($0V$), the bipolar device (Q_1) will be turned on. As a result, the output is pulled low to the ground level. After the output is pulled down, FB will switch to high. Then, $MN1$ is turned on and $MP1$ is turned off. As a result, the bipolar device is turned off and no current flows in $MP1$, $MP2$, and $MP3$. During operation, the bipolar device is on only during switching. In addition, a full swing of 1.5V at the output of the BiCMOS dynamic logic gate can be obtained.

Transient Analysis

In order to show the effectiveness of the 1.5V full-swing BiCMOS dynamic logic gate circuit, a test chip including a two-stage BiCMOS dynamic logic gate circuit with the BiPMOS pull-down structure has been designed based on a $1\mu m$ BiCMOS technology[9].

Fig. 3 shows the collector and the base currents (I_c, I_b) of the bipolar device Q_1 and the output voltage (V_o) of the BiCMOS dynamic logic circuit during switching. During the precharge period, as the clock signal CK switches low, the output voltage V_{out} is pulled high. After the clock signal CK is turned high, if inputs I_1 and I_2 are low, the bipolar device is turning on and substantial base and collector currents can be seen. After the output voltage is pulled low, $MN1$ is turned on and the bipolar device, which is in saturation, is turning off. With an output load of $0.2pf$, the switching time of the 1.5V full-swing BiCMOS dynamic logic gate circuit is 1.18ns. As shown in Fig. 3, the turn-off process of the bipolar device is slow, which can be modeled by PISCES [10] using the 2D device-level simulation for the bipolar device with the related CMOS circuit environment. Fig. 4 shows the 1D electron density distribution in the substrate direction in the intrinsic region of the bipolar device during the transient. As shown in this figure, charge removal process is slow, which can be understood by considering the 2D current flow lines in the bipolar device during turn-off at 3ns as shown in Fig. 5. As shown in this figure, most of the current flows via the base contact as a result of saturation of the bipolar device. Despite the slow charge removal process, the switching speed of the dynamic logic gate is not affected since only the turn-on process is important.

The speed performance of the 1.5V BiCMOS dynamic logic gate circuit is sensitive to the power supply voltage. Fig. 6 shows the propagation delay of

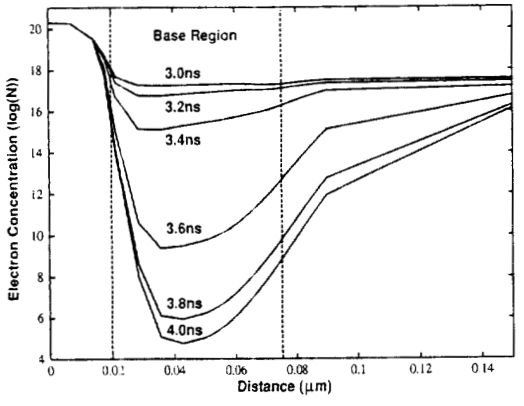

Figure 4: The 1D current density distribution in the substrate direction in the intrinsic region of the bipolar device during the turn-on process.

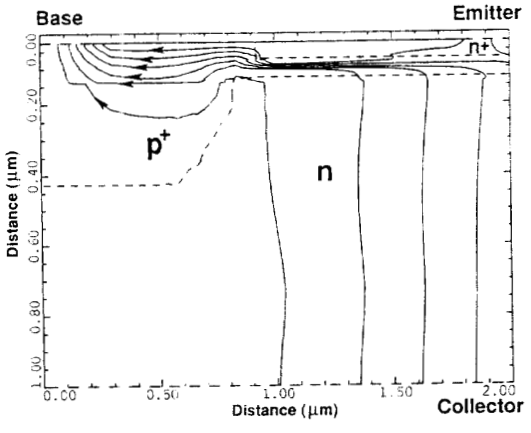

Figure 5: The current flowline in the bipolar device at $3ns$.

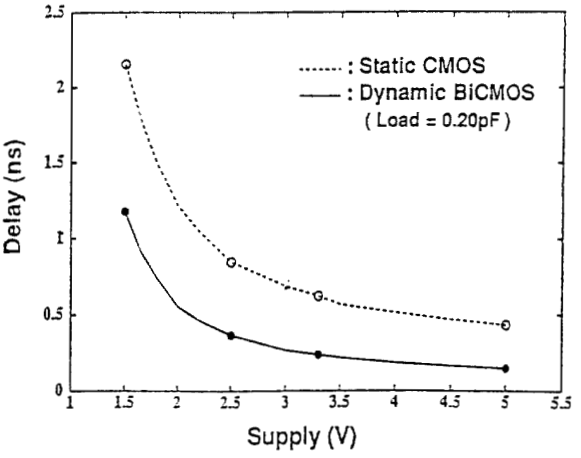

Figure 6: Propagation delay of the logic gate using BiCMOS dynamic and CMOS static techniques vs. the supply voltage.

the logic gate using the BiCMOS dynamic and the CMOS static circuit techniques vs. the supply voltage. As shown in Fig. 5, the propagation delay of the BiCMOS dynamic circuit improves depending on the supply voltage used, as compared to the CMOS static circuit. For a power supply of 5V, the improvement is 3 times. For a power supply of 1.5V, the improvement 1.8 times.

Conclusion

In this paper, a device-level transient analysis of a BiPMOS pull-down structure for a low-voltage full-swing BiCMOS dynamic logic gate circuit suitable for VLSI using advanced BiCMOS technology has been reported. Thanks to the BiPMOS pull-down structure, despite the slow turn-off of the bipolar device, the 1.5V full-swing BiCMOS dynamic logic gate circuit shows a more than 1.8 times improvement in speed as compared to the CMOS static one.

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