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Unified Convolutional/Turbo Decoder Architecture Design Based on Triple-Mode MAP/VA Kernel

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ABSTRACT

In this paper, we proposed triple-mode MAP/VA timing charts that can run two different algorithms at the same time by complementing each other. Then, we address the implementation of a reconfigurable architecture for unified convolutional/ turbo decoder design. According to the triple-mode MAP/VA timing chart and by merging some similar modules in both the Viterbi decoder and the log-MAP turbo code decoder, we build one unified component decoder with both of these two functions. Besides, in order to conform to the advance communication standard, our decoder can also perform as a reconfigurable trellis decoder. That is, our design meets the requirement of the multi generator polynomial in the convolutional code specification.

1. INTRODUCTION

In the modern forward-error-control coding system, the convolutional decoder based on the Viterbi algorithm (VA) is a maximum-likelihood decoding method, which minimizes the probability of word errors [1]. In the recent years, a new class of convolutional codes called turbo codes was introduced by Berrou, Glavieux, and Thitimajashima [2], and it is well known for its extremely superior decoding accuracy. The turbo decoder consists of two component soft-in-soft-output (SISO) decoders and operators by iteration-decoding property. The soft-output algorithm prescribed in the original turbo code paper [2] is usually known as the maximum a-posteriori probability (MAP) algorithm or Bahl-Cocke-Jelinek-Raviv (BCJR) algorithm [3]. There are also many new researches about component decoders, such as Soft-Output Viterbi-Algorithm (SOVA) [4], Maximum-Log-MAP or Log-MAP algorithm [5]. Additionally, the Log-MAP algorithm, which has better bit error rate (BER) performance than the SOVA and the Max-Log-MAP algorithm, is adopted to decode the data from the turbo encoder.

Generally speaking, the performance of turbo code is closer to the Shannon limit than any other convolutional code today. Due to the outstanding decoding ability, turbo coding gets rapid development within just a few years and become standardized. As a result, the 3G mobile wireless communication system standards, like WCDMA [6] in Tab. 1, adopted turbo coding as one of the channel-coding scheme.

In current 3G standards, the voice and data streams in the transmitter use different types of FEC coding schemes, such as convolutional code and turbo code. And traditionally, the corresponding convolutional and turbo code decoders are built separately. To satisfy the advanced FEC standard, a prototype design of a triple-mode convolutional/turbo decoder is proposed in Fig. 1,which can save chip area and make the timing efficient.

The design issues are based on two targets, which are timing association and hardware association. We proposed a triple-mode timing chart that can run Viterbi and MAP algorithms by complementing each other at the same time, or run separately to archive timing association. Moreover, a reconfigurable architecture can make hardware association. Thus our design performs dual functions at the same time and the chip area is only a little larger than the original turbo decoder. Besides, early-termination employing cyclic redundancy check (CRC) aided design is adopted for power saving purpose [7]. And our reconfigurable design can be applied to specifications with different generator polynomials.

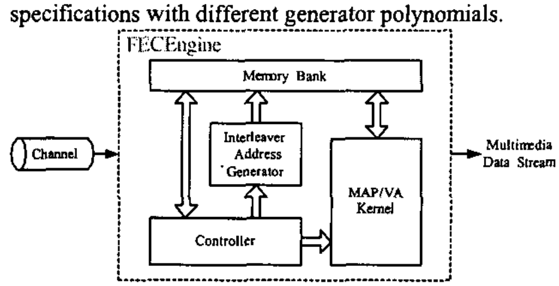

Fig. 1. The proposed unified FEC engine

Tab. 1 3GPP specification

Type of TrCH	Coding Scheme	Coding Rate
BCH, PCH, RACH	Convolutional	1/2
CPCH, DCH, DSCH, FACH		1/2, 1/3
	Turbo	1/3

2. SUMMARY OF DECODING ALGORITHMS

For a forward-error-control (FEC) system, information bits u_i are transmitted an encoder and output encoded symbols x_i. After demodulating, the received symbols $_i$ have been corrupted by channel noise and should be recovered to be noiseless d_i signal by a decoder.

2.1. Viterbi algorithm

The Viterbi algorithm [8] is a maximum-likelihood decoding method for the convolutional code. For a $(n, \ ,m)$ convolutional encoder, it receives bits information data, outputs n bits encoded symbol and has constrain length K that equals $m+1$. The procedure of a Viterbi decoder can be modeled as a trellis. It has 2^{K-1} states and each state S_{i-1} has 2 transitions to next state S_i while i means time steps.

In each time step, the received bits $_i$ must be computed Euclidean distance with each branch symbol $ranch(s,s)$ that S_{i-1} equals s state and S_i equals s state. It s also named branch metric.

$$BM_i(s,s) = [\ _i - \ ranch(s,s)]^2 \qquad (1)$$

Since the object of the decoder is to find the minimum likelihood sequence, we hope that the accumulated Euclidean distances of the last state path metric $PM_{i-1}(s)$ with the present branch metric $BM_i(s,s)$ is to be the minimum. And we can find that eq. (2) is a forward recursive operation.

$$PM_i(s) = \min_s \ PM_{i-1}(s) + BM_i(s,s) \qquad (2)$$

Moreover, the decoder must to store the decision bits d_i that record which state of path metric is accumulated to next state.

$$d_i(s) = \arg\min_s \ PM_{i-1}(s) + BM_i(s,s) \qquad (3)$$

Finally, the decoder selects the minimum distance path and trace back to decode information bits according to decision bits.

2.2. Log MA algorithm

In 1974 Bahl et al. [3] propose a new method to decode the convolutional code, named maximum a-posteriory probability (MAP), which minimizes the probability of symbol (or bit) error while the Viterbi algorithm minimizes the probability of word error. But the computing complexity of MAP is so high that the hardware is impossible to realize due to cost. Therefore, based on Max-Log-MAP algorithm, Log-MAP algorithm was proposed [5] that simplifies the MAP algorithm by transferring these equations into the log arithmetic domain and then using the approximation

$$\ln(\sum_i e^{x_i}) \approx \max_i(x_i). \qquad (4)$$

Then, the forward recursive accumulation with $A_i(s)$, backward recursive accumulation $B_{i-1}(s)$ and transition probability $R_i(s,s)$ defined and rewritten as follows:

$$A_i(s) \approx \max_{\text{all } s} \ A_{i-1}(s) + R_i(s,s) \qquad (5)$$

with the same rule

$$B_{i-1}(s) \approx \max_{\text{all } s} \ B_i(s) + R_i(s,s) \qquad (6)$$

and

$$R_i(s,s) \approx \log[\Pr(\_{}_i|\underline{x}_i)] + \log[\Pr(u_i)]. \qquad (7)$$

Additionally, eq. (5), eq. (6) and (7) are also called alpha, beta and gamma operations. Finally, we can write for the a-posteriori LLRs as

$$L(u_i|\_) \approx \max_{(s,s)\Rightarrow u_i=1} \ A_{i-1}(s) + R_i(s,s) + B_i(s) - \max_{(s,s)\Rightarrow u_i=0} \ A_{i-1}(s) + R_i(s,s) + B_i(s). \qquad (8)$$

Because of the approximation we applied, the Max-Log-MAP algorithm is sub-optimal and the problem can be fixed by using the Jacobian logarithm [5]:

$$\begin{aligned}\ln(e^{x_1} + e^{x_2}) &= \max(x_1 + x_2) + \ln(1 + e^{-|x_1 - x_2|}) \\ &= \max(x_1 + x_2) + L \quad T(|x_1 - x_2|)\end{aligned}, \qquad (9)$$

where $\ln(1 + e^{-|x_1 - x_2|})$ is a correction function and can be realized by look-up-table (LUT). We apply this rule to the Log-MAP algorithm by compensating for one correction term.

3. TRI LE MODE MA VA TIMING ANALYSIS

We proposed the triple-mode MAP/VA timing chart that include MAP/VA mode, VA mode and MAP mode. Besides, the MAP/VA mode indicates that the MAP decoding and VA decoding are operating at the same time. It s special that the timing in the VA mode, is different with the VA part of MAP/VA mode, and as well as the MAP mode.

3.1. MA VA mode

For MAP/VA mode in Fig. 2, Viterbi decoding and MAP decoding are running at the same time. In the timing chart, the horizontal axis means computing time, the vertical axis means decoding symbols and L means the sliding widow length that approximates five times constrain length K. The parameters Npm, Nt , Na and N mean the number of path-metric unit, trace-back unit, forward-recursive unit and backward-recursive unit. The parameters M and T mean the memory size and throughput (decoding output to overall running time ratio). We will describe VA and MAP part respectively.

In the VA part, the forward recursive unit (RUF) does path metrics (PM) operation in the area I and II from the head of the first data block. The vertical length of the gray triangular indicates the size of memory, in which are the decision bits produced by the PM operation, and the horizontal length indicates the surviving time of the decision bits for being used. In area

III, trace-back unit (TB) begins to fetch decision bits d from memory and trace back from the tail of the second data block. The dotted line means invalid trace backing until more than L. Then, TB produces correct information bits in area IV.

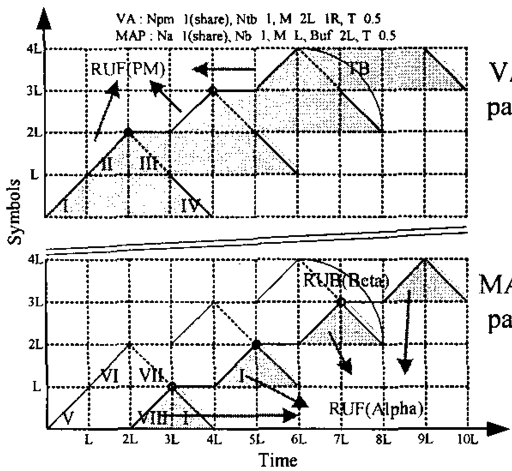

Fig. 2. Timing of triple-mode (MAP/VA mode)

In the MAP part, the slight gray area indicates buffers. In area V and VI, the encoded symbols are serially inputted and stored in buffers. The backward recursive unit (RUB) does beta operation in area VII from the tail of the second data block. The dotted line means dummy beta operation until more than L, and thus the backward recursive probability $B_i(s)$ need not to be stored. At the same time, the RUF does alpha operation in area VIII and produce forward recursive probability $A_i(s)$ for being used. The gray triangular has the same meaning with VA part except the content that is forward recursive probability $A_i(s)$. In area I , RUB does valid beta operation and produce backward recursive probability $B_i(s)$ and at the same time combines with the forward recursive probability $A_i(s)$ fetched form memory and transition probability $R_i(s,s)$ to produce log-likelihood-ratio (LLR) $L_i(u_i|\_)$.

In particular, in the timing chart, we can find that the RUF does PM operation in VA part (area I, II and) and does alpha operation in MAP part (area VIII and I). Therefore, the VA and MAP decoding can run at the same time successfully by sharing the RUF.

3.2. VA mode

For VA mode in Fig. 3, we use the interleaving and pointer techniques to reduce memory. Specially, we try to reconfigure the RUB in MAP part into additional RUF by exchanging the input and output ports of trellis wires. Thus, the hardware of RUB in MAP part does not waste and improve the reducing of memory. In area I and II, the RUF0 does PM operation and produces decision bits d . Instead of a big memory requirement (gray triangular) in Fig. 2, it stores only one stage of forward recursive probability $PM_i(s)$ in registers used to be the initial probability by RUF1, and the small gray triangular of decision bits d . Then, in block III and IV, except TB does trace-back operation, RUF1 fetches the initial probability $PM_i(s)$ from registers and does PM operation that produces decision bits d at the same time.

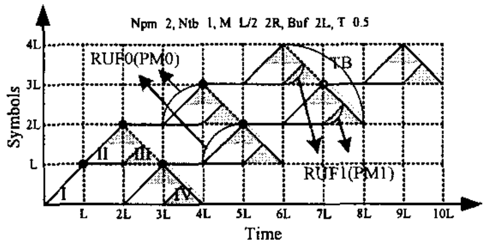

Fig. 3. Timing of triple-mode decoding (VA mode)

3.3. MA mode

For the MAP mode in Fig. 4, we use the pointer technique in area IV by the original sharing part of RUF in MAP/VA mode to reduce the memory. In the view of hardware, there is just TB in VA part idle, which has smaller area and less computing power.

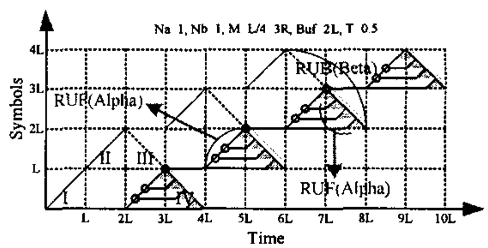

Fig. 4. Timing of triple-mode decoding (MAP mode)

4. RO OSED ARCHITECTURE OF TRI LE MODE KERNEL

To satisfy advanced multi-spec communication system, a FEC engine, shown in Fig. 1, is necessary that just change some control signal or memory bank for different system. Therefore, except our proposed triple-mode MAP/VA timing chart, we proposed a MAP/VA kernel, which can be reconfigured for different decoding method or different parameters

4.1. MA VA ernel

According to our proposed triple-mode MAP/VA timing chart, one forward recursive unit (PM0/RUF), one backward recursive unit (PM1/RUB) and one trace-back unit (TB) are needed. Moreover, the distance between the received bits and the symbol one each branch is computed immediately for recursive units, so the transition probability-computing units (BM0/Gamma0 and BM1/Gamma1) are built. Based on trellis decoding, the encoder-embedded-trellis-routers (EETR0 and EETR1) can be reconfigured for different generation parameters and code rates. Fig. 5 shows the proposed block diagram of the MAP/VA kernel, including computing blocks, wires and memory modules.

5. CONCLUSIONS

For the recently similar studies [9][10], they only archive hardware association concept. But in this work, we archive the timing association and hardware association.

A practical design of a triple-mode convolutional/ turbo code decoder is proposed. The methodologies we use here to combine the Viterbi decoder and the Log-MAP decoder are based on the triple-mode MAP/VA timing chart and similarities of the innate characters between these two algorithms. Besides, the basic principle of triple-mode and multi specifications for channel-coding design can also be easily adopted to other advanced communication system standards such as CDMA2000 or WCDMA.

6. REFERENCES

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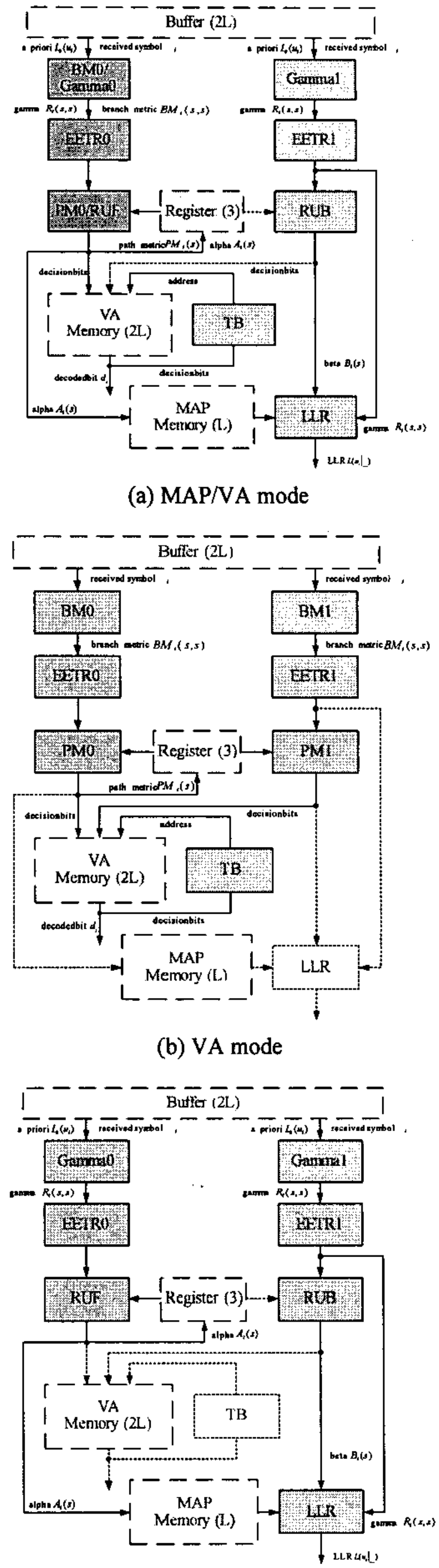

(a) MAP/VA mode

(b) VA mode

(c) MAP mode

Fig. 5. Block diagram of triple-mode MAP/VA kernel