行政院國家科學委員會專題研究計畫 期中進度報告

先進 CMOS 元件及製程研究--子計畫一：適用於低溫基板製程之高品質絕緣膜形成技術(2/3)

期中進度報告(精簡版)

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執 行 期 間 ：95 年 08 月 01 日至 96 年 07 月 31 日
執 行 單 位 ：國立臺灣大學電子工程學研究所

計 畫 主 持 人 ：胡振國

處 理 方 式 ：期中報告不提供公開查詢

中 華 民 國 96 年 05 月 30 日

行政院國家科學委員會補助專題研究計畫成果報告

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※ **先進 CMOS 元件及製程研究 – 子計畫一 ：** ※
※ **適用於低溫基板製程之高品質絕緣膜形成技術(2/3)** ※
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計畫類別：□個別型計畫　■整合型計畫

計畫編號：**NSC95-2221-E-002-358**

執行期間： 95 年 8 月 1 日 至 96 年 7 月 31 日

計畫主持人 ： 胡振國　台大電子工程學研究所教授

計畫參與人員：張嘉華、陳志豪、王志慶、江榮進

成果報告類型(依經費核定清單規定繳交)：■精簡報告　□完整報告

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執行單位：台大電子工程學研究所

中　華　民　國　**96** 年　**5** 月　**25** 日

行政院國家科學委員會補助專題研究計畫期中成果報告

先進 CMOS 元件及製程研究
子計畫一:適用於低溫基板製程之高品質絕緣膜形成技術(2/3)

第二年(95/8~96/7)期中進度報告

計畫編號:NSC95-2221-E-002-358

主　持　人: 胡 振 國　台大電機工程學系/電子工程學研究所教授

共同參與研究生: 張嘉華、陳志豪、王志慶、江榮進

一、　摘要：

本計畫在第二年度之主要研究成果可分為以傾斜晶圓濺鍍Hf金屬並以硝酸氧化再純水補償備製低溫 HfO_2 高介電常數絕緣層技術、以純水應力陽極氧化生長法備製高品質超薄閘極氧化層技術、及以傾斜遮罩蒸鍍 Al 金屬並以硝酸氧化備製低溫 Al_2O_3 高介電常數絕緣層技術三大部份。三部份之執行均以低溫備製完成，適合低溫基板應用。

在以傾斜晶圓濺鍍Hf金屬並以硝酸氧化再純水補償備製低溫 HfO_2 高介電常數絕緣層技術部份，提出新穎特殊之傾斜晶圓來得到不同厚度 Hf 金屬，經過室溫硝酸氧化為 HfO2 再以純水陽極氧化補償漏電路徑，得到等效厚度可達 19 nm，崩潰電場可達 12 MV/cm，漏電流低且可靠性佳之低溫高介電常數絕緣層。

在以純水應力陽極氧化生長法備製高品質超薄閘極氧化層技術部份，延續第一年的研究成果，對 p 及 n 型基板之晶圓均進行研究比較，發現 MOS(p)與 MOS(n)元件氧化層之漏電流明顯較對照組減少，特性獲改善。

在以傾斜遮罩蒸鍍Al金屬並以硝酸氧化備製低溫 Al_2O_3 高介電常數絕緣層技術部份, 將晶圓前方放置一遮罩，利用傾斜角度調整得到同一晶圓上有不同之鋁厚度，經由本單位提出之硝酸氧化法可得不同連續厚度變化之低溫 Al_2O_3 高介電常數絕緣層，特性穩定。

關鍵詞：高介電常數絕緣層、HfO_2、Al_2O_3、應力陽極氧化

Abstract:

In the second year of this project, there are three main subjects studied. The first is the low temperature HfO_2 prepared by tilted sputtering of Hf metal and then followed by nitric acid oxidation compensated with anodization in D.I. water. The second is the preparation of high quality ultra-thin gate oxides by strain-oxidation technique carried out in D.I. water with bent wafer. The third is the preparation of Al_2O_3 high-k dielectrics by shadow evaporation of Al film on a wafer and then oxidized by nitric acid. The above three works are related to low temperature which are suitable for low temperature substrate applications.

In the first subject of the low temperature HfO_2 prepared by tilted sputtering of Hf metal and then followed by nitric acid oxidation compensated with anodization in D.I. water, the wafer is tilted during sputtering to obtain continuously distributed thickness in one single substrate. The oxidized HfO_2 was compensated by anodization in D.I. water to repair the leaky path in existing oxides. The smallest equivalent oxide thickness is 19 nm, the effective breakdown field is higher than 12 MV/cm, the leakage current is low and the reliability is satisfactory for the prepared low temperature high-k dielectrics.

In the second subject of the preparation of high quality ultra-thin gate oxides, the method as proposed in the first year was continuously studied. Both of p and n type wafers are used for comparison. The leakage currents for MOS(p) and MOS(n) structures with oxides prepared by strain-oxidation methods are obviously lower than those control samples under the same oxide thickness. The reliability for the former ones are also superior to the latter ones.

In the third subject of the preparing high-*k* Al_2O_3 gate dielectrics by evaporation of Al films with a shadow mask during evaporation and then oxidized in nitric acid, a shadow mask with a tilt angle with respect to the horizontal wafer is placed in front of the wafer during evaporation. The continuously varied Al thickness on a single wafer is obtained by this simple technique. The former proposed method of oxidation in nitric acid was used to oxidize the formed Al films to become Al_2O_3. This low temperature Al_2O_3 high-k dielectrics are stable in reliability.

Keywords: High-*k* dielectrics, HfO_2, Al_2O_3, strain-anodization.

二、緣由與目的：

在顯示器或軟性基板上，有許多製程是需要在低溫下進行的，由於溫度低，所以絕緣層之品質改善倍受注意，如何有效改善漏電流或提高可靠度，相關技術是值得注意的。本計畫所度提出要得到低溫絕緣層，可將薄金屬層予以液體酸中氧化，但必需金屬很薄；因此將晶圓於濺鍍設備中傾斜一角度，利用不同之視角因素調整，可得連續厚度分布之金屬膜層，再於之後的氧化步驟可得連續厚度分布之不同氧化層，這對元件特性分析是相當有用的。

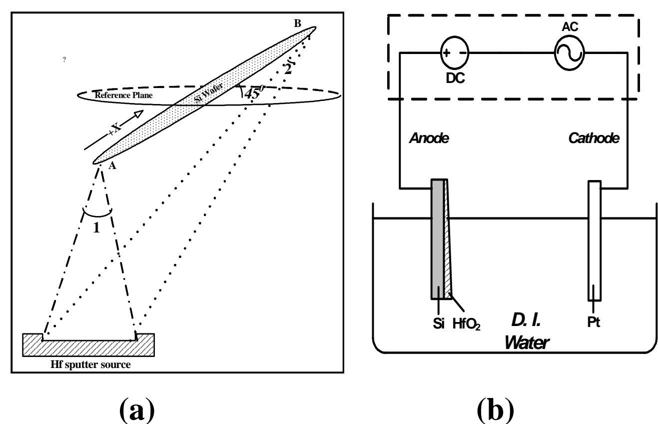
另外，延續第一年之成果，發現若在 SiO_2 與 Si 界面間給予適當之應力，則在氧化層生長時會有較完整之晶格結構，所得之氧化層特性獲改善。在本年度中，同時研究 p 型及 n 型矽基板之應力陽極氧化生長氧化層，結果均發現在相同厚度下，MOS 元件之漏電流獲明顯改善，這對矽基板相關氧化層之低溫備製技術是有相當的助益。

在研究不同厚度之高介電絕緣層時，本單位亦發現在傳統之蒸鍍鋁金屬時，若將一遮罩置於晶圓之前，再給予適當之傾斜角度，可得不同厚度且連續變化之金屬鋁膜，之後再利用硝酸氧化法可得 Al_2O_3 高介電常數絕緣層, 由於均為低溫下完成，且在同一片晶圓上可以有多種厚度可供研究，可得知何種厚度配合最佳氧化製程可得最可行之絕緣層膜備製條件，相當具前瞻性。

三、研究方法與成果：

(A).以傾斜晶圓濺鍍 Hf 金屬並以硝酸氧化再純水補償備製低溫 HfO_2 高介電常數絕緣層技術

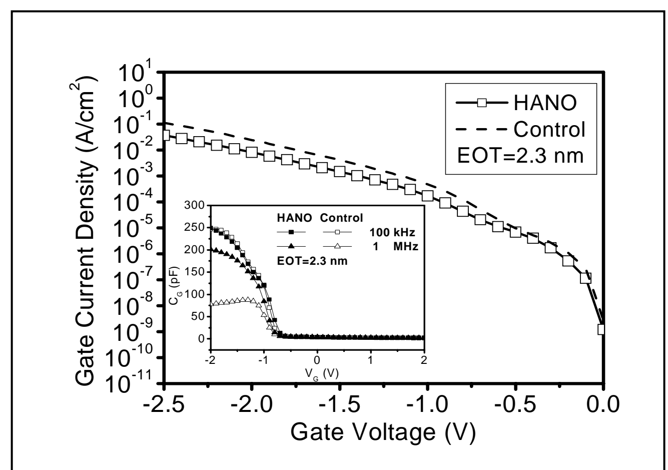
圖一(a)為一傾斜晶圓於濺鍍時之不同濺鍍視角示意圖，由於濺鍍源非點狀源，而是有一空間之分布，因此在晶圓上會形成不同之厚度。圖一(b)為陽極氧化槽示意圖，用來將氧化後之 HfO_2 予以純水中修補漏電路徑。在陽極氧化補償後, 元件會在 380°C 下於 N2 環境中進行退火，期使元件特性改善。



(a) (b)

圖一

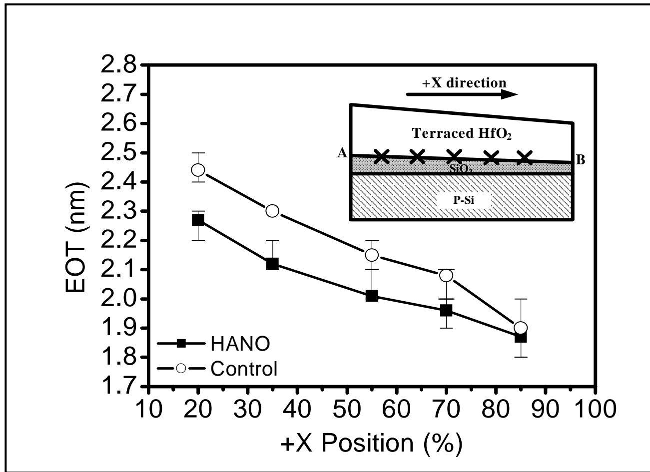
圖二為所得有經陽極氧化補償的 HfO_2(簡稱 HANO)與對照組之 C-V 及 I-V 比較圖, 可看出在相同等效厚度(EOT)為 2.3nm 下, HANO 較 Control 的漏流為小。



圖二

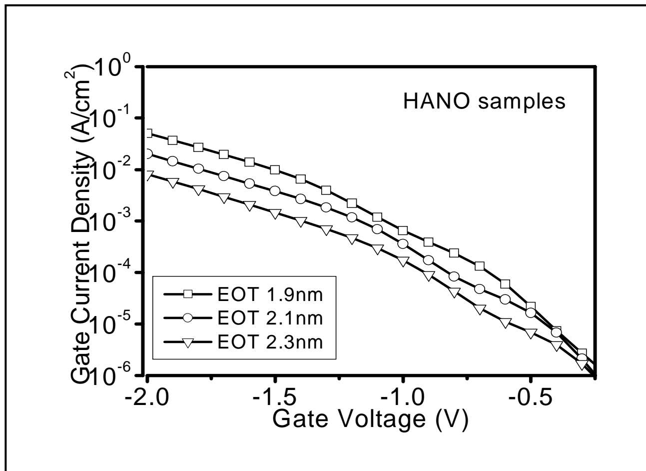
圖三為在同一晶圓上所量得之 HANO 與 Control 之 EOT 對位置分布圖，可看出 EOT 確

實隨位置而漸變，表示傾斜濺鍍確實發揮效果;同時可得知 HANO 較 Control 之 EOT 為小，表示 HANO 所得之 HfO_2 較為理想，其介電常數值較大，因此 EOT 較小。



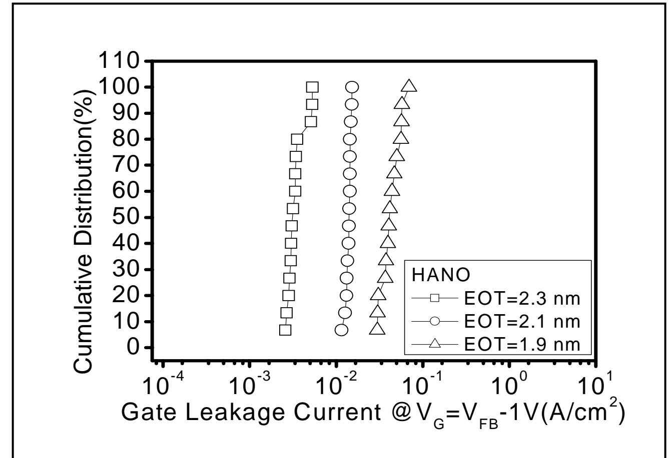
圖三

圖四為所得 HANO 元件在 EOT 為 1.9、2.1、及 2.3 nm 下之 I-V 特性，可看出電流會隨厚度而做變化，具高介電常數絕緣層之不同厚度特徵。

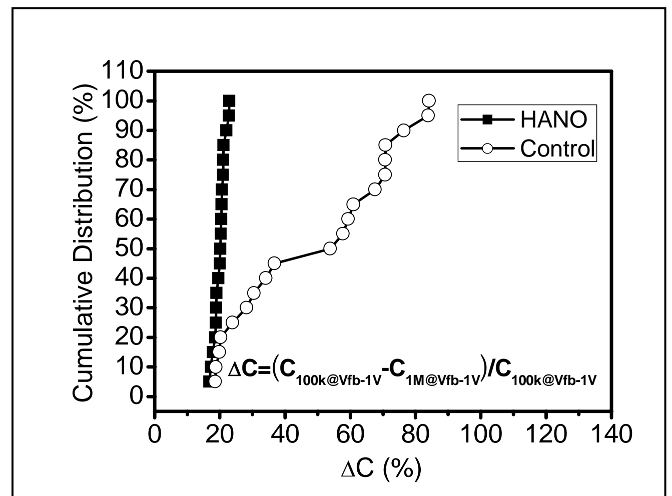


圖四

圖五為 HANO 元件在 EOT 為 1.9、2.1、及 2.3 nm 下在 $V_G=V_{FB}$-1V 下之電流密度累積統計分布圖，可看出電流分布相當均勻，較純 SiO_2 的漏電流為低，本 HANO 元件已充份展示出高介電常數絕緣層之特徵。圖六則為 C-V 曲線在聚集區(accumulation region)之電容在不同頻率下之變化量比較，可得知 HANO 較 Control 的電容隨頻率變化率為小，也就是說絕緣層之品質較佳，陽極氧化補償效果相當明顯有用。

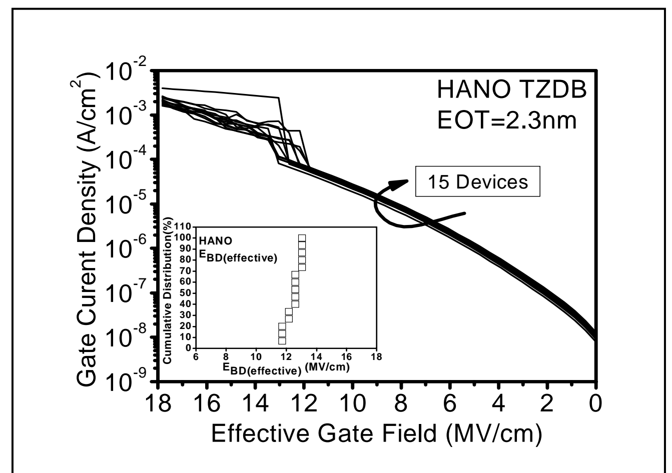


圖五



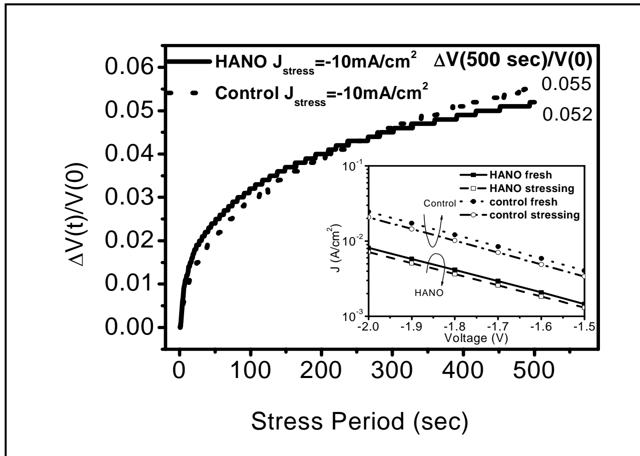
圖六

圖七為 EOT=2.3 nm 的元件其 I-V 特性，相當一致，而 TZDB 崩潰電場可高達 12MV/cm 以上，充份顯示該低溫製程所得 HANO 絕緣層品質之優異。



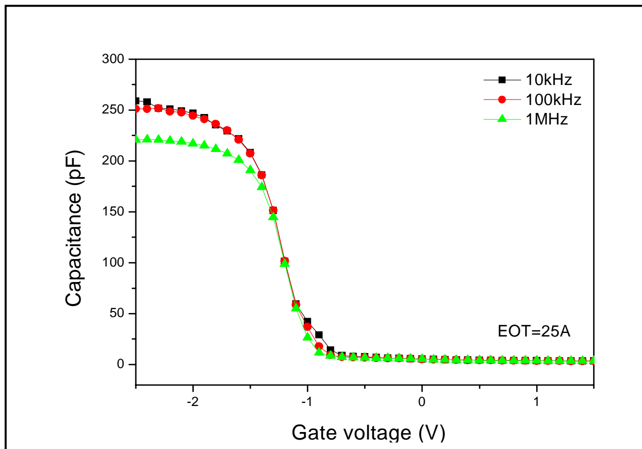
圖七

圖八為 HANO 與 Control 元件在定電流施加下之可靠度比較，可看出 HANO 之表現較為穩定。



圖八

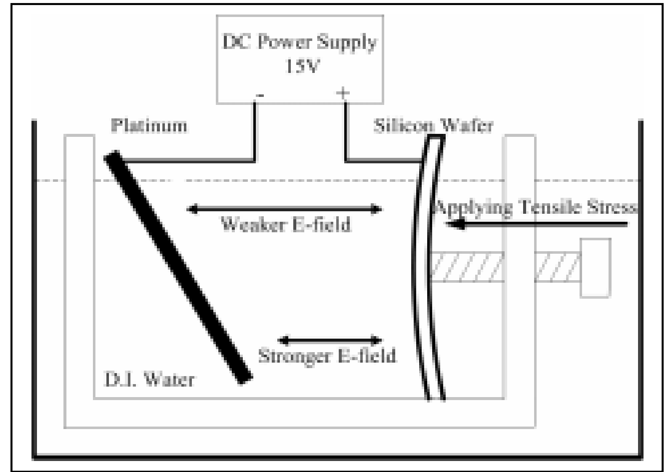
圖九為一 EOT = 2.5 nm 的 HANO 元件不同頻率下之 C-V 特性，可看出界面陷阱密度甚小，頻率引起之變化不大，V_{FB} 值亦接近理想值，可視為一絕佳的絕緣層。



圖九

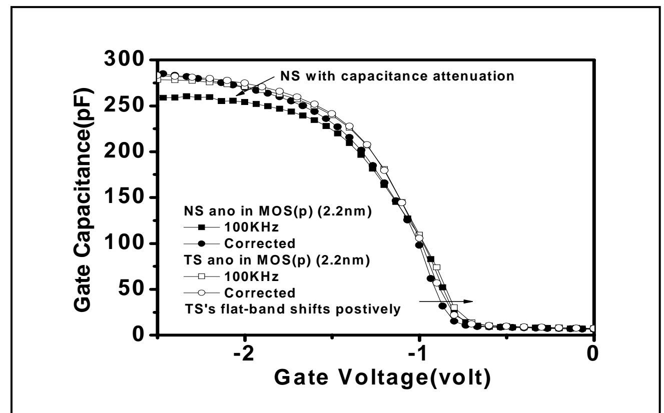
(B). 以純水應力陽極氧化生長法備製高品質超薄閘極氧化層技術

本計畫第一年即已提出如圖十所示之傾斜陽極氧化系統，將 Pt 陰電極予以傾斜，再進行陽極氧化可得不同厚度之氧化層於同一晶圓上，此外在晶圓背面施加一外應力，可使晶圓生長時承受伸張應力，因為在室溫下陽極氧化可有效控制生長速率，很適合超薄氧化層之生長，而伸張應力施加可改善氧化時之晶格距離之差異，因此可達到控制氧化層品質之目的。



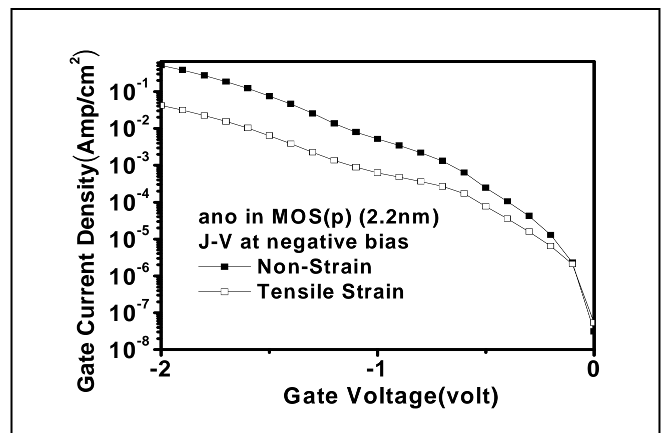
圖十

圖十一為以伸張力生長(TS)與對照組(NS) MOS(p)元件在同厚度為 2.2 nm 下之 100 KHz 與修正後 C-V 特性比較，可清楚看出 TS 元件之電容變化甚少，較 NS 元件表現為佳。



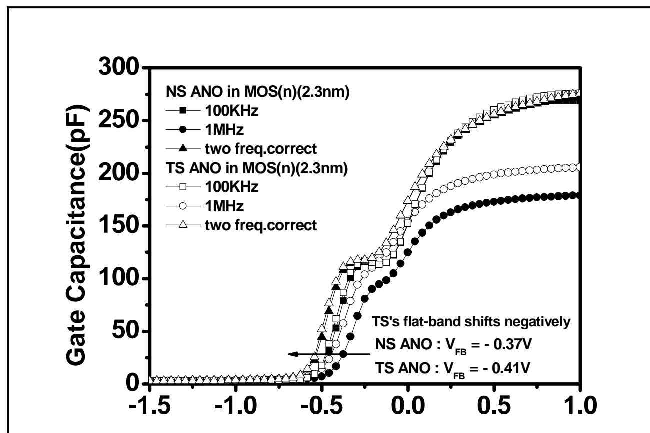
圖十一

圖十二為圖十一兩元件之 J-V 特性比較，可清楚得知 TS 之漏電流明顯較 NS 為小，顯示氧化層之品質較佳。



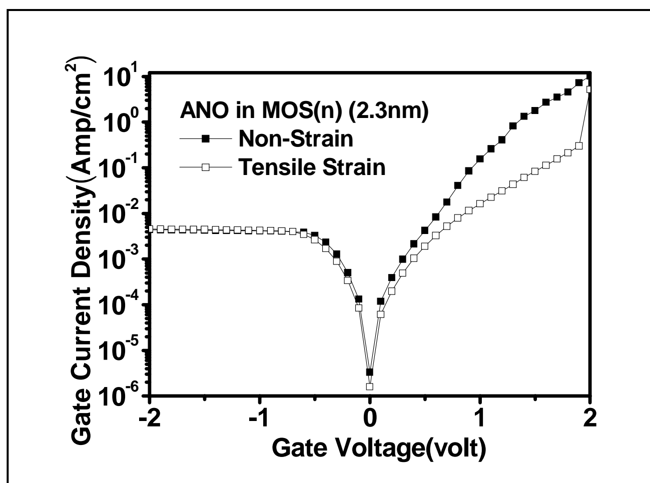
圖十二

圖十三為以伸張力生長(TS)與對照組(NS) MOS(n)元件在同厚度為 2.3 nm 下之 1 MHz, 100 KHz 與修正後 C-V 特性比較，可清楚看出 TS 元件之電容變化較少，較 NS 元件表現為佳。



圖十三

圖十四為圖十三兩元件之 J-V 特性比較，可清楚得知 TS 之漏電流明顯較 NS 為小，顯示氧化層之品質的確獲改善。

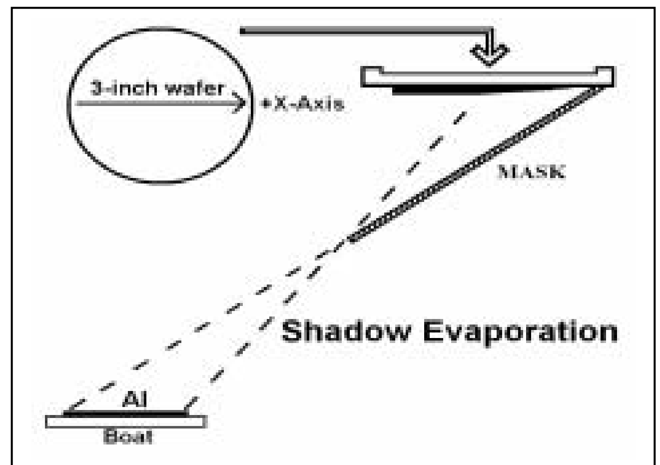


圖十四

從上述之實驗觀察可得知，在超薄氧化層生長時，若能在基板上給予適當之伸張力施加，所得之氧化層因晶格較匹配之故，特性獲明顯改善，此技術仍有相當大的研究空間，將會持續進行並強調其應用性。

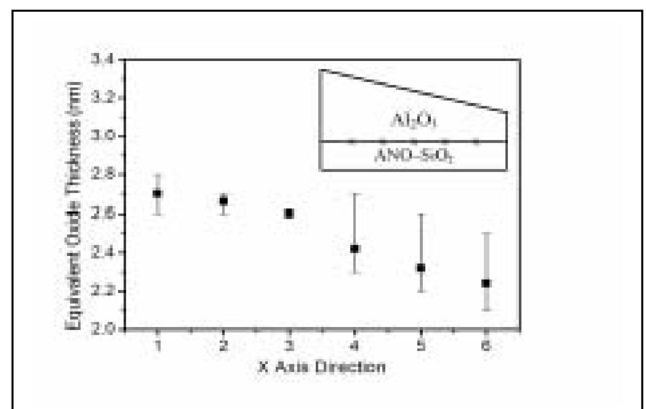
(C).以傾斜遮罩蒸鍍 Al 金屬並以硝酸氧化備製低溫 Al_2O_3 高介電常數絕緣層技術

在備製超薄高介電常數絕緣層時，若是經由氧化金屬得到絕緣層，則事先之金屬膜需愈薄愈好，但因蒸鍍金屬需兼顧蒸鍍速率及時間，才能得到甚薄之金屬，相當不易。本研究提出有別於(A)部份所提之方法，於傳統蒸鍍金屬鋁時，另加一遮板如圖十五所示，利用遮板形成不同之視角因素(view factor)，可得不同厚度之金屬膜於同一晶圓上，而且可得甚薄之金屬膜以供超薄高介電常數絕緣膜備製用。



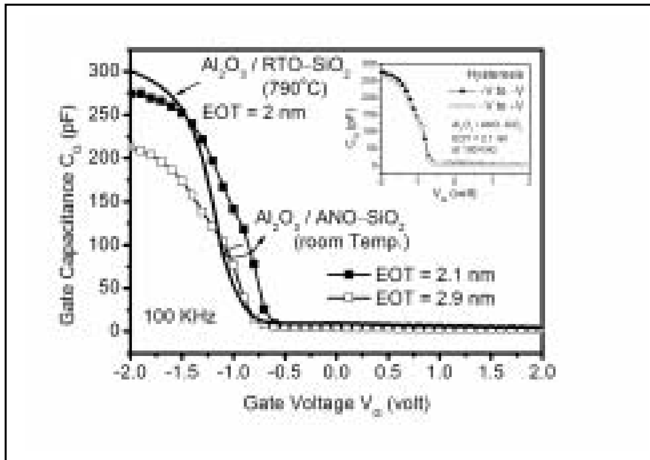
圖十五

圖十六為將漸變厚度金屬鋁經硝酸氧化後，並經低溫 400°C 於 N2 下退火 10 minutes 所得之 MOS(p)元件等效厚度(EOT)分布圖，可看出 EOT 的確隨位置而漸變，如上述之預測。



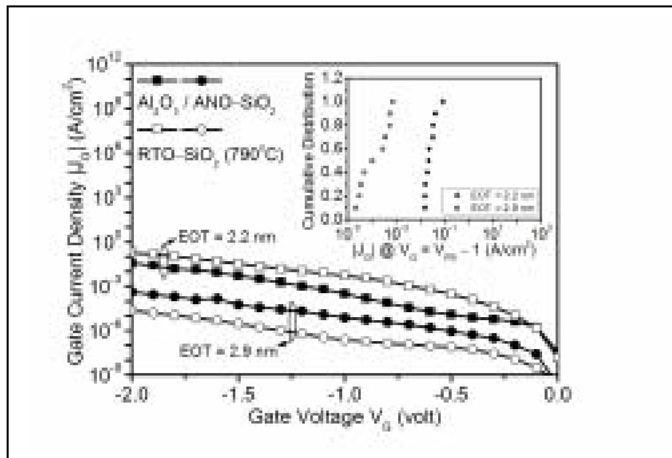
圖十六

圖十七為低溫製程所得 Al_2O_3/ANO-SiO_2 堆疊結構 MOS(p)元件於 2.1 及 2.9 nm 下之 C-V 特性，同時高溫之 Al_2O_3/RTO-SiO_2 於 2 nm 下之 MOS(p) C-V 曲線亦做為比較, 可得知低溫之 Al_2O_3/ANO-SiO_2 具有較多之負電荷，但絕緣層之基本特徵均在，其遲滯現象亦不大，如內插圖所示。



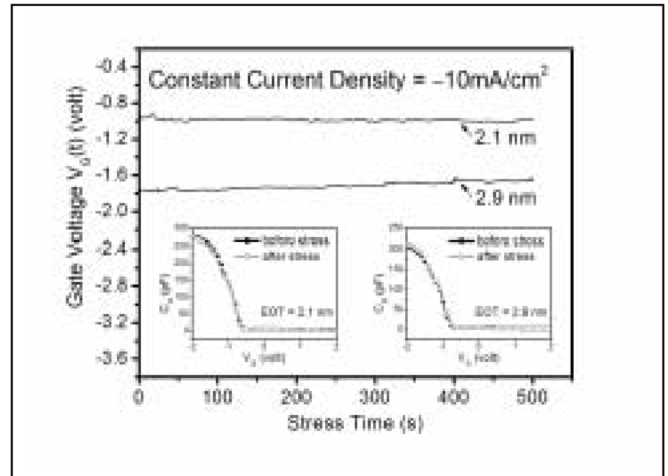
圖十七

圖十八為上述元件之 J-V 特性圖，可看出對於 EOT=2.2 nm 的元件，Al_2O_3/ANO-SiO_2 較 RTO-SiO_2 具有較小之漏電流，顯示高介電常數絕緣層之特徵；但對 EOT= 2.9 nm 則相反，這與金屬鋁被氧化之程度有關，若金屬鋁太厚，則氧化容易不完全，造成漏流嚴重。本研究顯示出可用遮板方式得到甚薄之金屬鋁膜，超薄且低溫製程之 Al_2O_3 高介電常數絕緣層是可預期的。



圖十八

圖十九為 Al_2O_3/ANO-SiO_2 結構於 EOT=2.1 及 2.9 nm 下之定電流施加可靠度分析，可看出較薄之元件其穩定度較佳，而且經施加前後之 C-V 特性變化甚小，對低溫製程(<400°C)絕緣層而言，本方法是相當具參考性的，值得持續研究與改善。



圖十九

四、總結與討論

在本計畫第二年度之研究中，主要提供了二種具前瞻性之超薄膜層備製技術及延續第一年開發之應力下生長高品質氧化層技術，發現出利用傾斜晶圓濺鍍 Hf 金屬並以硝酸氧化再純水補償可備製低溫 HfO_2 高介電常數絕緣層，及以傾斜遮罩蒸鍍 Al 金屬並以硝酸氧化可備製低溫 Al_2O_3 高介電常數絕緣層，兩項技術均具創意及應用性；同時提出之以純水應力陽極氧化生長法備製高品質超薄閘極氧化層技術，對超薄氧化層備製法有其參考價質。所提出之技術均為低溫製程，因此尚有許多的改善空間可做為研究題材。所得成果已發表於 *Applied Physics Letters* 及整理投稿中，相信在後續的研究中會將本計畫提出之技術給予更多之應用。主持人在執行國科會研究計畫由 2004 年至今所產出之研究成果表列如下，僅此提供參考。

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Electrochemical Society, Vol.151, No.9, G549-G553.

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(B) Conference Paper

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(C) Technical Report

1. J.G.Hwu, May 2004, "Study on The Oxide Uniformity and Stress Effect in Rapid Thermal Processing (2/3)", *National Science Council,* NSC92-2215-E-002-005
2. J.G.Hwu, July 2004, "Development of Si Novel Devices and Module Technology (3/3)", *National Science Council,* NSC92-2120-E-002-004
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可供推廣之研發成果資料表(一)

■ 可申請專利　■ 可技術移轉　日期：96 年 5 月 25 日

國科會補助計畫	計畫名稱：適用於低溫基板製程之高品質絕緣膜形成技術(2/3) 計畫主持人：胡 振 國 計畫編號：NSC95-2221-E-002-358　學門領域：微電子
技術/創作名稱	以傾斜晶圓及加遮罩技術備製超薄低溫高介電常數絕緣層
發明人/創作人	胡振國 江榮進 張嘉華
技術說明	中文： 提出之傾斜晶圓及加遮罩技術，可使金屬膜層超薄，配合低溫製程可得超薄品質佳之高介電常數絕緣層，成本低，甚具應用性。 英文： Novel technology of using tilted wafer and adding mask to prepare ultra-thin metal films is potential for the preparation of ultra-thin low temperature high-*k* dielectrics. It is cost-effective and low in process temperature.
可利用之產業及可開發之產品	1. 先進低溫製程高品質絕緣層 2. 低溫大面板絕緣層品質改善
技術特點	1. 低成本 2. 可在同一基板上備製不同厚度絕緣層 3. 具超薄高介電常數絕緣層之開發潛力 4. 低溫處理不易引起雜質重分布
推廣及運用的價值	1. 現今低溫製程廣受重視，高品質絕緣層之備製極為重要，若能取得先機，商機無限。 2. 研發成本低，相對風險低，值得投入開發。