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A Cost-Effective Design for MPEG-2 Audio Decoder with Embedded RISC Core

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Abstract. MPEG-2 audio decoding algorithms are involved of several complex coding techniques and therefore difficult to be implemented by an efficient dedicated architecture design. In this paper, we present an effective architecture for the MPEG-2 audio decoder. The MPEG-2 audio algorithms can be roughly divided into two types of operations. The first type is regular but computation-intensive such as filtering, matrixing, degrouping, and transformation operations. The second type is not regular but computation-intensive such as parsing bitstream, setting operation mode and controlling of all system operations. A RISC core with variable instruction length is designed for the decision-making part, and the dedicated hardware such as special divider, and synthesis filterbank is designed for the computation-intensive part. Based on the standard cell design technique, the VLSI chip consists of 27000 gate counts with the chip size of 6.4×6.4 mm^2. The chip can run at maximum 43.5 MHz clock rate, with the power dissipation of 150 mW at 3 V power supply.

Keywords: MPEG-2, RISC, multichannel, degrouping, synthesis filterbank

1. Introduction

The digital audio coding is more and more popular today. But the amount of the digital-represented audio data is still too large for transmission and storage. Thus the compression techniques are necessary. Some audio efficient compression schemes have been proposed [1–3]. One of the standardized audio compression algorithms, MPEG-2 audio coding technique, can code up to 5.1 audio channels and has been widely used for current digital audio broadcasting and multimedia applications.

The existing audio decoder designs are basically based on three kinds of architectures, namely DSP-based, pure-ASIC, and semi-ASIC architectures. The DSP-based approach has the programmable ability and can minimize the time to market, but the cost of each product will be high and the power dissipation is also the problem. Since it's hardware is not the dedicated design for specific audio application, the optimization in software will not be as efficient as that in hardware. Thus it always requires higher operation frequency than the dedicated hardware design in order to meet real-time requirements [4–6].

On the other hand, the pure-ASIC design solves the above problem. But in the audio decoding process, there are many decision-making procedures which are difficult to be implemented in ASIC. As a sequence, it makes the design more complex and not flexible [7, 8].

The semi-ASIC design could provide an alternative solution for this kind of application. For time-consuming and regular operations, a dedicated hardware could be designed for them, while for decision-making operations, an uP-like hardware is a good choice [9]. In this approach, the design is more

cost-effective than the DSP-based design and more programmable than the pure-ASIC design.

In this paper, we present a semi-ASIC architecture for MPEG-2 audio decoding. The target of the proposed design is mainly for the portable and multifunction audio playback devices. Since the major issue to the portable device is the low power consideration, the easiest way for low power design is lower the power supply and the operation frequency and integrate all the functions into one chip. In addition, we will also analyze the computation complexity of each block in decoding process. With this approach, a high efficiency and low cost design can be achieved. This paper is organized as follows. In Section 2, a brief description of MPEG-2 decoding process will be described. The system configuration and detailed implementation for the MPEG-2 decoder will be discussed in Section 3. The performance of the chip and the related simulation result will be shown in Section 4. Finally, the conclusions will be discussed in Section 5.

2. Overview for MPEG-2 Audio Decoder

The MPEG-2 audio bitstream syntax is shown in Fig. 1. It is the frame-based structure with 1152 subband samples per channel. With backward compatibility, the multichannel part of MPEG-2 audio data is put in the ancillary part of MPEG-1. The MPEG-1 compatible part is composed of header, CRC, side information which include the bit allocation information (BAL), scalefactor select information (SCFSI), scalefactor (SCF), and the quantized-rescaled subband samples of basic channel. The multichannel part is similar to the compatible part with some additional multichannel informations which include the transmission channel switching, dynamic cross talk, and multichannel prediction information.

Figure 2 shows the MPEG-2 audio decoding flow. At first, the decoder should synchronize the bitstream at the beginning of the frame for decoding. Then the side information of MPEG-1 audio basic channel is extracted. This information is utilized to dequantize

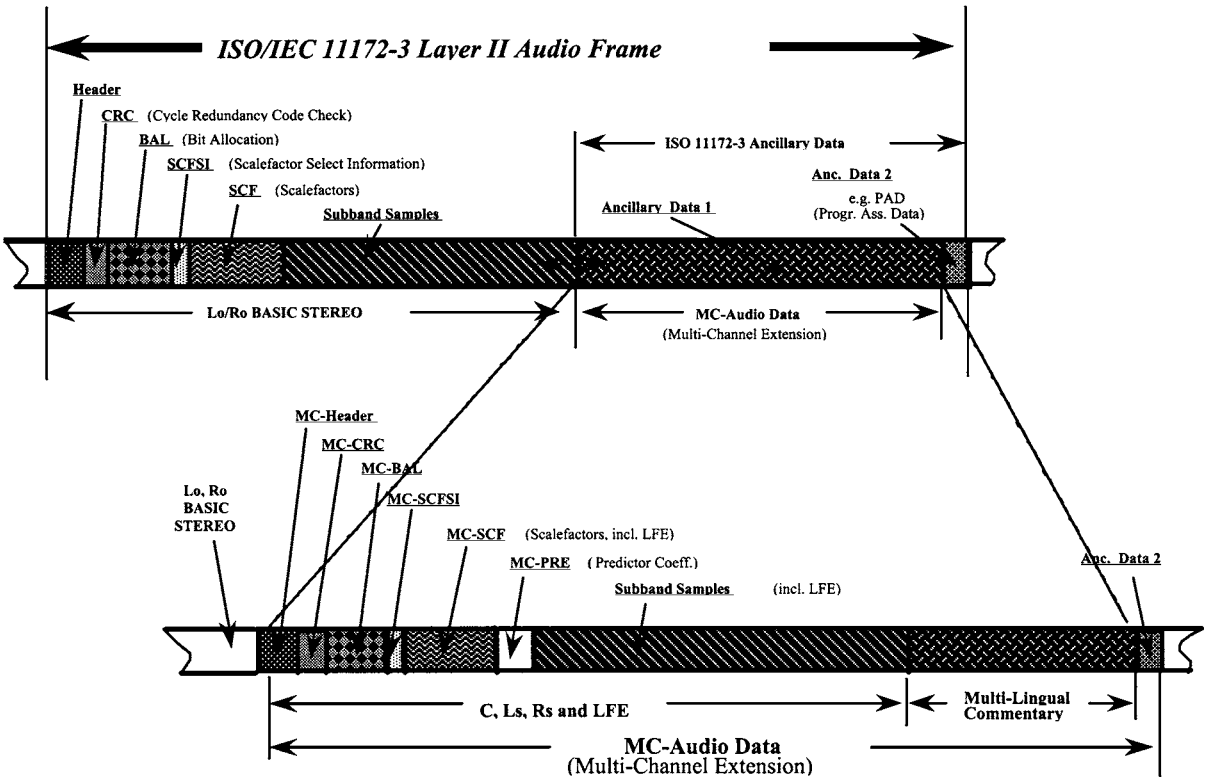

Figure 1. The MPEG-2 audio bitstream syntax.

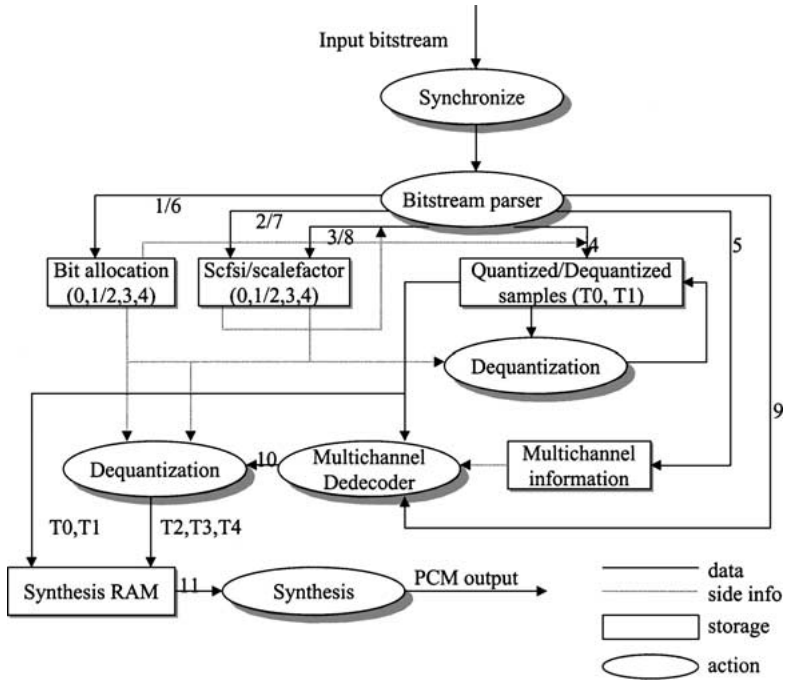

Figure 2. The MPEG-2 audio decoding flow.

and synthesize the subband samples. The next field is the multi-channel part for MPEG-2 audio decoding. According to the multi-channel information and dequantized subband samples of basic channel, the multi-channel process can reconstruct another three channels. After all the subband samples of each channel are ready, the synthesis filterbank could be started to generate the PCM samples which are ready for sound reproduction [1].

3. Proposed Architecture

The computation requirements of each decoding blocks are listed in Table 1. Since the synthesis filterbank takes the most computation power while the others are more decision-making, a dedicated hardware for synthesis filterbank and a RISC processor for the other blocks will be a good design strategy [10]. For some special operations, such as bitstream parsing and degrouping, the dedicated hardware is also offered to improve the performance.

Figure 3 shows the proposed architecture of the MPEG-2 audio decoder. The blocks enclosed in the dashed line are built in one single chip. The program ROM is placed outside the chip for programmability. Bitstream splitter splits the input bitstream into the desired bit-width. Synchronizer & Composer helps to synchronize the input bitstream and compose the two bitstreams into one bitstream. The special divider performs the degrouping process in the MPEG-2 audio decoding. The synthesis filterbank performs the transformation with fully hardware support. All the other blocks are deal with dedicated RISC-core and corresponding to the instruction sequences.

Table 1. Computation power analysis of MPEG-2 audio decoding.

Classification	Function	Required processing power (MOPS)	Total
IQ	Degrouping	0.88	
	Requantization	1.44	
	Rescalization	0.96	3.28
MC	Dematrixing	0.576	
	Denormalization	1.44	2.016
Syn. Subband	IMDCT	61.44	
	IPQMF	19.22	81.36
Total			86.656

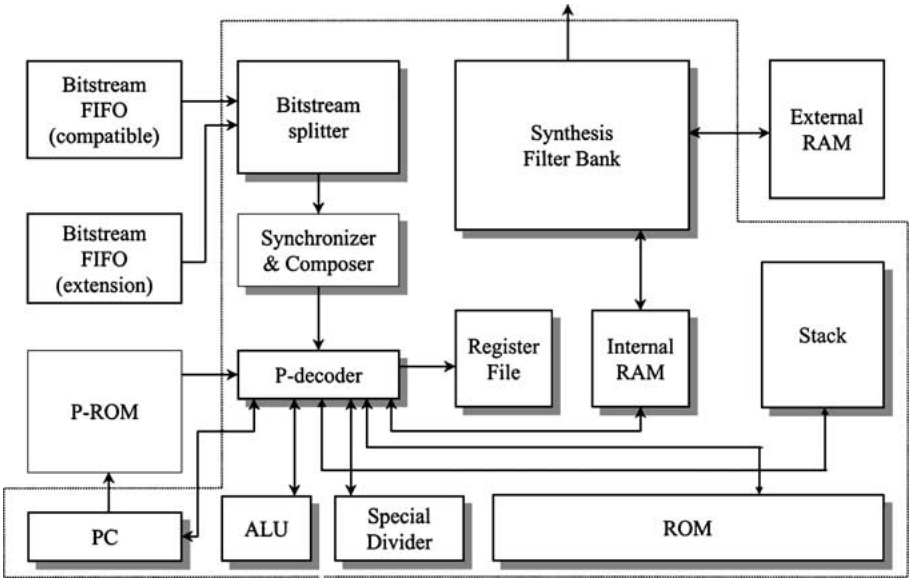

Figure 3. System architecture of MPEG-2 audio decoder.

A. Bitstream Splitter

To achieve high compression ratio, coding the information as short as possible is necessary. Therefore, it is necessary to extract the information with different bit-width in the decoding process. In general purpose DSP, it uses the "and", "or", and "shift" operations to accomplish this task. But it obviously lacks the ability to handle the variable length data.

In our design, the variable-in-constant-out architecture is used to get one token within maximum bit-width in one clock cycle. Figure 4 shows the block diagram of

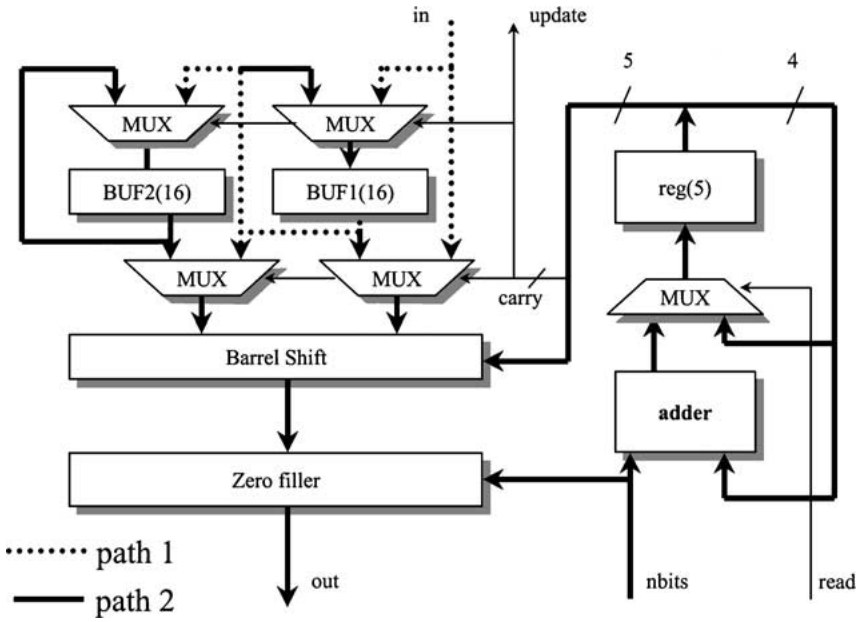

Figure 4. The block diagram of bitstream splitter for audio bitstream.

the bitstream splitter. At the first two clock cycles, the input data will be fed into buffer1 (BUF1) then buffer2 (BUF2), which is totally 32 bits. The adder and reg (5) form an accumulator, which record the number of bits have been read. The barrel shifter is used to shift data right according to the bit number acquired (nbits) and previous read. The zero filler will fill the unused bits from barrel shifter with zeros and send the data out. The four multiplexers are designed for latency free. When more than 16 bits have been read, the buffer2 will run and the accumulator will generate a carry to acknowledge the multiplexers to select the data directly from the input. The buffer1 will shift the data from buffer1 to buffer2, and move the input data to buffer1. At the next clock cycle, the data is ready in bufferl and buffer2 and the path can be redirected from the buffer1 and buffer2.

B. *Composer and Synchronizer*

The synchronizer and composer module is a finite state machine that controls the bitstream splitter directly. Only one command from the RISC processor is needed to synchronize the next frame of the bitstream. It can also merge two bitstreams into one bitstream. From the viewpoint of RISC processor, only one bitstream which is needed to be processed will simplify the task of RISC processor.

C. *Variable-Length Instruction RISC Core*

Since there are many decision-making procedures in MPEG-2 audio decoding, the implementation based on a RISC processor is a good design strategy. The basic instruction length is 8 bits to save chip area. Unfortunately, 8 bits is not enough when there are applied in memory address (16 bits), immediate value (16 bits) and register selections (4 bits). Therefore, variable instruction length design is proposed. Five types of instructions are specified and illustrated in Table 2 and Table 3 in terms of the instruction length and instruction type, respectively.

Figure 5 shows the corresponding RISC core architecture. The register files and memory are separated into several banks with different word length. Some data from MPEG-2 audio bitstream have the length of 4, 6, or 12, not the length of 8 or 16 in general RISC processors. Each bank is optimized for MPEG-2 audio bitstream specification for saving the chip area.

Table 2. The instruction format and the related instruction length.

Length	Format
24 bits	op(4) reg(4) immediate(16)
	op(8) immediate(16)
16 bits	op(4) reg(4) immediate(8)
	op(8) reg(4) reg(4)
	op(8)reg(4) × (4)
	op(l2) reg(4)
	op(8) immediate(8)
8 bits	op(4) reg(4)
	op(4) immediate(4)
	op(3) imm(5)
	op(8)

Table 3. The instruction format and the related instruction type.

Type	Format
op	op(8)
op reg	op(4) reg(4)
	op(8) reg(4)
	op(l2) reg(4)
op imm	op(4) imm(4)
	op(3) imm(5)
	op(8) imm(8)
	op(11) imm(5)
op reg, imm	op(4) reg(4) imm(16)
	op(8) reg(4) imm(4)
	op(4) reg(4) imm(8)
op reg, reg	op(8) reg(4) reg(4)

The control words for the other dedicated hardware are stored in special register files. The instruction sets have been arranged to shorten the most often used instructions. This consideration will also enhance the overall performance.

D. *Special Divider*

In MPEG-2 system, three types of quantization steps, which namely as 3, 5, and 9, are not the multiple of power of 2. It codes three samples with the same step of grouping by using the equation: $s = x + l \times y + l^2 \times z$. The "$x$", "$y$", "$z$" are the three samples, "l" is the

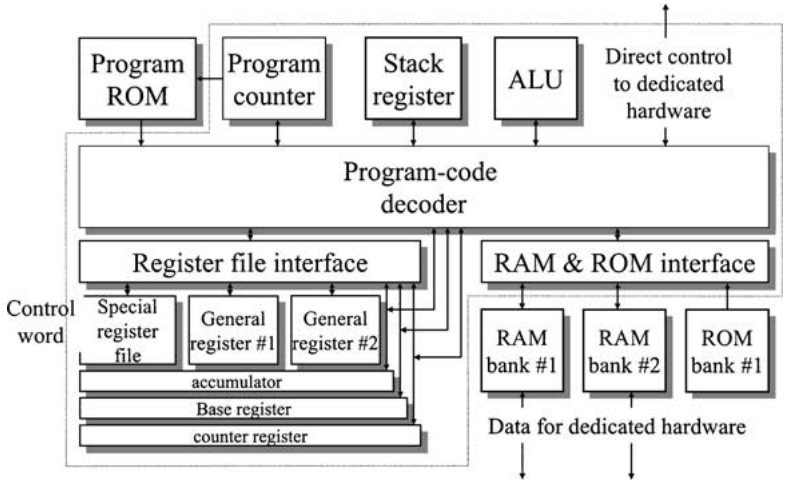

Figure 5. The proposed RISC processor with variable instruction length.

quantization step, and "s" is the coded sample. This grouping technique can provide better compression rate. For instance, if the quantization step which equals to 9, 12 bits are needed to code three samples without grouping. Use grouping, the maximum value of "s" is $8+8\times 9+8\times 9^2 = 728$, therefore only 10 bits are needed to code it.

To decode the original three samples "x", "y" and "z" from "s", the following procedure will be performed: $x = s\,\%\,l$, $s' = s\,/\,l$, $y = s'\,\%\,l$, $s'' = s'\,/\,l$, $z = s''\,\%\,l$. This decoding procedure needs several dividing and modulo computa tion for degrouping the codes. Since in the binary system, division by 2^n can be realized easily, thus the efficient design of the degrouping process is to map this operation into the division by 2^n. Deriving the dividing procedures as follows:

$$\begin{aligned} a &= (2^n+1)q + r \Rightarrow \text{solve } q \text{ and } r \\ a &= 2^n q_1 + r_1 = (2^n+1)q_1 - q_1 + r_1 \\ q_1 &= 2^n q_2 + r_2 = (2^n+1)q_2 - q_2 + r_2 \\ &\vdots \\ q_K &= 2^n q_{k+1} + r_{k+1} = (2^n+1)q_{k+1} - q_{k+1} + r_{k+1} \end{aligned}$$

where $q_{k+1} = 0$, i.e. $q_k = r_{k+1}$ Thus

$$\begin{aligned} a &= (2^n+1)q_1 - q_1 + r_1 \\ &= (2^n+1)q_1 - [(2^n+1)q_2 - q_2 + r_2] + r_1 \\ &= (2^n+1)(q_1 - q_2) + (q_2 - r_2 + r_1) \\ &= (2^n+1)(q_1 - q_2) + [(2^n+1)q_3 - q_3 + r_3] \\ &\quad - r_2 + r_1 \\ &= (2^n+1)(q_1 - q_2 + q_3) + (-q_3 + r_3 - r_2 + r_1) \\ &= \cdots \\ &= (2^n+1)[q_1 - q_2 + q_3 + \cdots + q_k(-1)^{k+1}] \\ &\quad + [r_1 - r_2 + r_3 + \cdots + r_{k+1}(-1)^k] \end{aligned}$$

The q and r are replaced by the sum of q_k and r_k respectively, whereas q_k and r_k are the quotient and the remainder of q_{k-1} divided by 2^n. Thus only hardwired connection is required to get q_k and r_k. Based on this algorithm, an efficient degrouping circuit is shown in Fig. 6. It shows only two adder/subtractors are needed for dividing and modulo computation.

E. Synthesis Filterbank

Since the synthesis filterbank is the most computation-intensive part in the decoding process, therefore an efficient algorithm and dedicated hardware is necessary to reduce the computation overhead. The fast algorithm is shown as follows [11, 12]:

$$\begin{aligned} V_i &= \sum_{k=0}^{31} \cos\left[\frac{(16+i)(2k+1)\pi}{64}\right] \times S_k,\ i = 0 \sim 63 \\ u[i\times 64 + j] &= v[i\times 128 + j] \\ u[i\times 64 + 32 + j] &= v[i\times 128 + 96 + j] \\ S_j &= \sum_{i=0}^{15} U_{j+32i} \times D_{j+32i}, \quad j = 0 \sim 31 \end{aligned} \tag{1}$$

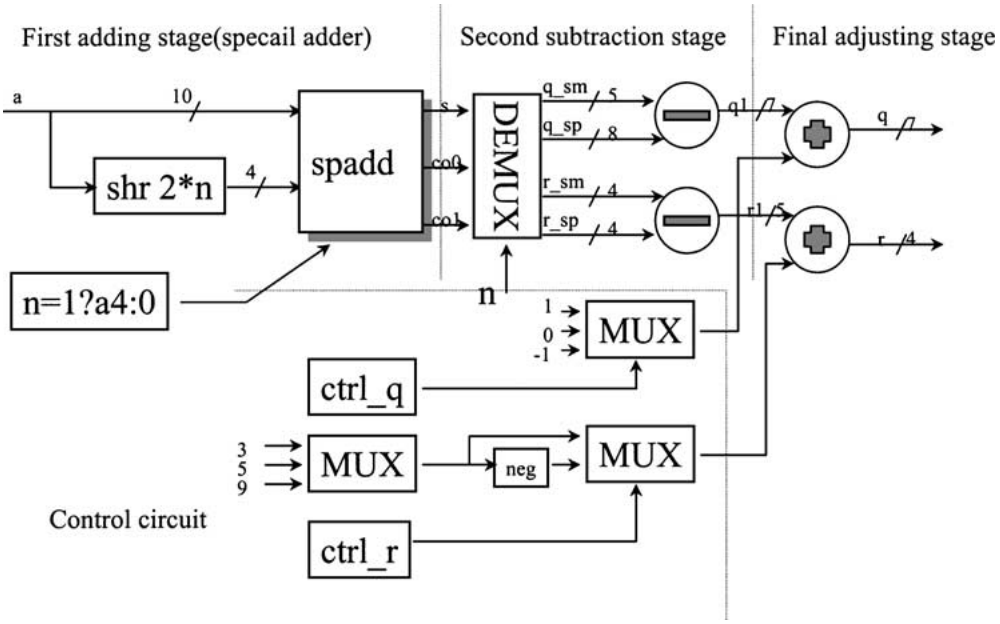

Figure 6. Degrouping circuit for MPEG-2 audio decoder.

Equation (1) can be simplified as follows:

$$v_i = \sum_{k=0}^{15} \cos\left[\frac{(16+i)(2k+1)\pi}{64}\right] \times [S_k + (-1)^i S_{31-k}], \quad i = 0 \sim 63 \qquad (2)$$

Based on the fast synthesis subband algorithm, we use the two-stages architecture to perform this operations. Figure 7 shows the proposed architecture of the synthesis filterbank. At the first pass, the subband samples and cosine coefficients are the inputs of MAC, and the output is stored in the external RAM. At the second pass, the data stored in the external RAM and decoding window coefficients are the inputs to MAC, whereas the outputs are the PCM samples. The address generator and controller will generate the corresponding address and control signal to control the memories, ROMs, and other blocks which are needed to be controlled.

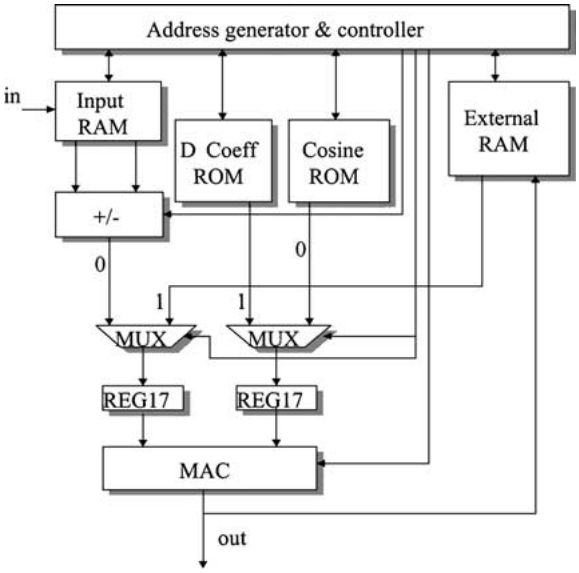

Figure 7. The block diagram of MPEG-2 audio synthesis subband.

4. Design Analysis and Chip Implementation

The word length of the synthesis filterbank determines the quality of PCM output signals. In order to obtain the higher auditory quality with minimum fix-point length, three kinds of samples have been simulated: the normal amplitude signal, the signal with maximum amplitude up to 100% signal level, and the signal amplified from the first one and clipped. Two PSNR calculations are taken as criteria. The first one is to calculate the PSNR frame by frame, and then average them. The second is to calculate the PSNR on overall samples. Seldom large errors will not affect the values in the

Table 4. Simulation result of fix-point analysis.

No	Subband sample	External RAM	Accumulator	Sample type	PSNR1 float/fix		PSNR2 float/fix	
1	−(1, 14)	−(1, 14)	(4, 20)	clipped	97.13	70.12	93.69	13.2
2	−(1, 14)	−(1, 14)	(4,20)	normal	102.11	74.53	98.62	74.29
3	−(1, 14)	−(1, 14)	(4, 20)	critical	100.11	74.39	96.62	40.47
4	−(2, 13)	−(1, 14)	(4, 20)	clipped	97.13	64.79	93.69	18.43
5	−(2, 13)	−(1, 14)	(4, 20)	normal	102.11	69.22	98.62	68.99
6	−(2, 13)	−(1, 14)	(4, 20)	critical	100.11	69.08	96.62	40.46
7	−(0, 15)	−(1, 14)	(4, 20)	clipped	97.13	75.58	93.69	21.44
8	−(0, 15)	−(1, 14)	(4, 20)	normal	102.11	78.68	98.62	78.44
9	−(0, 15)	−(1, 14)	(4, 20)	critical	100.11	78.52	96.62	40.47
10	−(0, 15)	−(2, 13)	(4,20)	clipped	97.13	73.65	93.69	21.44
11	−(0, 15)	−(2, 13)	(4, 20)	normal	102.11	75.38	98.62	76.18
12	−(0, 15)	−(2, 13)	(4, 20)	critical	100.11	76.27	96.62	40.47
13	−(0. 15)	−(0, 15)	(4, 20)	clipped	97.13	73.4	93.69	19.05
14	−(0, 15)	−(0, 15)	(4, 20)	normal	102.11	79.75	98.62	79.50
15	−(0, 15)	−(0, 15)	(4, 20)	critical	100.11	79.54	96.62	40.47
16	−(0, 15)	−(0, 15)	(4, 24)	clipped	97.13	73.63	93.69	18.96
17	−(0, 15)	−(0, 15)	(4, 24)	normal	102.11	80.29	98.62	80.03
18	−(0, 15)	−(0, 15)	(4, 24)	critical	100.11	80.07	96.62	40.47
19	−(0, 15)	−(0, 15)	(0, 28)	clipped	97.13	73.71	93.69	18.99
20	−(0, 15)	−(0, 15)	(0, 28)	normal	102.11	80.32	98.62	80.06
21	−(0, 15)	−(0, 15)	(0, 28)	critical	100.11	80.09	96.62	40.47
22	−(0, 15)	−(0, 15)	(0, 24)	clipped	97.13	73.63	93.69	18.96
23	**−(*0, 15*)**	**−(*0, 15*)**	**(*0, 24*)**	***normal***	***102.11***	***80.29***	***98.62***	***80.03***
24	−(0, 15)	−(0, 15)	(0, 24)	critical	100.101	80.07	96.62	40.47

first calculation too much, but they will seriously affect that of the second calculation. The performance of word length of the external RAM (EXT), accumulator (ACC), and subband samples (SUB) are simulated as illustrated in Table 4. When the input samples are clipped, the PSNR calculation with second method is dropped down. However, when the input samples are normal, the PSNR which are calculated by the first and second one are almost the same. The experiments also show that the increase of word length of integer part does not increase the PSNR in proportion when the input samples are clipped. In addition, the increase of the fractional part does increase the PSNR when the input samples are normal. Obviously, in order to maintain the best quality in most case, the fractional part is more important than the integer part. Based on the simulation, we choose the 23rd result to be applied in our design.

The overall architecture is consisting of about 27000 gate counts by using 0.6 um CMOS single-poly-triple-metal technology and cell-based design style. The die size is 6.4 mm × 6.4 mm. The chip has been fabricated and the tested results show it can run at maximum 43.5 MHz clock rate with 5 V power supply or 33.3 MHz with 3 V power supply. Table 5 lists

Table 5. Chip specification.

Technology	0.6 um SPTM
Die Size	6.4×6.4 mm^2
Package	160 CQFP
Transistor Count	287551
Maximum Freq. and Power Dissipation	43.5 MHz @ 5V, 375 mW
	33.3 MHz @ 3V, 225 mW
	30 MHz @ 3V, 150 mW

Table 6. Performance comparisons between the proposed and other design.

Reference	Approach	Gate Count	Speed	Power	Area	Technology
[9] An ASIC implementation of MPEG-2 decoder	semi ASIC	–	54 MHz	–	–	0.6 um
[6] A Dolby AC-3/MPEG-1 audio decoder core suitable for audio/visual system integration	pure ASIC	325k Transistors RAM120640b	27 MHz	250 mW @3.3 V	6.26×6.26 mm^2	0.35 um triple metal
Normalized result of [6]	pure ASIC	325k Transistors RAM120640b	27 MHz	428 mW @3.3 V	10.7×10.7 mm^2	0.6 um triple metal
[6] An AC-3/MPEG Multi-standard audio decoder IC	DSP(dual)	30k Gates	27 MHz	–	–	TEC3000T CMOS
Our design	semi ASIC	288k Transistors	27 MHz	150 mW @ 3 V	6.4×6.4 mm^2	0.6 um triple metal

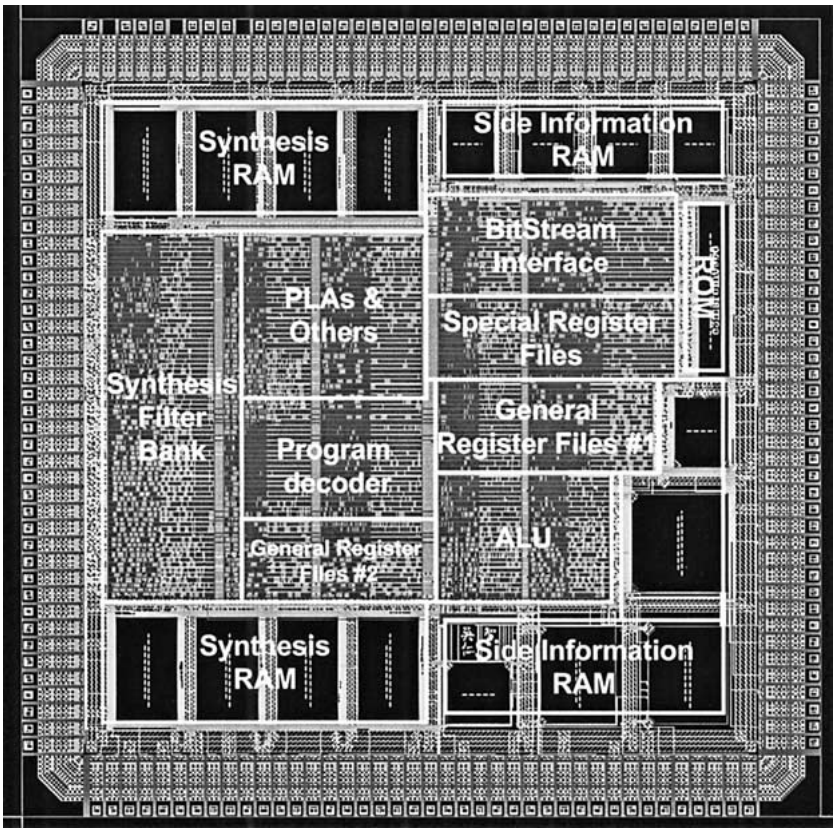

Figure 8. The whole chip layout of MPEG-2 audio decoder.

the chip specification. The whole chip layout is illustrated in Fig. 8. In addition, Table 6 lists the performance comparisons with the other design. Based on the comparisons, Our design achieves the least hardware requirements and power consumption. It is obviously that the proposed design is cost-effective and suitable for some portable digital audio applications which apply MPEG-2 audio coding techniques.

5. Conclusion

In this paper, a semi-ASIC design of MPEG-2 audio decoder is presented. With the well analysis of the decoding flow, a high efficient semi-ASIC architecture and firmware are achieved and implemented. The main features of our design include: i) A modified one-cycle bitstream splitter is proposed for fast bitstream extraction; ii) An efficient synthesis filterbank with less memory usage, clock cycles, and high pipelined structure to achieve a low power and small area design; iii) A divider-free degrouping circuit, and iv) A RISC-core with optimized instruction sets for MPEG-2 audio decoding process. The instruction sets are dedicatedly designed to maximize the performance of the control processing and the communication between all the other dedicated hardware. Based on 0.6 um CMOS technology, the audio decoder can operate at 5 V power supply with 43.5 MHz clock rate, or 3 V power supply with 30 MHz. The power dissipations are 375 mW and 150 mW, respectively.

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