0013-4651/2002/6(2)/F9/3/$7.00 © The Electrochemical Society, Inc.

Growth and Electrical Characteristics of Liquid-Phase Deposited SiO_2 on Ge

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The liquid-phase deposition (LPD) of SiO_2 at 50°C on Ge substrates is investigated. Silicic acid ($SiO_2 \cdot xH_2O$) is used to saturate hydrofluorosilicic acid at 30°C and this shortens the time required for solution preparation to 3 h. The growth rate of LPD oxide on Ge is much slower than that of LPD oxide on Si at the beginning of the deposition process, while surface roughness of LPD oxide on Ge is larger than that of LPD oxide on Si. A metal-oxide-semiconductor tunneling diode on Ge is fabricated using the LPD oxide. The tunneling current of the Ge diodes at inversion bias increases as LPD oxide thickness increases, indicating that the trap density in the LPD oxide increases with increasing oxide thickness, and the current transport is dominated by the trap assistant tunneling.
 [DOI: 10.1149/1.1530030]

Manuscript received September 1, 2002. Available electronically December 3, 2002.

Silicon dioxide (SiO_2) is a most frequently used material in modern ultralarge scale integrated (ULSI) technology. To avoid dopant out-diffusion,[1,2] the low temperature oxide is often required to reduce the thermal budget in device fabrication. Liquid-phase deposition (LPD) has been investigated for the last decade to serve this purpose. Due to the lack of reliable oxide on Ge, the metal-oxide-semiconductor (MOS) structure on Ge cannot be fabricated, and this has restricted the fabrication of some novel devices on Ge substrates. The process of SiGe materials for Si/SiGe heterojunction bipolar transistors[3] and high speed strained Si field effect transistors[4,5] also demands low-temperature insulators to avoid material degradation such as strain relaxation and Ge segregation. The low temperature LPD oxide on Ge can provide good insulators to facilitate device fabrication on the Ge substrate as well as on the Si substrate with SiGe layers. LPD is a promising low-temperature process for SiO_2 formation with the advantages of low thermal budget, low cost, selective growth, and high throughput.[6,7] A simplified mechanism of LPD growth was proposed originally by Nagayama *et al.*[8,9] based on the reaction of H_2SiF_6 with water to form hydrofluoric acid and solid SiO_2

$$H_2SiF_6 + 2H_2O \leftrightarrows SiO_2 + 6HF \quad [1]$$

Several LPD methods were reported. Hydrofluorosilicic acid (H_2SiF_6) was first diluted with water to 2 M. Then silica powder was added to this solution to saturate the solution for 16-20 h at 30°C. After heating the solution to 50°C, boric acid (H_3BO_3) was added to supersaturate the solution with SiO_2. However, the time for solution preparation was too long in this LPD process. LPD oxide films were also obtained by adding Al or boric acid to H_2SiF_6 solution saturated with silica[10] with complicated chemical reactions. In this article we use LPD without Al or H_3BO_3 addition, which was similar to Ref. 11-13. The experimental flow diagram for the LPD process is illustrated in Fig. 1a.

First, silicic acid ($SiO_2 \cdot xH_2O$) was added to hydrofluosilicic acid (H_2SiF_6, 3 mol/L) at 35°C to replace the SiO_2 powder in a conventional LPD process. Since the hydroxyl (OH) abounding in silicic acid makes it more soluble than SiO_2 powder, the saturation time for the solution can be short. In our experiment, the solution stirred for 3 h is sufficient for applications. Next, the solution was filtered to remove the undissolved silica, and a solution saturated with silica was obtained. H_2O was then added to the saturated solution. The H_2O enabled the solution to become supersaturated with silicon oxide. Both 0.4 Ω cm n-type Ge and 1-5 Ω cm n-type Si wafers were used in this experiment to compare the deposition rate of LPD oxide on both substrates. The native oxide was removed by dipping the wafers in diluted HF solution before the LPD process. The substrates were then placed in the immersing solution at 50°C for different growth times. The substrates were then removed from the solution and rinsed with deionized water. Oxide thickness was measured by ellipsometry. Aluminum was evaporated on the LPD oxide as the gate electrode with various circular areas defined by photolithography, and the MOS tunneling structures were fabricated. The solution for Al etching contains H_3PO_3, HNO_3, CH_3COOH, and H_2O in a ratio of 85:5:5:5. No damage to the device was found according to our years' experience. The device structure is shown in Fig. 1b.

The LPD oxide thickness *vs.* growth time on both Si and Ge substrates is illustrated in Fig. 2a. The growth rate of LPD oxide on Si substrates is much higher than that on Ge substrates, especially in the initial 20 nm growth. After 20 nm, the growth rate of LPD oxide on Ge substrate increases, and the growth rate on Ge is similar to that on Si. The result indicates that at the very beginning of the process, it is difficult for SiO_2 to nucleate on Ge substrate as compared to Si substrate. But after 20 nm growth, the deposition process changes from SiO_2 deposition on Ge substrate to SiO_2 deposition on SiO_2, and the growth rate of LPD oxide on Ge substrate starts to increase after initial 20 nm growth. Because the Si substrate is cleaned by HF dip, the surface is almost all terminated with hydrogen.[14] Reoxidation occurs if the surface is exposed to water because the Si-H bond on the surface can react with water molecules with certain time constant and is transformed to Si-OH. Further immersion in hydrofluoric acid transforms the Si-OH back to Si-H. The reactions are described as

$$SiH + H_2O \leftrightarrows Si\text{-}OH + H_2 \quad [2]$$

$$SiOH + HF \leftrightarrows SiF + H_2O \quad [3]$$

$$Si_3\text{-}Si\text{-}F + 5HF \leftrightarrows 3Si\text{-}H + H_2SiF_6 \quad [4]$$

When a substrate is immersed in H_2SiF_6 solution, two competing reactions occur. One is the replacement of Si-H with Si-OH by water (Eq. 2) and subsequent oxidation. The other reaction is the etching of oxide by HF (Eq. 3 and 4). It has been reported that the modification of the surface from Si-H to Si-OH is the main mechanism for the delay time in initial growth.[7] Therefore, we assumed that the same reactions occur on the Ge surface, and the difficulty of changing the Ge surface to form Ge-OH bond is responsible for the longer delay time as compared to Si substrate, because the weak Ge-OH bond can enhance the forward reaction of Eq. 3. Note that there is no obvious adhesive problem in our device process with LPD oxide on Ge substrates. To further study the difference of the LPD oxide on Ge and Si substrates, the surface roughness of LPD oxide was

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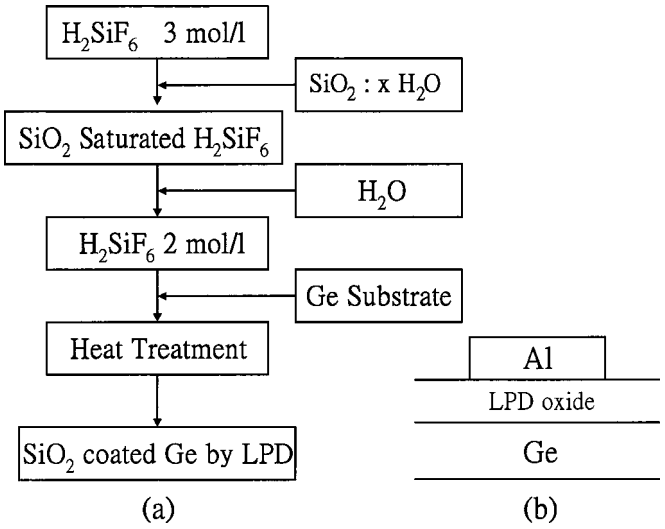

Figure 1. (a) Experimental flow diagram of the LPD process. (b) The Al/LPD oxide/n-type Ge MOS devices.

measured. The surface roughness was measured by atomic force microscope (AFM). Figure 2b shows that the surface roughness of LPD oxide on Ge continues to increase as oxide thickness increases. However, the surface roughness is relatively constant for LPD oxide on Si substrate. This indicates that the initial nucleation of SiO_2 on Si is very dense and uniform, and this leads to a smooth morphology during deposition. Therefore the surface roughness of LPD oxide on Si is small and the roughness is relatively independent of oxide thickness. However, the nucleation of SiO_2 on Ge is not as uniform and dense as on Si. The coarse nucleation yields large island growth before the overlapping between islands. This rough oxide surface can cause extra MOS device leakage.

Figure 3 shows the current voltage (*I-V*) characteristics of Al/LPD oxide/n-Ge diodes with different oxide thicknesses. The oxide roughness of each sample is also indicated in Fig. 3. Since the oxide thickness is measured by ellipsometry, where the flat interface and surface are assumed, the oxide thickness given here is only for reference. Note that the thickness of really rough oxide is not well defined. The circular areas for all devices are 3.2×10^{-4} cm^2. For sufficiently large negative gate voltage at an inversion condition, the gate current is relatively constant in the log scale. There are two current components in this PMOS diode at inversion bias.[15] Figure 4 illustrates these two current transport mechanisms. Since the conduction band discontinuity between Si and Ge is negligible,[16] the bandgap difference falls into the valence band discontinuity. Therefore, the valence band barrier height in Fig. 4 is calculated as 5 eV, given a Ge bandgap of 0.66 eV.[17] The hole current of the

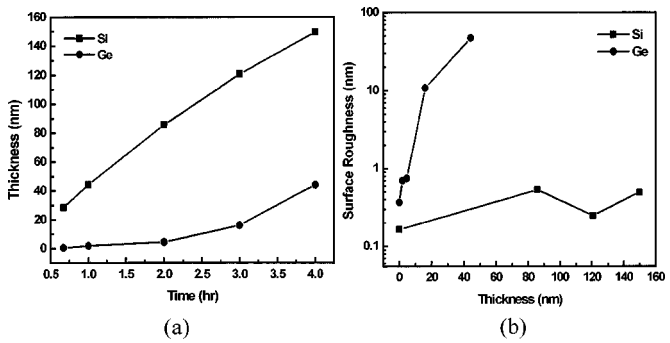

Figure 2. (a) LPD oxide thickness *vs.* growth time on Si and Ge substrates. (b) Surface roughness *vs.* LPD oxide thickness on Ge and Si substrates.

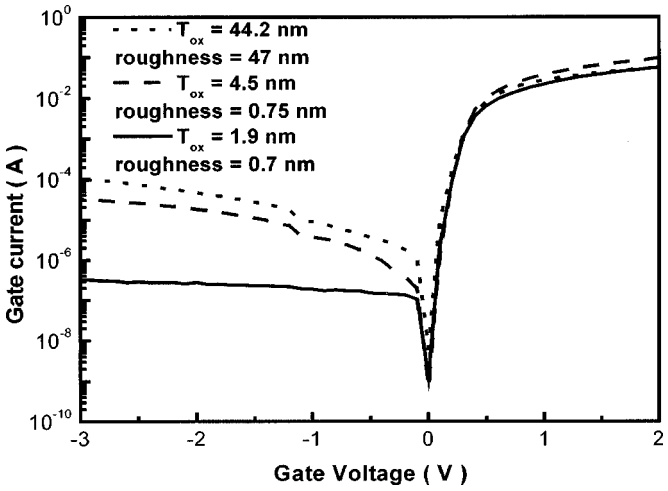

Figure 3. *I-V* characteristics of Ge PMOS diodes with different oxide thicknesses prepared by LPD.

PMOS diode at inversion bias is determined by the minority (hole) generation rate in the deep depletion region, because the tunneling rate through the LPD oxide via traps is sufficiently large at large negative gate bias. The hole concentration at the oxide/Ge interface of the PMOS diode is balanced by the thermal generation rate and the tunneling rate through the oxide. As negative gate bias continues to increase, the hole concentration at the oxide/Ge interface increases slowly and oxide voltage also increases slightly (soft pinning). Since the oxide voltage increases slightly with gate voltage, most gate voltage drops on Ge substrates to form deep depletion in Ge substrates. The oxide voltage also causes the tunneling of electrons from the Al gate electrode to an n-type Ge substrate. However, the soft pinning of oxide voltage at large negative gate bias restricts the further increase of the electron tunneling current, which is strongly dependent on oxide voltage, and the total inversion current is relatively constant in log scale. In Fig. 3, the inversion current increases with LPD oxide thickness. The mechanism that the thick oxide generates large stress at Ge/SiO_2 interface, and creates interface states may be responsible for this. These interface states generate excessive holes at the interface, and increase the leakage current at the inversion bias.

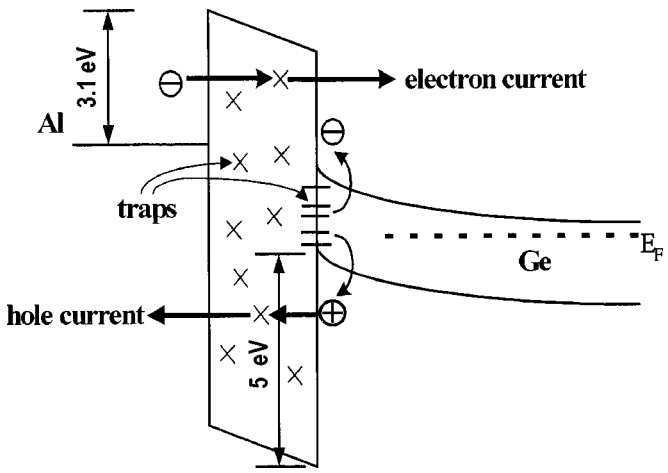

Figure 4. The schematic diagram of inversion current mechanisms for a PMOS diode. The dark current consists of thermal generated hole current and electron current. Note that the conduction bandedge of Si and Ge are at the same position. Therefore most of the bandgap difference between Si and Ge falls in the valence band discontinuity.

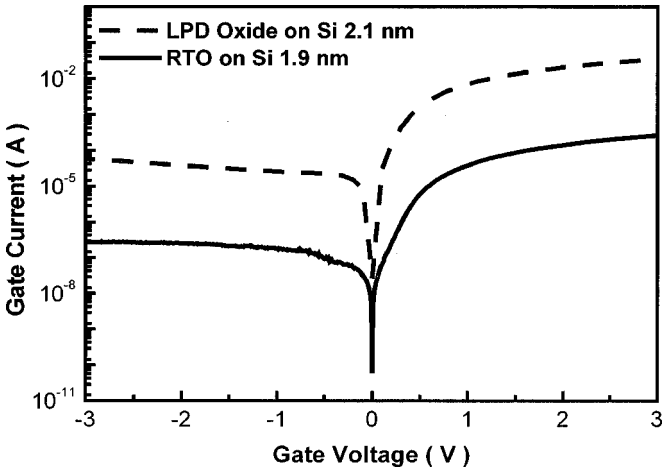

Figure 5. *I-V* characteristics of two devices with RTO and LPD oxide.

The current at an accumulation region (positive gate voltage) shows similar magnitude for different oxide thicknesses. This indicates the transport mechanism is trap-assistant tunneling (Poole-Frenkel effect),[18,19] when the electrons tunnel from Si to Al at positive gate bias. The tunneling rate through LPD oxide is not thickness-dependent, because the trap in the oxide dominates the tunneling rate through the oxide and the carriers can tunnel through oxide via the assistance of multiple traps.

To further confirm our results, the MOS diodes with rapid thermal oxide (RTO) and LPD oxide on Si were also investigated. Note that no thermal oxide can be grown on Ge substrates. Figure 5 illustrates the *I-V* characteristics of two these kinds of MOS diodes on Si substrates. The devices areas are 3.2×10^{-4} cm^2. The oxide thickness is slightly different. RTO oxide is 1.9 nm and LPD oxide is 2.1 nm. From Fig. 5, the devices with LPD oxide have higher gate leakage current (about two orders of magnitude) on both polarities as compared to devices with RTO oxide. The traps in the LPD oxide cause trap-assistant tunneling of gate current, and are responsible for the increase in accumulation current in the LPD oxide. The large interface state density at the Si/LPD oxide interface is responsible for the large inversion current as compared to devices with RTO oxide. Due to the large leakage current, low frequency capacitance-voltage (*C-V*) and quasi-static *C-V* cannot be measured,[20] and the quantitative value of interface states cannot be determined.

In conclusion, a low-temperature LPD process for SiO_2 on Ge substrates was well developed. Silicic acid was used to saturate hydrofluorosilicic acid and the time required for solution preparation was only 3 h. At the beginning of the deposition process, the growth rate for LPD oxide on Ge substrates was slow. The surface roughness for LPD oxide on Ge was larger than that on Si substrates. The inversion current increased with LPD oxide thickness because the thick oxide generated a large stress at the Ge/SiO_2 interface, and created interface states. This LPD process for oxide deposited on Ge can facilitate the integration of SiGe into the Si process.

Acknowledgment

This work is supported by National Science Council, Taiwan, R.O.C. under contract no. NSC 90-2212-E-002-224 and NSC 90-2212-E-002-226.

National Taiwan University assisted in meeting the publication costs of this article.

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