傳輸線模型下之連線效能最佳化

Performance Optimization Under the Transmission Line Model

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一、中文摘要

隨著操作頻率增加到 Giga Hz 以及訊號上升時間小於或相等於訊號從導線的一端傳輸到另一端的時間，傳統利用電阻和電容的 RC 延遲模型(RC delay model)來計算訊號延遲已經不夠準確。因為在這些情況下計算訊號延遲需要考慮到傳輸線以及電感的特性。本計畫之目的為(1)在傳輸線的模型下，發展一個計算時間延遲的解析型公式；(2)對於一條考慮反射效應的傳輸線，找出其最小時間延遲的特性；(3)基於我們所提出計算時間延遲的解析型公式，對導線路徑和繞線樹(routing trees)發展一個有效的時間延遲最佳化的演算法。

關鍵詞：傳輸線模型，RC 延遲模型，RLC 延遲模型

二、英文摘要(Abstract)

As the operating frequency increases to Giga Hertz and the rise time of a signal is less than or comparable to the time-of-flight delay of a line, the traditional RC delay model is no longer accurate, and it is necessary to consider the transmission line behavior and the RLC model for delay computation. We propose in this project (1) to develop an analytical formula for the delay computation under the transmission line model, (2) to explore the properties of the minimum delay for a transmission line with the reflection consideration, and (3) to develop effective and efficient optimization scheme for circuit paths and routing trees based on the analytical formula.

Keywords: Transmission line model, RC delay model, RLC delay model

三、背景和目的

1. Background

As the operating frequency increases to Giga Hertz, the rise time of a signal is less than or comparable to the time-of-flight delay of a line. Also, the die size goes larger. These trends make it important to consider the transmission line behavior for delay computation [1]. When two transmission lines on a chip are connected and these two lines have different characteristic impedance, such mismatches of line impedance can cause reflections from the junction point [1]. Since reflections may cause logic failure or add additional delay, the discontinuities of impedance at junction points must be controlled in order to minimize the side effects of reflections. It is advantageous that a small amount of ringing could help to decrease delay [9]. Therefore, in practice, it is desirable to correctly transmit a signal between the two end points of a transmission line within one round trip, and the first undershoot must be sufficiently small to maintain the signal level.

Transmission phenomenon becomes significant when $t_r < 2.5t_f$, where t_r is the rise time and t_f is the time of flight determined by the line length l divided by the velocity v [1]. On one hand, if the driver resistance is larger than the line impedance, it requires multiple trips to switch the load; on the other hand, if the driver resistance is smaller than the line impedance, the load may be falsely triggered. We can eliminate the reflections by matching the driver resistance and the line impedance. Because the resistance of a gate or the impedance of a wire is inversely proportional to its width, gate sizing and wire sizing can affect the delay. Thus, sizing circuit components (buffer and wire) can optimize delay under reflection constraints.

Timing is a major concern in the high performance circuits. Many techniques such as wire sizing and gate sizing have been proposed to optimize timing (e.g., [3, 4, 10], etc); however, these techniques are all based on the Elmore delay model [6]. Not much work in the literature considers the minimization of delay under the transmission line model. The algorithm presented in [8] applies continuous wire-sizing to minimize delay under the transmission line model; however, they did not consider the influences of reflections. Besides, there are several previous works that develop modeling and analysis techniques for the simulation and timing characterization under the transmission line model, e.g., [7, 13, 14, 15, 19], but they do not consider delay optimization.

2. Objective

In this project, we focus on the performance optimization and avoid the false switching due to reflections. We shall first develop an analytical formula for the delay computation under the transmission line model and conduct extensive simulations with SPICE to show the accuracy of the formula for transmission lines (both of the lossy and the lossless transmission lines). Based on this formula, we shall explore the properties of a transmission line with reflection considerations. Then, we shall develop an effective and efficient optimization scheme for circuit paths and routing trees based on the analytical formula.

3. Transmission Line Model

When the rise time of a signal is less than or comparable to the time-of-flight delay from one end of a wire to the other end, the wire should be modeled as a transmission line.

3.1. Gate and Wire Modeling

Figure 1 illustrates the gate and the lossy transmission line models used in this project. For a gate i with size g_i, the gate resistance r_i^b is $\hat{r}_b / g_i$ and the gate capacitance c_i^b is $\hat{c}_b g_i$, where $\hat{r}_b$ and $\hat{c}_b$ are the unit-sized resistance and unit-sized capacitance of a gate, respectively.

A uniform lossy transmission line i of width w_i can be represented by a serial sections of unit-length resistance,

$\hat{r}_w / w_i$, unit-length inductance, $\hat{u}_w / w_i$, and unit-length capacitance, $\hat{c}_w w_i$, where $\hat{r}_w$, $\hat{u}_w$, and $\hat{c}_w$ are the sheet resistance, the unit-sized inductance, and the unit-sized capacitance of a wire, respectively. The effect of inductance and capacitance can be represented by a characteristic impedance, Z_i, which equals $\sqrt{\hat{u}_w} / (w_i \sqrt{\hat{c}_w})$. The propagation velocity of a wire i, v_i, equals $1/\sqrt{\hat{u}_w \hat{c}_w}$ [1]. If the length of a wire is l_i, its total resistance, total inductance, and total capacitance are $\hat{r}_w l_i / w_i$, $\hat{u}_w l_i / w_i$, and $\hat{c}_w w_i l_i$, respectively.

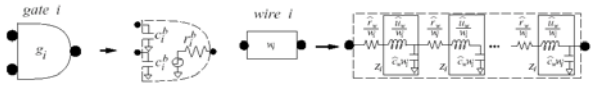

Figure 1: A gate is the loading of its upstream, but is the driver of its downstream. A lossy transmission line is represented by a serial of its resistance, inductance, and capacitance, or we can merge each section of inductances and capacitances into a characteristic impedance.

Therefore, with the gate and the lossy transmission line models, we can represent a circuit path by resistors, capacitors, and characteristic impedance. Figure 2 illustrates the resulting circuit modeling for a circuit path with n buffers, where R_S and C_L are the resistance of source and the capacitance of load, respectively.

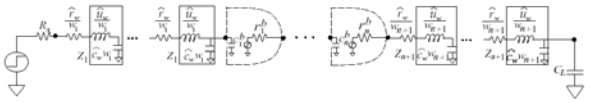

Figure 2: A circuit path is a combination of resistors, capacitors, and characteristic impedance.

3.2. Reflections on a Wire

As shown in Figure 3, the gate i-1 drives lossy transmission line i and gate i. Inductive and capacitive discontinuities may occur at the points *A* and *B*. Due to the inductive and capacitive discontinuities, the resulting reflections may cause logic failure or excessively longer delay [1]. The initial voltage at the point B is the sum of the signal sent out from the point A and the reflection generated at the point B. When the reflection generated at the point B travels backward to the point A, a new reflection generated at the point A is transmitted toward to the point B. The new voltage at the point B is the sum of the incoming reflection, the new outgoing reflection, and the initial voltage. As shown in Figure 4(a), the initial voltage at point B does not reach the threshold voltage. Thus, multiple round trips along the line may be required to correctly transmit a signal. As shown in Figure 4(b), if the reflection generated at the point A is negative, the voltage may oscillate at the point B, causing *overshoot* or *undershoot*. This oscillating pattern is called *ringing*.

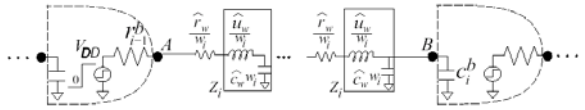

Figure 3: The resistor with resistance r_{i-1}^b drives a lossy transmission line with characteristic impedance Z_i and a capacitor with capacitor c_i^b.

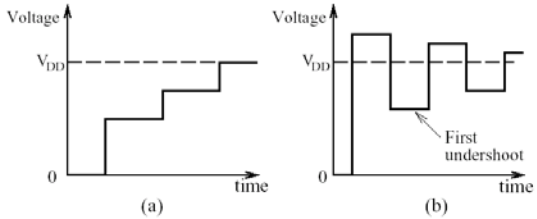

Figure 4: (a) Multiple trips are required to correctly transmit a signal. (b) Ringing may cause logic failures.

3.3. Voltage Attenuation on a Wire

On-chip interconnections and some thin film package wires, however, have significant resistance, and they should be treated as lossy transmission lines [5, 16]. When the line resistance becomes larger than the characteristic impedance, resistance dominates the electrical behavior, and the inductive effects disappear. Then the wire should be modeled as a distributed RC line [1, 11].

In a lossy transmission line, the resistance of a line causes voltage attenuation, and the voltage attenuation coefficient γ_i along a lossy transmission line i is derived in [1] as follows:

$$\gamma_i = e^{-\frac{\left(\frac{\hat{r}_w l_i}{w_i}\right)}{2Z_i}} = e^{-\frac{\hat{r}_w l_i \sqrt{\hat{c}_w}}{2\sqrt{\hat{u}_w}}}. \quad (1)$$

Therefore, in Figure 3, the voltage at the point B before reflection is given by

$$V_B = \gamma_i V_A. \quad (2)$$

3.4. When to Use Transmission Line Analysis

According to [1, 11], the transmission line behavior is significant when

$$t_r < 2\, t_f, \quad (3)$$

and

$$Rl \leq 2\, Z_0, \quad (4)$$

where $t_r = 2.2 r_{i-1}^b \left(\hat{c}_w w_i l_i + c_i^b\right)$ is the rise time of wire i, $t_f = l_i / v_i$ is the time-of-flight delay, $Rl = \hat{r}_w l_i / w_i$ is the total resistance, and $Z_0 = Z_i$ is the characteristic impedance. As illustrated in Figure 6, we can rewrite Inequalities (3) and (4) as Inequalities (5) and (6) as follows:

$$2.2\, r_{i-1}^b (\hat{c}_w w_i l_i + c_i^b) < 2\, \frac{l_i}{v_i}, \quad (5)$$

and

$$\frac{\hat{r}_w l_i}{w_i} \leq 2\, Z_i. \quad (6)$$

Besides, to make the voltage at the point B correctly drive the gate i, the voltage at the point B after infinite

reflections should be greater than or equal to V_t. In other words, the following inequality must be satisfied.

$$\begin{aligned} V_B &= 2\alpha_{i-1,i}\gamma_i(1+\gamma_i^2\beta_{i-1,i}+\gamma_i^4\beta_{i-1,i}^2+\ldots)V_{DD} \\ &= \frac{2\alpha_{i-1,i}\gamma_i V_{DD}}{1-\gamma_i^2\beta_{i-1,i}} \\ &\geq V_t, \end{aligned} \quad (7)$$

where

$$\begin{aligned} \alpha_{i-1,i} &= \frac{Z_i}{r_{i-1}^b + Z_i} \\ \beta_{i-1,i} &= \frac{r_{i-1}^b - Z_i}{r_{i-1}^b + Z_i} \\ \gamma_i &= e^{-\frac{\hat{r}_w l_i \sqrt{\hat{c}_w}}{2\sqrt{\hat{u}_w}}}. \end{aligned}$$

Therefore, we should model a line as a lossy transmission line if Inequalities (5)--(7) are satisfied; it should be modeled as a distributed RC line, otherwise.

四、研究方法

We shall in this form discuss the problem formulation, delay model, Buffer and Wire Sizing for a Circuit Path, and Buffer and Wire Sizing for a Routing Tree.

1. Problem Formulation

In this project, we shall first develop an analytical formula for the delay computation under the aforementioned transmission line model with the reflection consideration and then develop an effective and efficient delay optimization scheme by sizing the components of circuit paths or routing trees based on the analytical formula. We formulate this problem as follows:

- *Input: A circuit path/routing tree and the lower and upper bounds for buffer and wire sizes.*
- *Objective: Determine the optimal buffer and wire size for each segment in a circuit path/routing tree, so that delay is minimized.*

2. Delay Model

The time t_c for charging the capacitive load (defined at 50% of the final value) of the lumped network equals $\ln 2 R_p C_L$, where R_p is the pullup resistance and C_L is the total capacitive load [16, 17, 18]. According to [1], the current that a lossless transmission line can supply is limited by its characteristic impedance. As a result, looking from the receiving end, the line behaves like a resistor with a value Z_0. In a lossy transmission line, not only its characteristic impedance, but also its partial resistance of the line that causes voltage attenuation supplies the current. If the total resistance of a line causes voltage attenuation, the voltage at the receiving end becomes zero. We know that the voltage at the receiving end V_B equals $\gamma_i V_A$ in Figure 3. This implies that there is only $(1-\gamma_i)$ percentage of the total resistance for the line between nodes A and B, r_{i+1}, causing voltage attenuation. Consequently, the pullup resistance R_i for the transmission line is equal to the sum of the characteristic impedance of the line, and partial resistance of the wire, which causes voltage attenuation. We have the pullup resistance R_i for the line as follows:

$$R_p = Z_i + (1-\gamma_i)\frac{\hat{r}_w l_i}{w_i}. \quad (8)$$

Hence, the time t_c for charging the capacitive load of a transmission line is given by

$$t_c = \ln 2 \left(Z_i + (1-\gamma_i)\frac{\hat{r}_w l_i}{w_i}\right) c_i^b. \quad (9)$$

Because the delay computed by Equation (15) is defined at 50% of the final voltage, and the final voltage at the receiving end after reflection may not equal V_{DD}. Therefore, we should normalize t_c by dividing it by the final voltage $V_{DD}^{'}$, which equals $\frac{2Z_i}{r_{i-1}^b + Z_i}\gamma_i$. Therefore, we have

$$\begin{aligned} t_c^{'} &= \ln 2 \left(Z_i + (1-\gamma_i)\frac{\hat{r}_w l_i}{w_i}\right) c_i^b \Big/ \left(\frac{2\gamma_i Z_i}{r_{i-1}^b + Z_i}\right) \\ &= \eta_i \left(r_{i-1}^b + \frac{\sqrt{\hat{u}_w}}{w_i\sqrt{\hat{c}_w}}\right) c_i^b, \end{aligned} \quad (10)$$

where

$$\begin{aligned} \eta_i &= \frac{\ln 2\left(e^{\theta_i} + 2\theta_i\left(e^{\theta_i}-1\right)\right)}{2} \\ \theta_i &= \frac{\hat{r}_w l_i \sqrt{\hat{c}_w}}{2\sqrt{\hat{u}_w}}. \end{aligned}$$

Because transmission line analysis always gives the correct answer irrespective of the rise time of the driver, delay is the sum of the time-of-flight t_f along the wire, and the time $t_c^{'}$ for charging the capacitive load [1, 16]. Thus, the propagation delay $\Delta(g_{i-1}, g_i)$ from the gate g_{i-1} to the next gate g_i in Figure 3 is given by

$$\Delta(g_{i-1}, g_i) = (2n-1)\frac{l_i}{v_i} + \eta_i \left(r_{i-1}^b + \frac{\sqrt{\hat{u}_w}}{w_i\sqrt{\hat{c}_w}}\right) c_i^b \quad (11)$$

where n is the number of required round trips to correctly transmit a signal.

3. Buffer and Wire Sizing for a Circuit Path

3.1. Reflection Considerations

In practice, designers typically desire to optimize performance without generating undesirable reflections and transmit a signal correctly within a limited number of round trips. As the VLSI technology advances, the wire length is increasing and the capacitance of a gate is decreasing, making the time-of-flight delay dominate the delay. Therefore, we have the following theorem for the optimal number of round trips for delay optimization.

Theorem 1: The minimum delay for a circuit path with reflection occurs when the number of round trips equals one.

Thus, we can rewrite Equation (11) as follows:

$$\Delta(g_{i-1}, g_i) = l_i\sqrt{\hat{u}_w\hat{c}_w} + \eta_i \left(r_{i-1}^b + \frac{\sqrt{\hat{u}_w}}{w_i\sqrt{\hat{c}_w}}\right) c_i^b, \quad (12)$$

where

$$\eta_i = \frac{\ln 2\left(e^{\theta_i} + 2\theta_i\left(e^{\theta_i} - 1\right)\right)}{2}$$

$$\theta_i = \frac{\hat{r}_w l_i \sqrt{\hat{c}_w}}{2\sqrt{\hat{u}_w}}.$$

3.2. Optimal Wire Sizing

In this section, we minimize the delay of a circuit path by wire sizing. If all buffer sizes and locations are fixed, the delay function of a circuit path from the source s to sink t with n+1 segments (w_1, …, w_{n+1}) can be calculated as follows:

$$\begin{aligned}\Delta(s,t) &= \sum_{i=1}^{n+1} l_i\sqrt{\hat{u}_w\hat{c}_w} + \eta_1\left(R_S + \frac{\sqrt{\hat{u}_w}}{w_1\sqrt{\hat{c}_w}}\right)c_1^b \\ &+ \sum_{i=2}^{n}\eta_i\left(r_{i-1}^b + \frac{\sqrt{\hat{u}_w}}{w_i\sqrt{\hat{c}_w}}\right)c_i^b \\ &+ \eta_{n+1}\left(r_n^b + \frac{\sqrt{\hat{u}_w}}{w_{n+1}\sqrt{\hat{c}_w}}\right)C_L, \qquad (13)\end{aligned}$$

where

$$\eta_i = \frac{\ln 2\left(e^{\theta_i} + 2\theta_i\left(e^{\theta_i} - 1\right)\right)}{2}$$

$$\theta_i = \frac{\hat{r}_w l_i \sqrt{\hat{c}_w}}{2\sqrt{\hat{u}_w}}.$$

Notice that Equation (13) is a posynomial function in w_1, …, w_{n+1}, implying that the wire-sizing problem has a unique global minimum [2]. Thus, we can apply any efficient search algorithm, such as the well-known gradient search procedure, to find a locally optimal solution and thus the globally optimal solution.

3.3. Optimal Buffer Sizing

Similar to wire sizing, assume that all wire sizes and buffer locations are fixed, the delay function of a circuit path from the source s to sink t with n segments (g_1, …, g_n) can be calculated as follows:

$$\begin{aligned}\Delta(s,t) &= \sum_{i=1}^{n+1} l_i\sqrt{\hat{u}_w\hat{c}_w} + \eta_1\left(R_S + \frac{\sqrt{\hat{u}_w}}{w_1\sqrt{\hat{c}_w}}\right)\hat{c}_b g_1 \\ &+ \sum_{i=2}^{n}\eta_i\left(\frac{\hat{r}_b}{g_{i-1}} + \frac{\sqrt{\hat{u}_w}}{w_i\sqrt{\hat{c}_w}}\right)\hat{c}_b g_i \\ &+ \eta_{n+1}\left(\frac{\hat{r}_b}{g_n} + \frac{\sqrt{\hat{u}_w}}{w_{n+1}\sqrt{\hat{c}_w}}\right)C_L, \qquad (14)\end{aligned}$$

Notice that Equation (14) is also a posynomial function in g_1, …, g_n, implying that the buffer-sizing problem has a unique global minimum [2]. Thus, we can apply any efficient search algorithm, such as the well-known gradient search procedure, to find a locally optimal solution and thus the globally optimal solution.

3.4. Optimal Simultaneous Buffer and Wire Sizing

Again, assume that all buffer locations are fixed, the delay function of a circuit path from the source s to sink t with 2n+1 segments (w_1, …, w_{n+1}, g_1, …, g_n) is the same as Equation (14).

Notice that Equation (14) is also a posynomial function in w_1, …, w_{n+1}, g_1, …, g_n, implying that the simultaneous wire- and buffer-sizing problem has a unique global minimum [2]. Thus, we can apply any efficient search algorithm, such as the well-known gradient search procedure, to find a locally optimal solution and thus the globally optimal solution.

五、成果 (Publications)

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2. T.-C. Chen, S.-R. Pan, and Y.-W. Chang, ``Performance optimization by wire and buffer sizing under the transmission line model," in Proc. of IEEE International Conference on Computer Design (ICCD-01), pp. 192--197, Austin, TX, Nov. 2001.
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