A 100MHz Timing Generator for Impulse Radio Applications

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Abstract — **The timing generator is used to generate a 100MHz timing signal for impulse radio system with timing resolution of 19.5ps controlled by 9-bit digital input. A fine phase interpolator is used to generate one of the 32 interpolated phases by using common gate buffered switch techniques. The timing generator achieves ± 0.3LSB differential nonlinearity and ±2LSB integral nonlinearity. The chip is fabricated in a standard 0.35 μ m CMOS process and consumes 55mW power from a 3V supply. The chip area including pads occupies 1.5x1.5mm^2.**

I. INTRODUCTION

Sinusoidal signals have been widely used in most of the wireless communication systems, such as GSM, W-CDMA, etc. However, traditional sinusoidal radios suffer from many problems including extreme sensitivity to multi-path propagation effects and time dependent fading. One solution to this problem is to use impulse radio, consisting of very narrow impulses on the order of sub-nanoseconds and spreading over a very broad bandwidth in frequency. Impulse radio can be classified as one kind of signaling called "Ultra-Wideband", which has recently been approved to be used in the band from 3.1 GHz to 10.6 GHz, but also below 960 MHz for imaging application, at power levels similar to FCC Type 15 regulations. The differences in time domain and frequency domain between a narrowband wireless communication system and an impulse radio system are simply illustrated in Fig. 1. Besides wireless data communication, impulse radio can also be used in a location detection system with accuracy around the order of centimeters.

A simplified impulse radio transceiver system block diagram is shown in Fig. 2[1]. In the transmitter, the timing generation circuit generates a programmable time delay signal based on the correct code and modulation to trigger the pulse generator to generate the pulses at the desired time. The quality of the transmitted signal is directly related to how precise the timing signal is. At the receiver end, the received pulses are correlated with the expected impulses, i.e. the pulse template, controlled by the timing signal generated by the timing generator. The timing offset between the received pulse and the pulse template will apparently affect the results of the correlator and degrade the output signal-to-noise ratio of the receiver [2]. System level timing jitter will affect the tradeoff between coding gain, data rate, and multiple access of the system. Jitter of the timing signal can be modeled as an additive white Gaussian noise

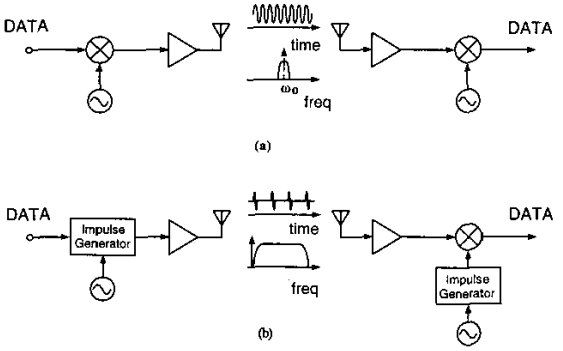

Fig.1 Time domain and frequency domain of (a) traditional narrowband radio and (b) impulse radio systems

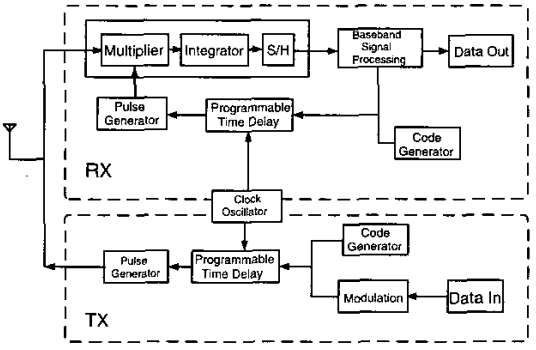

Fig.2 Block diagram of an impulse radio transceiver system

process in the receiver, and will also decrease the received signal-to-noise ratio [2]. For the reasons as stated above, the timing generator is one of the most important components in the impulse radio communication system. The proposed timing generator can be used to generate a programmable delayed 100MHz timing signal controlled by 9-bit digital word for a typical impulse radio system and the resolution is 19.5ps(i.e. 0.7degree phase). In section 2 we will describe the circuit architecture of the proposed timing generator. The modified phase detector and the charge pump are expounded in section 3. Section 4 states the phase selector and the improved phase interpolator. The experimental results are shown in section 5. Finally, a simple conclusion is drawn in section 6.

II. THE CIRCUIT ARCHITECTURE

Fig.3 shows the circuit architecture of the proposed timing generator. The core delay locked loop is locked

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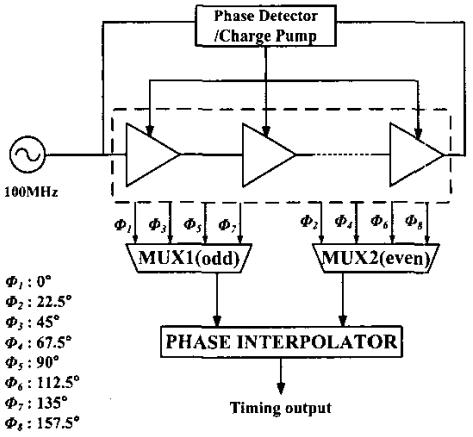


Fig.3 Circuit architecture of the timing generator

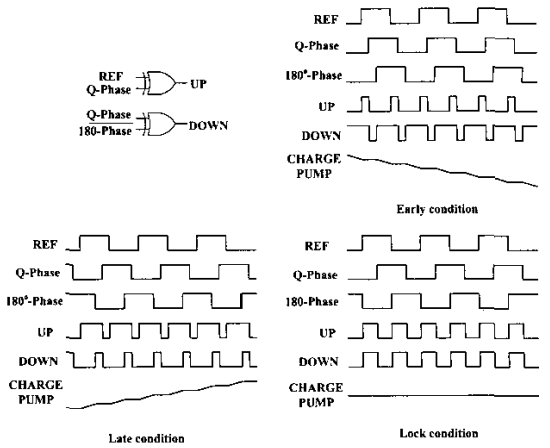


Fig.4 The operation of the modified PD and charge pump

at 180° phase shift. The delay line of the core DLL is composed of 8 delay stages and 8 output timing signals equally spaced by 625ps can be acquired when the reference clock is 100MHz. The multiplexer MUX1 selects one of the odd clock phases and the multiplexer MUX2 selects one of the even clock phases. The multiplexers can also alternate the polarity of the input signal so all the programmable timing signals in one clock can be generated by the timing generator. The selected odd clock phase and the selected even clock phase are exactly 625ps apart, and the 5-bit phase interpolator is used to generate the interpolated timing signal with 19.5ps resolution which is equivalent to 0.7° phase resolution. When the timing generator circuit is used in an impulse radio system with location detection, 19.5ps resolution is equivalent to about 0.6cm location accuracy.

III. The Modified Phase Detector and Charge Pump

When an XOR gate is used as the phase detector, the reference input clock and the feedback signal comes from the voltage control delayed line in a DLL will be locked at quadrature phase. The phase detector we modified and the simplified charge pump is shown in Fig.4. It is composed of 2 XOR gates which compare the reference clock, the feedback Q-phase signal, and the 180°-phase signal, and produces the pump-up pulses and the pump-down pulses. Under the lock condition as shown in Fig.4, the pump-up pulses and the pump-down pulses will cancel each other so the charge pump output remains the same level without any ripples that will induce offset between the output clock phase and the ideal clock phase when using just one XOR[3]. On the other hand, the modified phase detector will double the comparison rate of the phase detector. The output of the PD and charge pump is shown as below,

$$\Delta V_{cp} = 2 \times \frac{I_{cp} \cdot \theta_e}{C_{cp} \omega_{clk}}$$

where I_{cp} and C_{cp} are the tail current and the output capacitance of the charge pump. There are several drawbacks in the conventional CMOS single-ended charge pumps. Firstly, the inherent mismatches between PMOS transistors and NMOS transistors will induce periodical ripples at the charge pump output as well as unwanted offset in the delay line. Secondly, the inevitable single inverter delay between the UP and the DOWN outputs used to drive PMOS and NMOS switches will also give rise to periodical ripples at the charge pump output. Thirdly, the output operating range is quite limited for single-ended charge pumps when they are used in low voltage operation. However, the disadvantages listed above could be overcome by using a fully differential charge pump. The matching requirements between NMOS and PMOS transistors are relaxed to the matching between NMOS or between PMOS transistors. There is no inevitable delay between the UP and the DOWN signals because of the fully symmetric operation in the differential charge pump. The output operating range can also be doubled by using the differential charge pump. Moreover, the differential charge pump provides better immunity to the supply, ground and the substrate noise when an on-chip loop filter is used.

A fully differential charge pump is used in the DLL we proposed. In order to achieve fully symmetric operation in the fully differential charge pump, the modified XOR gate can also provide differential outputs to drive the charge pump. In the traditional symmetric XOR gate [3], the drains of the four input transistors are connected to the power supply and only single-ended output is provided. However, the differential output can be obtained when we simply connect the drains of the four input transistors together to an added active load, and add a current source to draw the same current as the other two current sources from this node to the ground as shown in Fig.5. With this complementary output, an

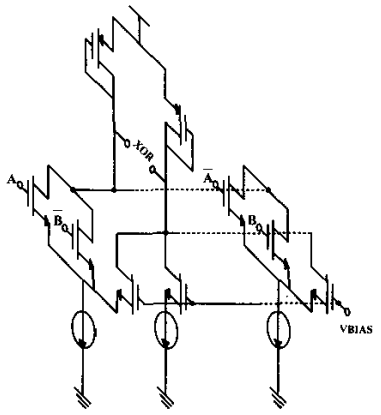


Fig.5 The modified XOR gate

when the phase detector is connected to the charge pump. With the fully differential output from the phase detector, the fully differential charge pump, the proposed DLL can provide exact symmetric operation. Under the locked condition of the DLL with the proposed phase detector and charge pump, the pump-up and the pump-down pulses can exactly cancel each other according to simulation.

IV. The Delay Cell and V-I Converter

The delay buffer used in this design is based on a differential source coupled pair with symmetric load elements which have good immunity to the supply noise. Because the charge pump we use is a fully differential circuit, a differential voltage to current converter [4] is used to generate the current source bias voltage for the delay buffers in the voltage controlled delay line. The voltage to current converter has good common mode noise rejection as long as the output voltage level of the charge pump is carefully designed.

V. The Phase Selection Multiplexer and Phase Interpolator Circuit

The phase selection multiplexer is all composed of 2-1 multiplexers as shown in Fig.6(a). When the control signal V_{c1} is high, the switch transistors M_{s11}, M_{s12}, M_{s13}, and M_{s14} are turned on and the differential input signal *Input1* will be cancelled out by itself at the output of the multiplexer; on the other side, the switch transistors M_{s21} and M_{s22} are turned off with the switch transistors M_{s23} and M_{s24} are still left turned on and the input signal *Input2* will be delivered to the output. The data-dependent loading effect between the multiplexers and the VCDL can be eliminated because the input transistors are never turned off and the buffers between the multiplexers and the voltage controlled delay line can be saved. Also, coupling from the output of the multiplexers to the input is removed due to the isolation provided by the common gate buffered switch transistors. Because the input and the output of the

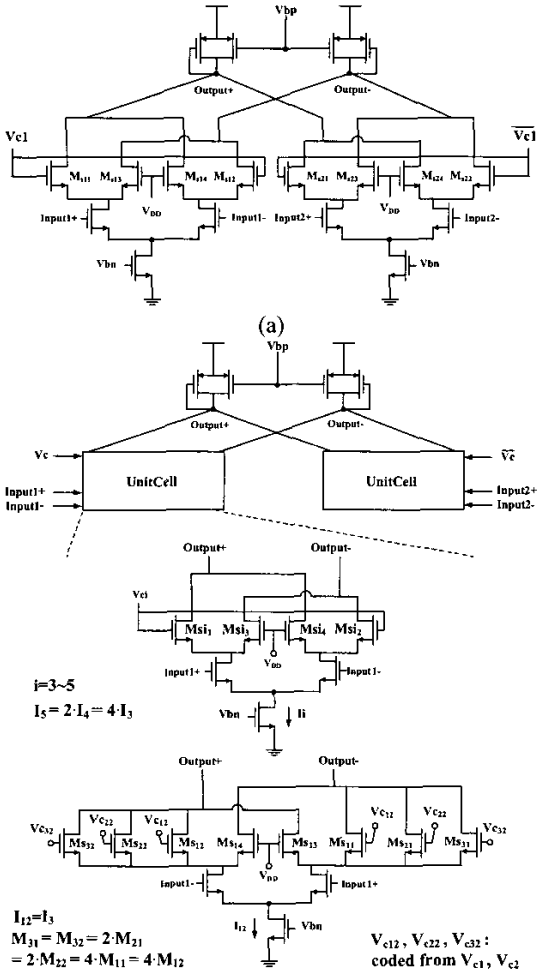


Fig.6 The circuit of (a) 2-1 multiplexer and (b) 5-bit phase interpolator

VCDL are 180° out of phase under the condition of locking, phase inversion multiplexers are needed to cover the whole 360° range. This can be easily achieved when we connect the control signal V_{c1} and $\overline{V_{c1}}$ to high, the gates of the transistors M_{13} and M_{14} to the control signal V_{c1} , and the gates of the transistors M_{23} and M_{24} to the control signal $\overline{V_{c1}}$.

The 5-bit phase interpolator is shown in Fig.6(b). The delay difference between the interpolated signal and the ouput signal from *Input1* is,

$$\Delta t_{delay} = \Delta t_{12} \times \left(\frac{Vc5}{2} + \frac{Vc4}{2^2} + \frac{Vc3}{2^3} + \frac{Vc2}{2^4} + \frac{Vc3}{2^5}\right)$$

where Δt_{12} is the output delay difference of *Input1* and *Input2*. The phase interpolator also has the advantages that the input loading remains the same without any data-dependant loading and capacitive coupling between the input and the output are isolated by the

switch transistors. Besides, the g_m of input transistors remains the same and won't affect the switching performance.

VI. Experimental Results

The experimental results of DNL, and INL for the timing generator are shown in Fig.7. Data-dependent loading effects and the capacitive coupling between the input and the output are clearly eliminated and the DNL is less than ±0.3LSB without boundary step effects. The INL is less than ± 2LSB caused by the mismatch between the delay stages along the VCDL and the mismatch when the polarity of the MUX is inversed. The output signal is shown in Fig.8. The measured output jitter is 46ps (p-p) and 5.272ps (RMS) as shown in Fig.9. The chip micrograph is shown in Fig.10 and the whole chip area is $1.5 \times 1.5 mm^2$ fabricated in a CMOS 0.35 μ m 1P4M process.

VI. Conclusions

In this paper we realized a 100MHz CMOS timing generator for impulse radio system adopting common gate buffered switch techniques to prevent Data-dependant loading and capacitive coupling effects. The timing generator can achieve high resolution with good linearity and low jitter.

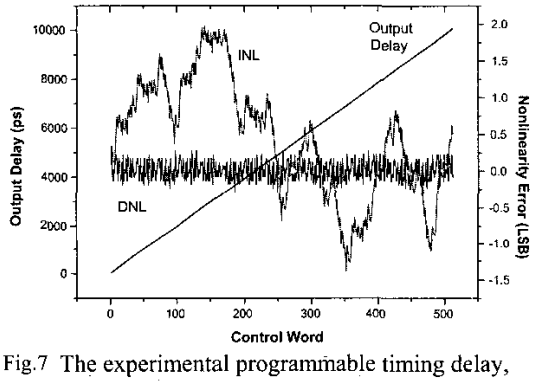
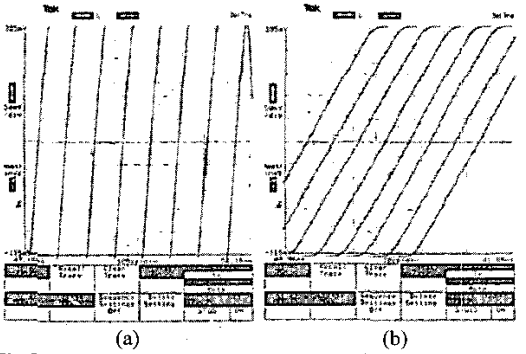


Fig.7 The experimental programmable timing delay, DNL, and INL of the timing generator



(a) (b)

Fig.8 The output signal of (a) 78ps resolution (b) 625ps resolution (19.5ps resolution is not shown due to the memory limit of the CSA 803A)

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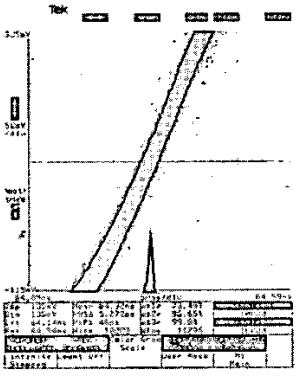

Fig.9 Jitter performance of the timing generator

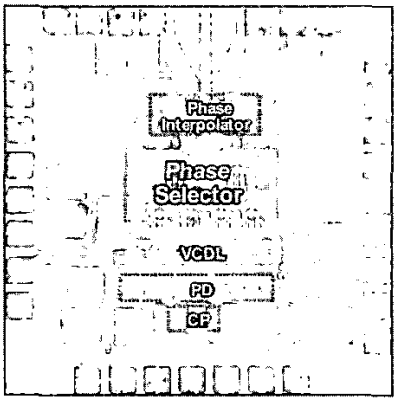

Fig.10 Micrograph of the chip

TABLE II
SUMMARY OF CHIP PERFORMANCE

Process	0.35μm CMOS 1P4M
Chip size	$1.5 \times 1.5 mm^2$
Timing resolution	20ps
DNL	±0.3 LSB(<±6ps@100MHz)
INL	±2 LSB(<±39ps@100MHz)
Jitter(p-p)	46ps
Jitter(RMS)	5.272ps
Operating frequency	45MHz~136MHz
Power consumption	55mW