Student paper

Annealing effects on the interfacial properties of GaN MOS prepared by photo-enhanced wet oxidation

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Abstract: We investigate the annealing effects on the interfacial properties of gallium oxide (Ga_2O_3) grown on gallium nitride (GaN) by the photo-enhanced wet oxidation technique. The depth profile resolved XPS analysis indicates an interfacial layer as thin as 20nm can be maintained at the Ga_2O_3/GaN interface when subject to a rapid thermal annealing in an oxygen ambient at 800°C. Our I-V and C-V analysis on the MOS device reveals a low interfacial density of state ~ 5×10^{10} $cm^{-2}eV^{-1}$ and high breakdown field above 3MV/cm. These results suggest the photo-grown Ga_2O_3 with post O_2 annealing is suitable for power device application.

Gallium nitride (GaN) has been regarded as an excellent material for power device application in the high frequency regime [1]. Unfortunately, the lack of high-quality gate insulator has limited the performance of GaN-based transistors. Capacitance analysis on a GaN metal-insulating-semiconductor (MIS) structure using conventional or novel gate dielectrics such as SiO_2 [2], Si_3N_3 [3], MgO [4], and $Ga_2O_3(Gd_2O_3)$ [5], only reveal an unsatisfactory minimum interfacial density of state (D_{it}) high above 10^{11} $cm^{-2}eV^{-1}$, except a recent work by jet-vapor deposition of Si_3N_3/SiO_2 stacks [6] on GaN showing a low D_{it} of ~ 5×10^{10} $cm^{-2}eV^{-1}$.

Here, we report the annealing effects on a Ga_2O_3/GaN MOS device structure that was prepared by the photo-enhanced wet oxidation technique [7]. The interfacial and electrical properties were characterized by the x-ray photo-emission spectroscopy (XPS), high frequency capacitance-voltage (C-V) and current-voltage (I-V) analysis, respectively. Our results indicate a low D_{it} on the order 5×10^{10} $cm^{-2}eV^{-1}$ and high breakdown field strength (E_{BD}) above 3MV/cm can be found with Ga_2O_3/GaN that undergoes a rapid thermal annealing (RTA) in an O_2 ambient at 800°C to transform the photo-grown Ga_2O_3 into a crystalline format.

The GaN film used in this study were epitaxially grown on sapphire substrates by metal-organic chemical vapor deposition and had an unintentional background doping about ~ 10^{17} cm^{-3}. The as-grown samples were first chemically cleaned and etched off a 50nm sacrificial GaN surface layer prior to initiate the photo-oxidation process. No external voltage was supplied to the oxidation apparatus in this study. Study of the annealing effects was conducted by placing the photo-oxide films in the following conditions of (1) 400°C annealing for one hour in a nitrogen (N_2) ambient gas, (2) with additional RTA at 800°C for 3 min, and (3) similar to (2) but in O_2 ambient gas. The Ga_2O_3/GaN MOS devices thus prepared were shown to have an oxide thickness of 180nm, 50nm, and 100nm, respectively. We confirm the formation of monoclinic β-Ga_2O_3 by x-ray diffraction analysis in samples undergone a RTA treatment at 800°C. The latter process will be shown in the following to play a crucial role in reducing the interfacial defect density, in particular subject to the O_2 ambient treatment, and to reduce the leakage current density and improve the forward breakdown field strength.

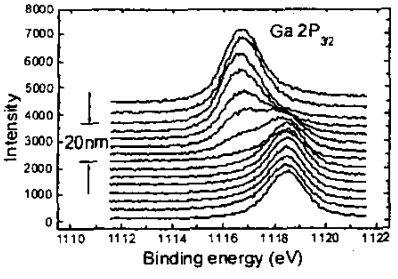

Fig.1 The depth profile of XPS measurements on an O_2-annealed Ga_2O_3/GaNsample

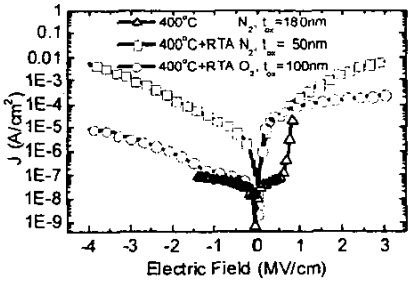

Fig.2 Dependence of leakage current density J on the applied electric field strength E, RTA at 800°C

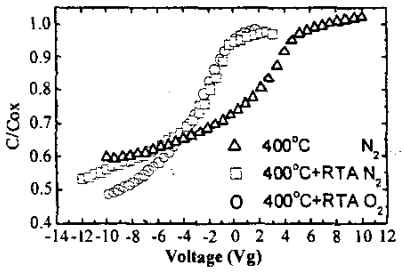

Fig.3 C-V characteristics measured at 1M Hz and room temperature

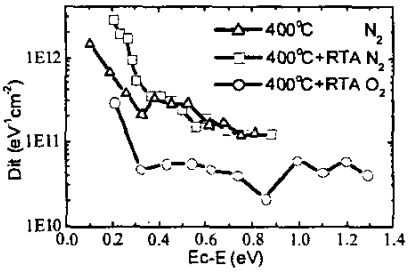

Fig.4 The interfacial density of state calculated by Terman's method.

First shown in Fig.1 is the depth profile resolved XPS data on the O_2 annealed sample. Note the characteristic shift of the gallium $2P_{3/2}$ binding energy from the Ga_2O_3 surface to GaN. Unlike a recent report of thermally oxidized Ga_2O_3 showing a diffusion-limited mechanism that can introduce an interfacial layer of Ga(ON) that is at least 100nm wide across the Ga_2O_3/GaN interface [8], our chemical sensitive data analysis of Fig. 1 reveals a sharp interface whose thickness is less than 20nm.

We illustrate in Fig.2 the measured leakage current density of MOS devices prepared by the above annealing process. Note an increase of forward breakdown field (E_{BD}) above 3 MV/cm can be maintained in samples subject to RTA treatment at 800°C, whereas for sample only received 400°C annealing, E_{BD} is only 0.65 MV/cm. Furthermore, we note sample under O_2 RTA treatment can have a leakage density at E_{BD} that is one order of magnitude smaller than that under N_2 RTA treatment. This indicates an optimum thermal treatment without degrading the interfacial and electrical properties of GaN can be achieved without suffering from the conventional high (1100°C) temperature process. [9]

Our data analysis in Table I further indicates Ga_2O_3/GaN MOS without high temperature treatment has the largest flat-band shift as shown in the CV measurement of Fig. 3 and highest interfacial density of state shown in Fig.4. However, a sharp slope can be seen in the depletion region of samples under RTA treatment at 800°C in Fig.3, and a dramatic decrease of D_{it} down to 5×10^{10} $cm^{-2}eV^{-1}$ and hysteresis width of 0.26V can be observed in MOS device prepared by O_2 annealing.

Table I: Flatband voltage, leakage density, fixed charge density, and interfacial density of state on the annealing conditions

Sample	V_{fb} (V)	Hysteresis width (V)	Leakage density	Nf (cm^{-2})	Dit ($cm^{-2}eV^{-1}$)
400°C N_2	3.39	3.02	Breakdown at 0.65 MV/cm	3.5×10^{11}	3×10^{11}
400°C + RTA:N_2	-0.97	0.64	100μA/cm^2 at 0.82 MV/cm	4.35×10^{10}	1.5×10^{11}
400°C + RTA:O_2	-1.42	0.26	100μA/cm^2 at 1.25 MV/cm	8.64×10^{10}	5×10^{10}

In summary, a low D_{it} on the order of 10^{10} $cm^{-2}eV^{-1}$ and high E_{BD} above 3 MV/cm can be resolved on Ga_2O_3/GaN MOS with O_2 annealing at 800°C. The improved electrical properties are ascribed to the annihilation of interfacial defects by post annealing and transformation into crystalline Ga_2O_3.

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