A Low Power Ka-Band SiGe HBT VCO Using Line Inductors

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Abstract — **An integrated low power, low phase noise Ka-band differential voltage-controlled oscillator (VCO) is developed in a 0.12-μm 200 GHz SiGe HBT technology. The use of line inductors instead of transmission lines is demonstrated to be feasible in LC-tuned resonators for Ka-band applications. The VCO operates on 1.6 V and dissipates 3.7 mW of power. A phase noise of -99 dBc/Hz at 1 MHz offset from the carrier frequency of 33 GHz is achieved, together with a VCO Figure-of-Merit of -183.7 dBc/Hz.**

Index Terms — SiGe, HBT, voltage-controlled oscillators, Ka-band, low power, line inductor.

I. Introduction

Integrated VCOs for Ka-band circuit applications have been historically developed using GaAs or other III-V technologies given that sufficient cutoff frequency (f_T) and maximum frequency of oscillation (f_{max}) around or beyond Ka-band are very difficult to achieve in silicon technology [1]-[6]. In addition, the lossy Si substrate also places serious constraints on the implementation of on-chip passive components such as inductors and transmission lines that are required for many Ka band circuit functions. With the rapid progress of SiGe HBT technology, however, fully Si-manufacturing-compatible SiGe HBTs with a peak f_T of over 200 GHz and a peak f_{max} of over 250 GHz are now commercially available [7], and the record peak f_T of SiGe HBTs has at present reached 350 GHz [8]. Such SiGe HBTs also offer extremely low 1/f broadband noise, making them ideally suited for low-phase noise oscillators. Thus, the intrinsic performance capability of Si-based technologies is no longer a bottleneck for Ka-band circuit applications, and there has been recent interest in developing SiGe VCOs [9]-[12].

The high f_T and f_{max} of SiGe HBTs not only make VCOs at Ka-band practical, but also facilitates a true power-aware design paradigm. SiGe HBT BiCMOS technology nicely enables the trend towards increased levels of integration, with more transistors and functionality effectively squeezed onto a single chip. Because SiGe technology are much more easily scaled than III-V technologies, the high f_T and f_{max} achieved with a 200 GHz SiGe technology at very small device geometries allows SiGe HBTs to deliver adequate gain and noise required for the Ka-band applications, even at very low current density. This inherent low power design advantage of SiGe technology can help relieve the serious power dissipation constraints faced at the package level and thereby extend the battery life of portable components.

The realization of high-quality on-chip passive elements, especially inductors and transmission lines, pose the major technical difficulty of using the SiGe technology for the applications beyond 10 GHz. On-chip inductors in Si were once thought to be impractical for the implementation of RFICs in the early 90's because of the lossy substrate and the thin metal interconnections which significantly degrade the quality factor of the inductors. Research into Q-enhancement of spiral inductors on Si has led to feasibility demonstrations of adequate on-chip inductors at to as high as 10 GHz. Passive elements for MMIC applications above 10 GHz are mostly made using microstrip or coplanar transmission lines techniques.

This paper presents a fully integrated, low power Ka-band SiGe HBT VCO using line inductors in its resonators and implemented in a state-of-the-art 0.12 μm 200 GHz SiGe HBT technology. A VCO Figure-of-Merit (FoM) of -183.7 dBc/Hz has been achieved, which is comparable to the best published results for both SiGe VCOs [9]-[17] and the Ka-band VCOs implemented in III-V technology [1]-[6].

II. SiGe HBT Technology

The SiGe HBT used in this VCO delivers an f_T higher than 40 GHz at extremely low current density and a peak f_T which exceeds 200 GHz. The SiGe HBT technology used in the present investigation employs a novel, reduced thermal cycle, "raised extrinsic base" structure, and

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utilizes conventional deep and shallow trench isolation, an *in-situ* doped polysilicon emitter, and an unconditionally stable, 25% peak Ge, C-doped, graded UHV/CVD epitaxial SiGe base. The device structure has been scaled laterally to 0.12-μm emitter stripe width in order to minimize base resistance and thus improve the frequency response and noise characteristics. Such a raised extrinsic base structure facilitates the elimination of any out-diffusion of the extrinsic base, thereby significantly lowering the collector-base junction capacitance. The SiGe HBT cross-section structure is shown in Fig. 1.

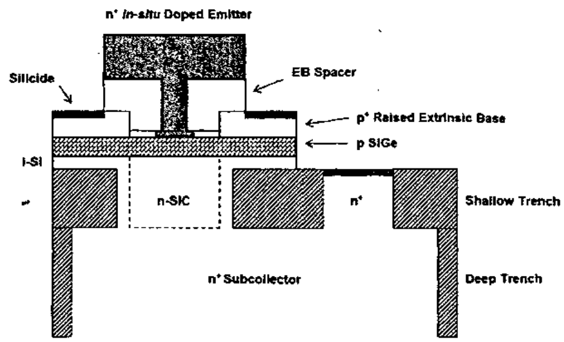

Fig. 1. A schematic SiGe HBT cross-section.

III. Line inductor development

Coplanar and microstrip lines are typically used to implement the inductive elements at Ka-band [1]-[6]. For this Ka-band VCO, however, line inductors instead are used to implement the resonators. The length of the line inductor is less than 1.5% of the transmission signal wavelength at Ka-band. Therefore, transmission line effects are not significant for the line inductors in this VCO. The line inductors are made of the top metal of the four interconnection metal layers in order to increase the distance away from the lossy substrate. This arrangement will mitigate the energy coupled into the substrate and reduce the parasitic capacitance between the inductor line and the substrate. The top metal is 4-μm thick *Al*, and is used to facilitate the development of low-loss interconnections, inductors, and transmission lines. In addition, the line inductors are implemented on top of the deep-trenched substrate to minimize the impact of the lossy Si substrate. The self-inductance of the line inductor can be calculated by the equation [18]-[19]

$$L = 0.02\ell\left[\ln(2\ell/GMD) - 1.25 + AMD/\ell + (\mu/4)T\right] \quad (1)$$

where *GMD* and *AMD* represent the geometric and arithmetic mean distances, respectively, of the line inductor cross section, μ is the conductor permeability, and T is the frequency-correction factor. From field simulations using a commercial EM solver, the line inductors are shown to work reasonably well at Ka-band.

IV. Differential VCO design

The capacitor feedback Colpitts architecture was used in the VCO core circuit in order to compensate the resistance of the resonators which consist of the line inductors, the parasitic capacitance of the inductors, and the varactors. Oscillation frequency tuning was achieved by changing the capacitance of the varactors. From the analysis of the single-ended Colpitts configuration, the negative resistance derived from the capacitor feedback is given by

$$R_c = \frac{-g_m C_1 C_2}{\omega^2 (C_1 C_2 + C_1 C_\pi + C_2 C_\pi)^2 + (g_m C_\pi)^2}. \quad (2)$$

For $C_\pi >> C_1$ and C_2, (2) can be simplified to

$$R_c = \frac{-g_m C_1 C_2}{\omega^2 (C_1 C_2)^2}. \quad (3)$$

The transconductance (g_m) of the SiGe HBT plays an important role in the generation of the negative resistance. The large the g_m, the larger the negative resistance. To maintain oscillation, the resistance of the resonator must satisfy the following equation:

$$R_r \le |R_c| \quad (4)$$

In addition to negative resistance, the Colpitts structure also results in capacitive reactance. The capacitive reactance compensates the inductive load of the resonator and sets the frequency of oscillation according to

$$f = \frac{1}{2\pi\sqrt{L\left(C_v + \frac{C_1 C_2}{C_1 + C_2}\right)}} \quad (5)$$

where C_v is the varactor capacitance. The cross-coupled transistor pair not only aligns the oscillation waveforms of the two resonators in 180-degree phase difference, but also functions as buffers to isolate the resonators from any external disturbance. To minimize the impact of the external loading, the differential outputs was further buffered by emitter followers. The schematic diagram of the integrated differential VCO is shown in Fig. 2.

The phase noise performance of the VCO at an offset f_m from the carrier frequency f_o can be described using Leeson's model

$$\Phi_n(f_m) = 10\log\left\{\frac{2FKT}{P_s}\cdot\left[1+\left(\frac{f_o}{2Q_L f_m}\right)^2\right]\cdot\left(1+\frac{\Delta f_{1/f^3}}{f_m}\right)\right\} \quad (6)$$

where F is the device excess noise, P_s is the average signal power, Q_L is the loaded quality factor of the resonator, and $\Delta f_{1/f}{}^3$ is the corner frequency between $1/f^3$ and $1/f^2$ regimes. It is widely accepted that the $1/f^3$ region is due to the up-conversion of the transistor low frequency noise. Since the SiGe HBT has extremely low $1/f$ noise corner frequency (in this case sub-kHz noise corner frequency), Leeson's model can be simplified for f_m larger than 100 kHz to:

$$\Phi_n(f_m) \cong 10\log\left\{\frac{2FKT}{P_s}\cdot\left[1+\left(\frac{f_o}{2Q_L f_m}\right)^2\right]\right\}. \quad (7)$$

The phase noise of the oscillator can be improved by minimizing the device excess noise, improving the Q of the resonator, and increasing the output power. The excess noise of the SiGe HBT with respect to the collector current usually presents a bathtub curve behavior. The inherent design tradeoffs center on: meeting the oscillation conditions, reducing the power consumption, and minimizing the phase noise.

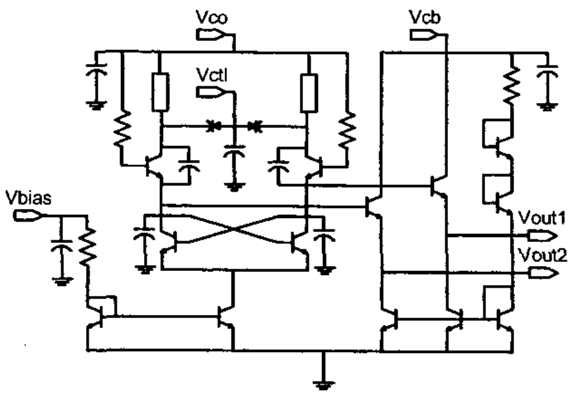

Fig. 2. Schematic diagram of the integrated SiGe VCO.

V. MEASURED RESULTS

The die size of the integrated SiGe HBT VCO is 650 x 730 μm^2, as shown in Fig. 3. The spectrum analyzer HP8565E with the phase noise measurement module HP85671A was used to measure the performance of the VCO. The VCO operates on supply voltage of 1.6V, and consumes 3.7 mW of power. The screen shot of the oscillation spectrum is shown in Fig. 4. The free-running frequency of the VCO is about 33 GHz, and the output power is -17 dBm without compensating the loss of the connection loss from the DUT to the spectrum analyzer. The measured SSB phase noise is -99 dBc/Hz at 1 MHz frequency offset.

In order to compare the performance of this work with those of other published VCOs, the VCO FOM is used to normalize the phase noise with respect to oscillation frequency, power consumption, and frequency offset according to

$$FOM = \Phi_n(f_m) - 20\log\frac{f_o}{f_m} + 10\log\frac{P_{diss}}{1mW} \quad (8)$$

where P_{diss} is the power dissipated by the VCO. This Ka-band SiGe HBT VCO achieves a FOM of -183.7 dBc/Hz, which is comparable to the best published results for VCOs realized in either SiGe or III-V technologies (see Table I).

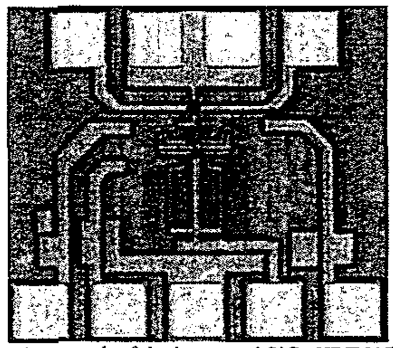

Fig. 3. Die photograph of the integrated SiGe HBT VCO.

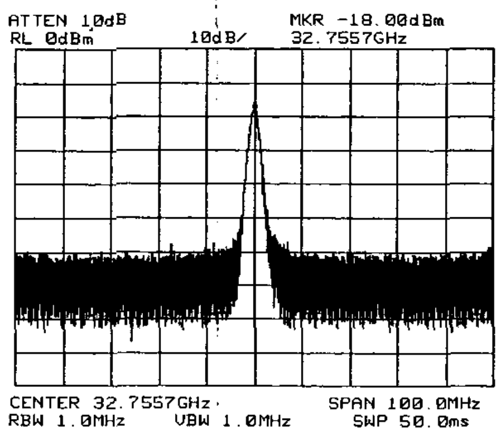

Fig. 4. Oscillation spectrum of the SiGe Ka-band VCO.

TABLE I
FIGURE-OF-MERIT COMPARISON OF PUBLISHED KA-BAND VCOS

Reference	[1]	[2]	[3]	[9]	[10]	[11]	[5]	This Work
Technology	InGaP/GaAs	GaAs HBT	InGaAs/InP	SiGe	SiGe	SiGe	AlGaAs/InGaAs	SiGe
Oscillation Freq.	41 GHz	41 GHz	34 GHz	41 GHz	40 GHz	28 GHz	42 GHz	33 GHz
Figure-of-Merit	-190.8	-182.6	-186.0	-155.1	-168.0	-152.3	-158.1	-183.7

VI. SUMMARY

A low power, fully integrated Ka-band VCO is implemented in the 200 GHz SiGe technology. Line inductors instead of transmission lines are demonstrated to be feasible for use in the resonators for Ka-band applications. The VCO oscillates at 33 GHz on a 1.6V supply voltage, consumes 3.7 mW, and yields a phase noise of -99 dBc/Hz at 1 MHz frequency offset. This SiGe VCO achieves a FOM of -183.7 dBc/Hz, which is comparable to the best published Ka-band VCOs in any semiconductor technology.

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