行政院國家科學委員會專題研究計畫 成果報告

超大型奈米積體電路無格線式全晶片繞線系統之研究(3/3)
研究成果報告(完整版)

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行政院國家科學委員會補助專題研究計畫成果報告

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※ **超大型奈米積體電路無格線式全晶片繞線系統 (3/3)** ※
※ ※
※ **Gridless Full-Chip Routing for Very-Large Scale Nanometer ICs** ※
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超大型奈米積體電路無格線式全晶片繞線系統（3/3）

Gridless Full-Chip Routing for Very-Large Scale Nanometer ICs

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一、中文摘要

隨著奈米技術的進步，在化學機械研磨之後的介電質厚度控制也變得對製造收斂有著關鍵的影響。為了增進化學機械研磨的品質，在繞線之後以 dummy feature 作填充是製造廠所使用的一種典型技術，然而，dummy feature 的填充卻可能大幅降低連線效能以及光罩資料的激增，也因此我們需要在繞線時考慮金屬線密度以減少 dummy feature 填充的負面效應。在這個計劃中，我們提出了一個可以考慮金屬線密度的全晶片繞線系統。為了考慮金屬線的分佈，我們採用二次式由上而下的繞線架構，並且使用了全新的金屬線密度分析技術與金屬層配置法。實驗結果顯示我們所提出的作法可以獲得比近年最新的研究獲得更平均的金屬線分佈。

關鍵詞：可製造性、化學機械研磨、繞線

二、英文摘要(Abstract)

As nanometer technology advances, the post-CMP dielectric thickness variation control becomes crucial for manufacturing closure. To improve CMP quality, dummy feature filling is typically performed by foundries after the routing stage. However, filling dummy features may greatly degrade the interconnect performance and lead to explosion of mask data. It is thus desirable to consider wire-density uniformity during routing to minimize the side effects from aggressive postlayout dummy filling. In this project, we present a new full-chip routing system considering wire density for reticle planarization enhancement. To fully consider wire distribution, the router applies a novel two-pass, top-down planarity-driven routing framework, which employs a new density critical area analysis based on Voronoi diagrams and incorporates an intermediate stage of density-driven layer/track assignment based on incremental Delaunay triangulation. Experimental results show that our methods can achieve more balanced wire distribution than state-of-the-art works.

Keywords: Manufacturability, chemical-mechanical polishing, routing

三、背景和目的

As IC process geometries shrink to 65nm and below, one important yield loss of interconnects comes from the chemical-mechanical polishing (CMP) step in the copper metallization (Damascene) process. Because of the difference in hardness between copper and dielectric materials, the CMP planarizing process might generate topography irregularities. A non-uniform feature density distribution on each layer causes CMP to over polish or under polish, generating metal dishing and dielectric erosion [22]. These thickness variation ns have to be carefully controlled, since the variation in one interconnect level is progressively transferred to subsequent levels during manufacturing, and finally the compounding variation can be significant on an upper level, which is often called the multi-layer accumulative effect [23].

Two key problems arise from the post-CMP thickness variation: (1) the layout surface fluctuates inside or outside the depth of focus (DOF) of the photolithography system, such that the exposed patterns do not appear acceptably sharp and open/short defects may even occur, and (2) these irregular variations greatly change the electrical characteristics of interconnects, especially for resistance and capacitance, degrading the accuracy of timing analysis and worsening the electromigration. As a result, in order to improve chip thickness uniformity, TSMC recommends performing virtual CMP (VCMP) analysis to identify the metal and dielectric thickness variation hotspot before chip fabrication for 65nm manufacturing processes (see TSMC Reference Flows 7.0) [24].

Recently, routing considering wire distribution has attracted much attention in the literature. The earlier studies for CMP processes have indicated that the post-CMP dielectric thickness is highly correlated to the layout pattern density, because during the polishing step, interlevel dielectric (ILD) removal rates are varied with the pattern density [23]. Further, the layout pattern (consisting of wires and dummy features) density can be systematically determined by the wire density distribution, as reported in [9]. Therefore, managing wire density at the routing stage has great potential for alleviating the aggressive dummy feature filling induced problems.

In this project, we present a new full-chip grid-based routing system, named TTR (Two-pass Top-down grid-based Router), considering wire-distribution uniformity for density variation minimization. To fully consider wire distribution, the router is based on a novel two-pass, top-down planarization-driven routing framework. Compared with the density-driven routing system [20], experimental results show that TTR can achieve 43% reduction on the maximum number of nets crossing in tiles and obtain at least 35% smaller standard deviations of wire distribution.

四、研究方法

4.1 Routing Model

We first explain the routing model. As illustrated in Fig. 1, G_k corresponds to the routing graph of level k. Each level contains a number of global cells (GCs), and the GCs belonging to different levels have different sizes. We denote GC_k as the GC of level k.

The first top-down routing pass is for global routing, which starts uncoarsening from the coarsest level to the finest level (level 0). At each level k, our global router finds routing paths for the local nets (those nets that entirely sit inside GC_k but not inside GC_{k-1}). After all the global routings of level k are performed, we divide one GC_k into four smaller GC_{k-1} and at the same time perform resource estimation for use at level k-1. Uncoarsening continues until

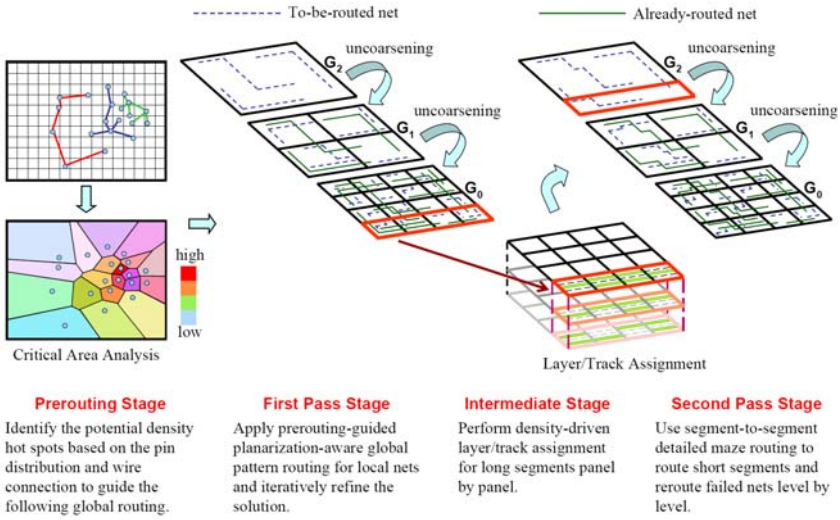

Fig. 1: The new two-pass, top-down routing framework.

the size of GC_k at a level is below a threshold.

The second top-down routing pass is for detailed routing. As the first pass, it processes uncoarsening from the coarsest level to the finest level. At each level, a detailed router is performed and rip-up/reroute procedures are applied for failed nets. The process continues until we reach level 0 when the final routing solution is obtained.

4.2 Density-Driven Routing

To deal with wire density optimization, we develop a Two-pass Top-down full-chip grid-based Routing system, named TTR (see Fig. 1). The rational for top-down routing lies in the fact that it tends to route longer nets first level by level, which directly contributes to better wire planning since longer nets have greater impacts on planarization than shorter ones. We detail the three distinguished stages of TTR in the following subsections.

4.2.1 Density Critical Area Analysis (CAA)

In order to guide the following routing for making better decisions, TTR features a density critical area analysis in the prerouting stage that identifies the potential over-dense hotspots. It is necessary to consider both topological information and wire connections of each pin to complement the density analysis. To remedy the deficiencies, we develop a new enhanced analysis model based on Voronoi diagrams. The Voronoi diagram of a point set P partitions the plane into regions, called Voronoi cells, each of which is associated with a point of P. If a point in the plane is closer to the point pt ∈ P than to any other point of P, then this point will be in the interior of the Voronoi cell associated with pt. The boundary segments of a Voronoi cell are called the Voronoi edges. A Voronoi diagram can efficiently compute the physical proximity and has been well studied in computational geometry [13]. Papadopoulou and Lee [21] used Voronoi diagrams of rectilinear polygons to compute the critical areas for short defects in a circuit layout.

Note that the Voronoi-diagram based CAA algorithm is performed only once, and its running time overhead is very small (about 3% of the total running time in our experiment). Further, it even leads to 3–5% faster overall routing process due to easier density control for later detailed routing, and it can substantially improve the resulting wire-density uniformity.

4.2.2 Planarization-Aware Global Routing

The global routing plans tile-to-tile routing paths for all nets and thereby is an important step to decide the wire distribution and maintain a uniform metal density across the chip. As mentioned in the introduction, both previous works [9], [20] consider only the wire density inside each global tile, which might incur larger inter-tile density gradient and thus more irregular post-CMP thickness. As a result, for better CMP control, a global router has to consider the density variation (gradient) among global tiles in addition to wire density inside each tile.

In our TTR, the global routing performed in the first top-down uncoarsening pass is based on pattern routing [17]. Pattern routing uses an L-shaped (1-bend) or Z-shaped (2-bend) route to make the connection, which gives the shortest path length between two points while reducing the routing bends. Therefore, the obtained routing path is the shortest, and we thus can focus on the objectives that we most concern.

We define the planarization-aware cost Φ_t for each global tile t as follows:

$$\Phi_t = \widetilde{d}_t + \begin{cases} \kappa_p, & \text{if } d_t \geq B_u \\ \beta(2^{d_t} - 1) + (1-\beta)(d_t - \overline{d_t})^2, & \text{if } B_l \leq d_t < B_u \\ \kappa_n, & \text{if } d_t < B_l \end{cases}$$

where d_t is the wire density of t, edt is the predicted hotspot cost calculated in the prerouting stage, d_t is the average wire density of tiles adjacent to t, B_l and B_u are density lower and upper bounds specified in foundry density rules respectively, and β, $0 \leq 1$, is a user-defined parameter. κ_p and κ_q are constants, where κ_p is a positive penalty that hinders the over denseness in the global tile, and κ_q is a negative reward that encourages paths to go through sparse tiles. The second equation simultaneously considers local density and minimizes the density difference among adjacent regions.

For more balanced wire distribution, the cost function Φ_p of the global routing path g_p is defined as follows:

$$\Phi_p = avg\{\Phi_t \mid \text{tile } t \text{ is on the path } g_p\},$$

in which the average manner can represent the consciousness of even wire distribution.

4.2.3 Density-Driven Layer Assignment

Recently, Cong et al. [11] proposed the first wire-planning scheme between global and detailed routers to reduce congestion. Batterywala et al. [2] also suggested to add a track assignment stage between global and detailed routing to improve the routing quality. Ho et al. [14] developed a layer/track assignment heuristic in the intermediate stage for crosstalk optimization. Later in [15], Ho et al. further extended their track assigner for the wirelength reduction in X-architecture routing. However, wire density is not addressed in these works.

In this project, we propose a new layer/track assignment algorithm for wire-density optimization. To our best knowledge, this is the first work of wire planning that addresses the wire-density optimization in the literature. We handle long horizontal (vertical) segments which span more than one complete global tile in a row (column) in the middle layer/track assignment stage and delegate short segments to the detailed router. The full row (or column) of a global tile array is called a row (column) panel. We will refer to a row panel as a panel throughout the paper for brevity, unless specified otherwise.

In a panel, the local density of a column is defined as the total number of segments and obstacles at that column, and the panel density is the maximum local density among all columns. For example, Fig. 2(a) gives a row panel with 11 columns, c_1 to c_{11}. There are six segments s_1 to s_6 in the panel and two obstacles o_1 and o_2 in layers, and its panel density is equal to 4. We intend to evenly arrange these segments to two horizontal layers (say layers 1 and 3) while minimizing the panel density at each layer. The density-driven layer assignment problem is defined as follows.

The Density-driven Layer Assignment (DLA) Problem: Given a set L of layers, a set S of disjoint segments in a panel, and a set O of fixed obstacles in layers, assign each segment of S to a layer, such that for each layer the local density is balanced, and the panel density is minimized.

To solve the DLA problem, we partition the segments and obstacles in each panel into |L| layer groups such that the main objective of DLA is achieved.

First, we build the horizontal constraint graph HCG(V,E) for S and O in the panel. Each vertex $v \in V$ corresponds to a segment or an obstacle, and two vertices v_i and v_j are connected by an edge $e \in E$ if their spans overlap. The cost of edge $e(v_i, v_j)$ is defined as the maximal local density among the overlapping columns between v_i and v_j . With this weighting policy, if two vertices are connected by an edge with a high cost, they should be separated into different layers. Fig. 2(b) shows the HCG of the panel in Fig. 2(a). Here, the obstacle o_2 and segment s_3 overlap in columns c_3 and c_4, and the maximal local density of c_3 and c_4 is 3. So the cost of the edge (o_2, s_3) equals 3.

Consequently, we can formulate the DLA problem as a max-cut, k-coloring problem (MCP) [10] on the HCG graph, where k equals |L|. In this way, we can guarantee that the partitioning result can evenly distribute the segments of the maximal local density to different layer groups. However, the MCP is NP-complete [10]. Thus, we resort to a simple, yet efficient heuristic by constructing a maximum spanning tree on the HCG and applying a k-coloring algorithm on this tree. Note that the k-coloring algorithm on a tree can be solved in linear time. Fig. 2(c) shows a layer-partitioning result of Fig. 2(a), where s_1, s_2, s_3 and s_6 are partitioned as one layer group, and o_2, s_4, s_5 and o_1 are partitioned as another one. Note that the objects o_1, s_3, s_5, and s_6 at columns c_9 and c_{10} that induce the maximum local density are separated into two different layer groups.

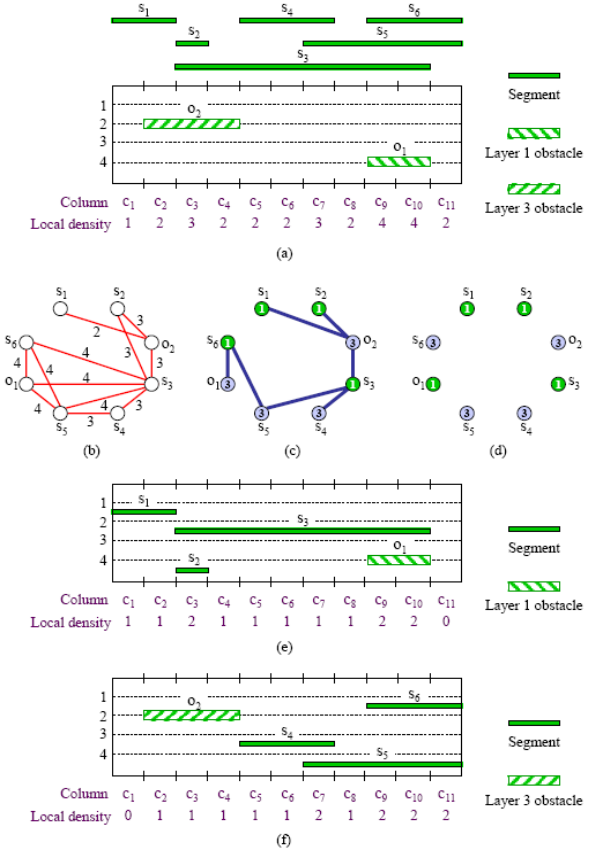

Fig. 2: A density-driven layer assignment example.

At the last step, since obstacles are already in fixed layers, we applied a minimum-impact repair procedure for obstacles. If an obstacle is not placed in the right layer (e.g., o_1 in Fig. 2(c)), the layer of a vertex v_o of an obstacle is exchanged with that of a vertex v_s of a segment such that the edge cost (v_o, v_s) is the maximum among the edges connected with v_o in the maximum spanning tree. If there does not exist such a vertex v_s, we can just assign v_o to the correct layer since there is no segment there (otherwise, there must be an edge connected with v_o). The final assignment result after the repair procedure for exchanging the layer of vertex o_1 with that of vertex s6 is shown in Fig. 2(d). As a result, the final assignment has a very balanced density distribution that the average local density of layer 1 is 1.18 and that of layer 3 is 1.27 while the panel densities in both layers equal 2. See Figs. 2 (e) and (f) for the resulting segment assignments for layers 1 and 3, respectively.

4.3 Experimental Results

The TTR routing system was implemented in the C++ programming language on a 1.2 GHz SUN Blade-2000 workstation with 8GB memory. We used the LEDA packages to compute the Voronoi diagrams and Delaunay triangulation. We conducted the experiments based on the 11 MCNC routing benchmarks [3] (these designs have 3–4 routing layers and contain up to 28K connections).

Table I shows the comparison results on the MCNC benchmarks. As shown in the tables, all routers obtain 100% routing completion on the MCNC benchmarks, and both routers applying the new framework of TTR outperform the multilevel router MROR in wire uniformity. Compared with

Table I: Comparison for the wire density control on the MCNC benchmarks.

Circuit	MROR [20]						Minimum pin density global routing [9] + TTR's routing framework								TTR (Ours)							
	$\#Net_{max}$	$\#Net_{avg\_v}$	$\#Net_{avg\_h}$	σ_v	σ_h	CPU (sec)	#LG	#Seg	$\#Net_{max}$	$\#Net_{avg\_v}$	$\#Net_{avg\_h}$	σ_v	σ_h	CPU (sec)	#LG	#Seg	$\#Net_{max}$	$\#Net_{avg\_v}$	$\#Net_{avg\_h}$	σ_v	σ_h	CPU (sec)
Mcc1	45	9.9	11.3	7.6	7.3	77.4	124	2600	41	10.3	11.1	5.1	7.6	36.1	124	2639	30	10.3	11.0	5.9	6.4	33.4
Mcc2	96	18.7	20.9	17.3	18.5	2714.9	256	15814	119	20.6	22.2	14.4	19.6	798.0	256	16644	87	20.5	22.2	13.9	16.0	645.0
Struct	7	1.4	1.4	1.1	1.6	61.4	193	2128	5	1.2	0.8	0.9	0.8	66.8	167	2124	6	1.1	0.8	1.1	1.0	58.2
Primary1	15	0.7	0.6	1.2	1.8	69.1	328	2423	12	0.8	0.7	0.9	1.4	27.0	215	2207	6	0.7	0.3	0.9	0.8	24.3
Primary2	25	2.1	1.9	1.6	4.5	322.2	387	8338	22	2.5	1.9	1.3	2.8	144.0	303	7693	8	1.8	0.9	1.3	1.6	131.0
S5378	15	4.4	3.5	3.4	2.1	4.5	87	1091	8	2.5	2.4	1.6	1.5	8.1	91	1193	9	2.5	2.4	1.8	1.5	8.2
S9234	14	4.0	2.6	3.2	1.6	3.2	95	912	7	1.7	1.6	1.4	1.3	5.2	95	1003	9	1.7	1.6	1.6	1.2	5.4
S13207	27	9.3	5.9	5.2	2.8	15.8	97	1727	13	3.4	3.0	2.1	1.8	24.8	97	1821	11	3.3	3.0	2.3	1.7	24.2
S15850	26	10.3	7.4	5.4	2.9	23.8	97	1834	12	4.0	3.8	2.3	1.9	34.2	97	1915	13	3.9	3.8	2.4	1.9	33.5
S38417	23	7.3	4.3	4.4	2.2	54.2	188	5043	10	3.0	2.4	1.8	1.4	62.5	188	5462	11	2.9	2.4	2.0	1.4	62.4
S38584	29	9.1	5.8	5.4	2.9	137.7	189	6004	16	3.3	3.1	2.3	1.6	112.0	189	6328	15	3.3	3.1	2.3	1.6	112.0
Comp.	1.00	1.00	1.00	1.00	1.00	1.00	-	-	0.68	0.72	0.74	0.59	0.65	1.01	-	-	0.57	0.66	0.64	0.64	0.65	0.98

MROR, TTR incorporated with the minimum-pin density global routing algorithm reduces $\#Net_{max}$, $\#Net_{avg\_v}$, and $\#Net_{avg\_h}$ by 32%, 28%, 26% respectively, and TTR with Voronoi-diagram-based CAA can achieve 43%, 34%, 36% reductions on $\#Net_{max}$, $\#Net_{avg\_v}$, and $\#Net_{avg\_h}$ respectively. Moreover, the routers using the TTR framework also result in at least 35% smaller standard deviations of wire distribu tion in both directions (which implies better density smoothness) than MROR.

五、成果 (Publications)

1. Z.-W. Jiang and Y.-W. Chang, "An optimal simultaneous diode/jumper insertion algorithm for antenna fixing," in Proc. of *IEEE/ACM International Conference on Computer-Aided Design* (*ICCAD-2006*), pp. 669--674, San Jose, Nov. 2006
2. C.-W. Lin, M.-C. Tsai, K.-Y. Lee, T.-C. Chen, T.-C. Wang, and Y.-W. Chang, "Recent research and emerging challenges in physical design for manufacturability/reliability," in Proc. of *ACM/IEEE Asia South Pacific Design Automation Conference* (*ASP-DAC-2007*), pp. 238--243, Yokohama, Japan, January 2007. (**invited paper**)
3. C.-W. Lin, S.-Y. Chen, C.-F. Li, Y.-W. Chang, and C.-L. Yang, ``Efficient obstacle-avoiding rectilinear Steiner tree construction," in Proc. of *ACM International Symposium on Physical Design* (*ISPD-2007*), pp. 127--134, Austin, TX, March 2007. (**Best Paper Nominee**)
4. B.-Y. Su, Y.-W. Chang, and J. Hu, ``An exact jumper insertion algorithm for antenna violation avoidance/fixing considering routing obstacles," in *IEEE Trans. Computer-Aided Design*, Vol. 26, No. 4, pp. 719--734, April 2007.
5. J.-W. Fang, C.-H. Hsu, and Y.-W. Chang, "An integer linear programming algorithm for flip-chip routing," to appear in Proc. of *ACM/IEEE Design Automation Conference* (*DAC-2007*), San Diego, CA, June 2007. (**Best Paper Nominee; received the highest score in the beyond-die track**)
6. T.-C. Chen and Y.-W. Chang, "Multilevel full-chip gridless routing with applications to optical proximity correction," in *IEEE Trans. Computer-Aided Design*, Vol. 26, No. 6, pp. 1041--1053, June 2007

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ACM International Symposium on Physical Design (ISPD-2007)

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一、參加會議經過

ACM International Symposium on Physical Design (ISPD) is sponsored by ACM and is a premier conference on VLSI physical design automation. It is a great honor for a researcher to have a chance to present her/his work at this conference. This year's event was held inAustin, Texas, U.S.A on March 18--21, 2007.

二、與會心得

This year we have two papers accepted by ISPD-2007, the most in the world. The first paper is entitled "X-architecture placement based on effective wire models" (joint work with my students T.-C. Chen and Y.-L. Chuang); this paper received the highest score in the review and was nominated for best paper. The abstract is as follows:

In this paper, we derive the X-half-perimeter wirelength (XHPWL) model for X-architecture placement and explore the effects of three different wire models on X-architecture placement, including the Manhattan-half-perimeter wirelength (MHPWL) model, the XHPWL model, and the X-Steiner wirelength (XStWL) model. For min-cut partitioning placement, we propose a generalized net-weighting method that can exactly model the wirelength after partitioning by the net weight. The net-weighting method is general and can be incorporated into any wire models such as the XHPWL and XStWL models. For analytical placement, we smooth the XHPWL function using log-sum-exp functions to facilitate analytical placement. Our study shows that both the XHPWL model and the XStWL model can reduce the X wirelength. In particular, our results reveal the effectiveness of the X architecture on wirelength reduction during placement and thus the importance of the study on the X-placement algorithms, which is different from the results given in the previous work that the X-architecture placement might not improve the X-routing wirelength over the Manhattan-architecture placement.

The 2nd paper is entitled “Efficient obstacle-avoiding rectilinear Steiner tree construction” (joint work with my students C.-W. Lin, S.-Y. Chen, C.-F. Li, and C.-W. Liu and Prof. C.-L. Yang). Its abstract is as follows:

Given a set of pins and a set of obstacles on a plane, an obstacle-avoiding rectilinear Steiner minimal tree (OARSMT) connects these pins, possibly through some additional points (called Steiner points), and avoids running through any obstacle to construct a tree with a minimal total wirelength. The OARSMT problem becomes more important than ever for modern nanometer IC designs which need to consider numerous routing obstacles incurred from power networks, prerouted nets, IP blocks, feature patterns for manufacturability improvement, antenna jumpers for reliability enhancement, etc. Consequently, the OARSMT problem has received dramatically increasing attention recently. Nevertheless, considering obstacles significantly increases the problem complexity, and thus most previous works suffer from either poor quality or expensive running time. Based on the obstacle-avoiding spanning graph (OASG), this work presents an efficient algorithm with some theoretical optimality guarantees for the OARSMT construction. Unlike previous heuristics, our algorithm guarantees to find an optimal OARSMT for any 2-pin net and many higher-pin nets. Extensive experiments show that our algorithm results in significantly shorter wirelengths than all state-of-the-art works.

In addition to ours, there were about 20 other papers presented at ISPD-2007. Based on those papers, the main research trends in VLSI Design Automation are physical design for manufacturability and methodologies for large-scale designs. Due to the advance in the nanometer IC technologies, devices ad wires are placed in very close proximity, and interconnect delay, instead of traditional gate delay, becomes a dominating factor in determining circuit performance. It is essential to simultaneously consider area, delay, power, noise, and manufacturability for the interconnect optimization in systems-on-a-chip design.

三、建議

I would like to suggest that NSC simplify the procedures for application for attending conferences abroad. Too much paper work or red-tape not only burdens the staff in NSC, but also affects the productivity and efficiency of a researcher. **In my opinion, for example, writing a report like this one is absolutely unnecessary. A red-tape like this will just hurt the competitiveness of our country and benefits to nobody. I wish the requirement for writing such a report could be abolished in the near future.**

四、攜回資料名稱及內容

1. Proceedings of the 2007 ACM International Symposium on Physical Design.
2. Call-for-papers for the 2008 ACM International Symposium on Physical Design.
3. Call-for-papers for the 2008 ACM/IEEE Design Automation and Test in Europe.