Microsystem Technologies 11 (2005) 444–451 © Springer-Verlag 2005
DOI 10.1007/s00542-004-0486-0

A circular micromirror array fabricated by a maskless post-CMOS process

Y.-C. Cheng, C.-L. Dai, C.-Y. Lee, P.-H. Chen, P.-Z. Chang

Abstract This work studies the fabrication of a circular micromirror array by the standard 0.35 μm SPFM (Single Polysilicon Four Metals) CMOS (complementary metal oxide semiconductor) process and a maskless post-process. The advantages of the post-process are its compatibility with conventional CMOS process and this method provides a way to designer to quickly construct micromachined structures using the standardized procedures. The mentioned circular micromirror array that contains 10 × 10 micromirror switches is integrated with a 1 × 8 de-multiplexer control circuit and a four-stage charge pump on a chip. The radius of each micromirror is about 25 ìm, and the gap from the bottom electrode to the top mirror plate is about 5 μm. The micromirror array is actuated using an electrostatic force. Simulated results show that the micromirror has a tilting angle of around 9° at a driving voltage of 30 V. The root-mean-square roughness and the average roughness of the mirror surface are measured at 15.31 nm and 12.58 nm respectively. In addition, the first and the second mode of natural frequency of the micromirror switch are around 492 KHz and 508 KHz, respectively.

Received: 19 April 2004 / Accepted: 17 June 2004

Y.-C. Cheng, P.-H. Chen
Department of Mechanical Engineering,
National Taiwan University,
106 Taipei, Taiwan, R.O.C

C.-L. Dai (✉)
Department of Mechanical Engineering,
National Chung Hsing University,
250, Kuo-Kuang Rd.,
402 Taichung, Taiwan, R.O.C
e-mail: cldai@dragon.nchu.edu.tw

C.-Y. Lee
Department of Mechanical Engineering,
Yuan Ze University,
320 Taoyuan, Taiwan, R.O.C

P.-Z. Chang
Institute of Applied Mechanics,
National Taiwan University,
106 Taipei, Taiwan, R.O.C

The authors would like to thank Song-Nan Chen, Yao-Tian Huang of the Institute of Applied Mechanics, National Taiwan University, Professors Lung-Jieh Yang, and Chien-Liu Chang for their valuable advice and assistance in experiment. In addition, we would, finally, like to thank the NSC Northern Region MEMS Research Center, the National Chip Implementation Center and the National Center for High-performance Computing for kindly making their complete research facilities available.

1 Introduction

MOEMS (micro-optical-electro-mechanical systems) are one of several promising technological methods for developing all-optical switching connection subsystems in telecom or data networks [1–7]. A micromachined mirror is well known to be an optical key component. The advantages of using an optical mirror include its low sensitivity to polarization, and its functionality in a broadband optical application. The development of MEMS-based mirrors for optical communication, including optical scanners [8], projection display systems [9], variable optical attenuators [10] and other specific applications has attracted much interest recently. Various circuit integrated actuators have been presented [11–12]. Prior work on micromirror optical switching has shown the feasibility of making surface or bulk micromachined micromirrors for steering light beam s or for use in optical interconnect applications, through silicon deep etching or using expensive SOI (silicon on insulator) wafers [13–14]. However, issues considered in the literature include high process complexity, high operation voltage or power consumption and incompatibility with currently used VLSI circuits. The standard CMOS process offers good opportunities for creating much smaller devices and more intelligent optical cross-connect devices with driving circuits on the same chip, based on a micromirror switch array, for optical telecommunication, steering light beams and communication applications.

This study investigates an integrated chip which contains a micromirror array, a 1 × 8 de-multiplexer and a four-stage charge pump control circuit. The standard 0.35 μm SPFM CMOS process and a maskless post-CMOS process are utilized to fabricate the integrated chip. The micromirror array includes 10 × 10 micromirror switches. The post-CMOS process involves two primary steps. The first step employs RIE to remove parts of the sacrificial layer, which is the silicon dioxide layer, without an etch mask. The second step utilizes buffer oxide etchant (BOE) solution to etch the silicon dioxide layer to release the suspended micromirror structures. The main advantages of the post-CMOS process are its compatibility with the CMOS process. Transistors with low threshold voltages with four-stage two-phase clocking scheme charge pump

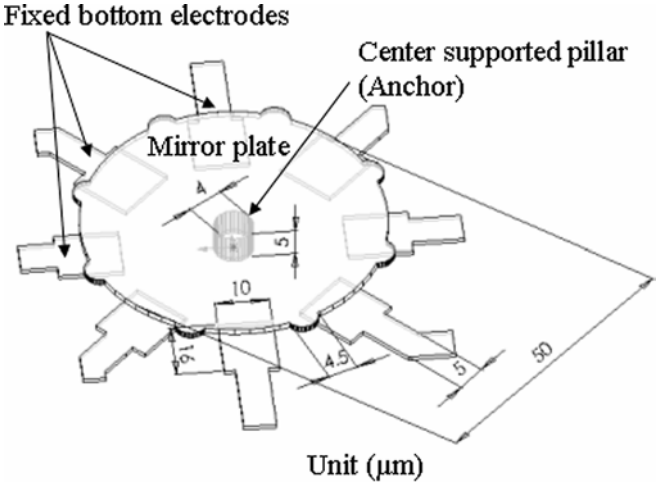

Fig. 1. Structure of a micromirror switch (not to scale)

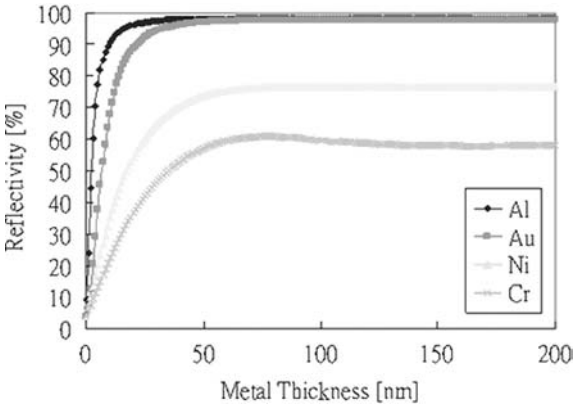

Fig. 3. Simulation of the reflectivity versus film thickness

circuit are used to increase the actuation voltage. Moreover, a 1 × 8 de-multiplexer is adapted to control the motion of the mirror plate to determine the direction of tilting. The micromirror is electrostatically actuated. Experimental results indicate that the micromirrors have a tilting angle of 9° at a driving voltage of 30 V. The first natural frequency simulated by a finite element method is around 492 KHz. The root-mean-square (RMS) and average surface roughness (Ra) of the mirror are measured at 15.31 nm and 12.58 nm, respectively.

2 Designing micromirror array

The integrated chip comprises a micromirror array, a 1 × 8 de-multiplexer and a four stage charge pump circuit. The chip is fabricated using the standard 0.35 μm SPFM CMOS process. The micromirror array and the circuits are outlined below.

2.1 Design of micromirror structures

A circular micromirror array consists of 10 × 10 micromirror switches. Figure 1 illustrates the structure and the dimensions of a micromirror. The figure contains a

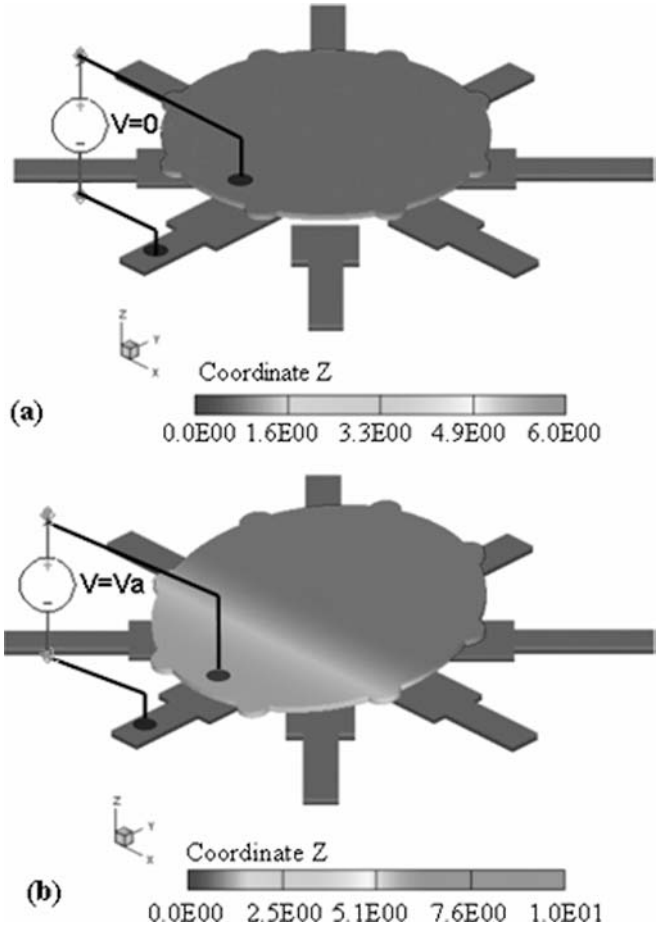

Fig. 2a, b. Motion of the micromirror, **a** not in the actuated state; **b** in the actuated state (Unit: μm)

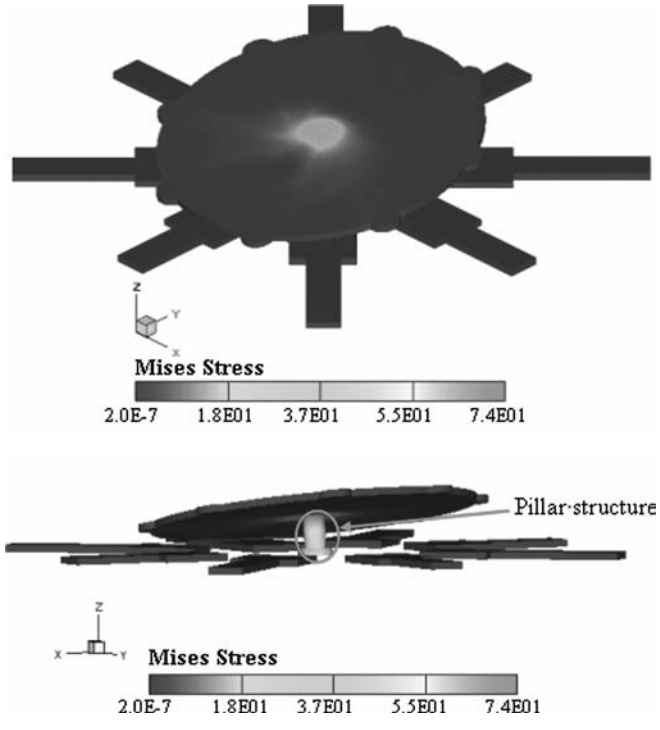

Fig. 4. Stress distributions in a micromirror structure (Unit : MPa)

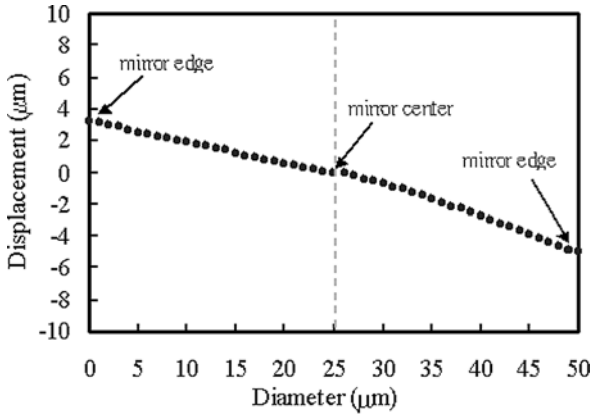

Fig. 5. Deformation curve of the micromirror plate in the actuated state

circular mirror plate with an aluminum layer with a thickness of about 1 μm, eight bottom-fixed electrode plates and a center-supported pillar structure. The mirror plate is a movable electrode plate, and has eight fixed electrode plates located below it. The fixed electrode plate and the mirror plate form a parallel-plate electrode. The gap between the fixed electrode plate and the mirror plate is about 5 μm. The micromirror switch includes eight sets of parallel-plate electrodes, formed from eight fixed-electrode plates and the mirror plate. The center-supported pillar structure is made of stacked aluminum layers and tungsten interlayers (vias). The bottom of the supported pillar is fixed to silicon substrate through the gate oxide layer by the contact layer, and the other end of this pillar is connected to the mirror plate. The radius and thickness of the mirror plate are 25 μm and 1 μm, respectively. The area of the all fixed-electrode plates is 16×10 μm^2. Moreover, the radius of each center-supported pillar is 2 μm. The circular mirror plate used in the standard CMOS process is made entirely from aluminum alloy. All mirror plates in the micromirror array are electrically connected to highly phosphorous-doped regions through pillars to yield micromirror switches with the same electrical potential.

In the unactuated state, or without applied voltage, as illustrated in Fig. 2(a), the mirror plate exhibits no action

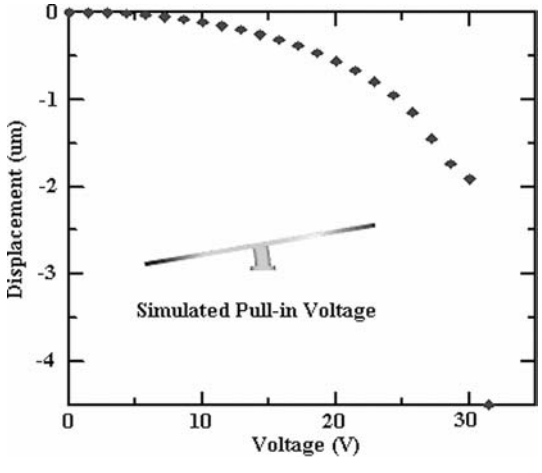

Fig. 6. Simulated displacements versus applied voltage

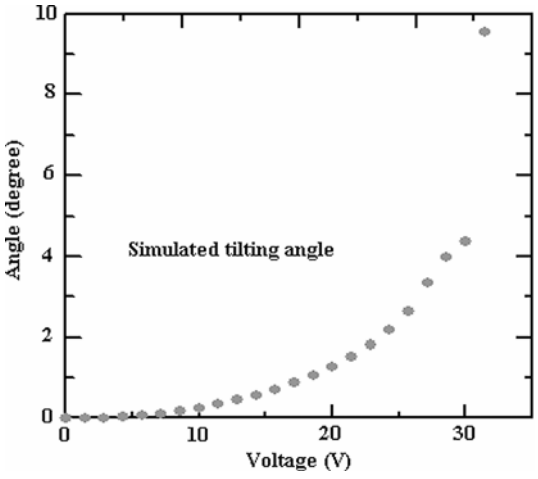

Fig. 7. Tilting angle versus applied voltage

in relation to the fixed electrode plate, accounting for the fact that the angle between the incident and reflective light beams is almost the same because aluminum is highly optically reflective (>90%) according to the simulated result by a commercial optical simulation tool-G-Solver, shown in Fig. 3. No other metal coating add-on process is required since the mirror plate is made by aluminum and the deposited oxide layer beneath the aluminum is polished by chemical-mechanical-polishing (CMP) in CMOS process. In the actuated state, a voltage of *Va*, as shown in Fig. 2(b), is applied to the fixed electrode plate and the mirror plate. The mirror plate is pulled down by the electrostatic force, which changing the direction of the incident light. The micromirror switch possesses eight operating modes, or directions, owing to the set-up of eight parallel-plate electrodes sets.

CoventorWare, professional MEMS development software is used to perform the dynamic analysis with coupled electrostatic (BEM), mechanical analysis (FEM) and stress distribution on the micromirror switch. Figure 4 illustrates the stress distribution of the micromirror plate in the actuated state. The maximum stress in the micromirror switch, 74 Mpa, is below the yield stress of aluminum, about 120 Mpa, and thus the deformation of the micromirror switch can be actuated in elastic range. Figure 5 reveals the deformation curve of the micromirror plate along radial direction in the actuated state. Figure 6 shows the simulated relation between the displacement and the applied voltage of proposed micromirror switch. The pull-

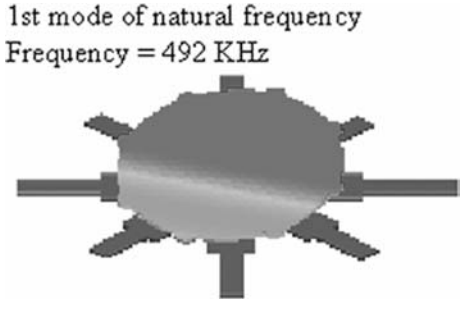

Fig. 8. First mode shape of the micromirror switch

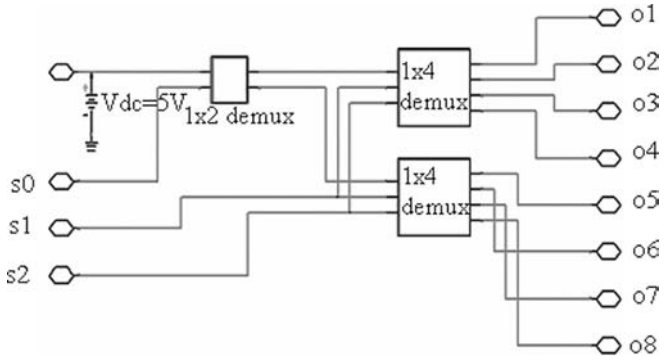

Fig. 9. 1 × 8 demultiplexer circuit

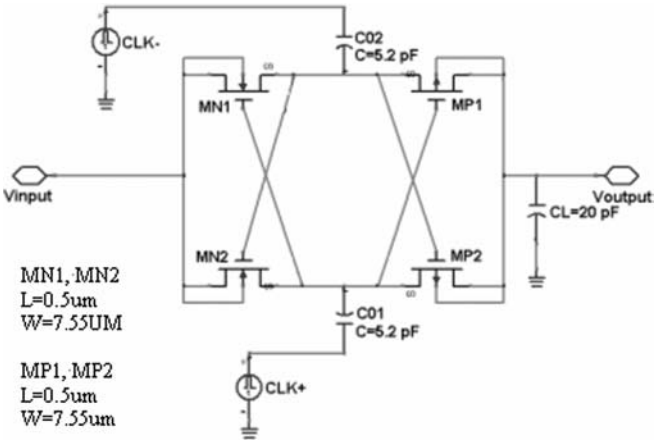

Fig. 11. Single stage charge pump circuit

in voltage is around 30 V. Figure 7 shows the relationship of the tilting angle versus applied voltage of the mirror plate. The maximum simulated angle of deflection of the micromirror is approximately 9° at a voltage of 30 V. Additionally, the first and second natural frequencies of the micromirror switch are 492 KHz and 508 KHz, respectively. Figure 8 shows the first mode shape of the micromirror switch.

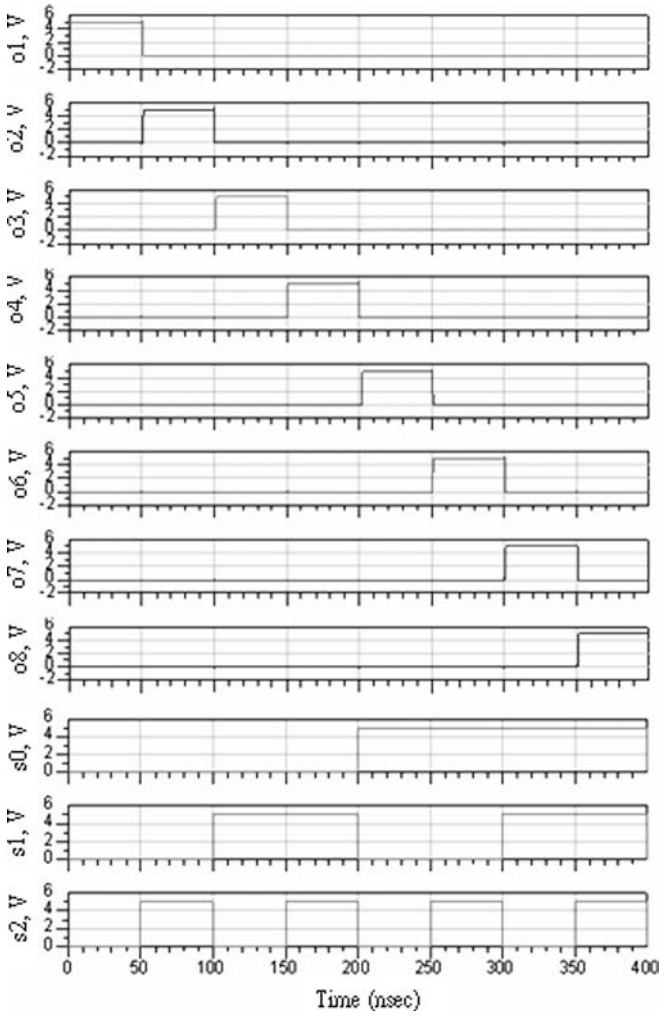

Fig. 10. Behavior of the micromirror switch when a 1 × 8 demultiplexer circuit is used

2.2
1 × 8 demultiplexer circuit

Figure 9 schematically depicts the 1 × 8 demultiplexer for the micromirror switch. Figure 10 displays the simulated relationship between the input and output voltage of the on-chip 1 × 8 demultiplexer circuit. The first eight signal curves correspond to the output ports (outputs 1, 2, 3, ~8), which are connected to the eight bottom-fixed electrode plates (bottom electrode pads 1, 2, 3, ~8) in the micromirror switch respectively. The last three signal curves represent the input signals. Eight operating modes of the mirror plate depend on the signal at the output ports. e.g., if the input signal is set to s0 = 0 (low), s1 = 1 (high) and s2 = 0 (low), then the output signal will be sent into the output port 3 (o3). A voltage can then be applied to the bottom-fixed electrode plate (pad 3) to pull down the mirror plate.

2.3
Charge pump circuit

The mosfet transistor fabricated by the standard 0.35 μm CMOS process cannot be operated at over 5 V. Care must be taken to ensure compatibility between the MEMS

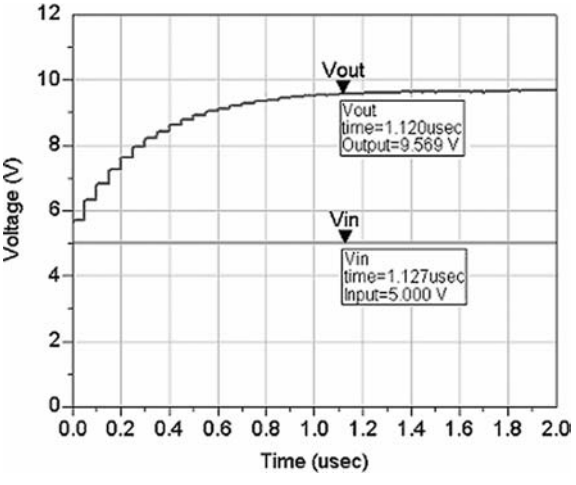

Fig. 12. Simulated signals obtained using the single-stage charge pump

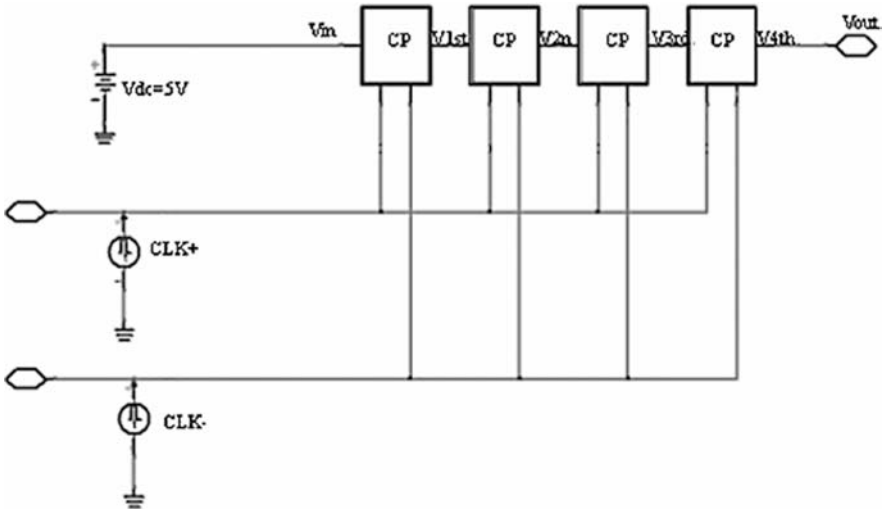

Fig. 13. Cascaded four-stage charge pump circuit

devices commonly operated at a higher voltage and the currently used low-voltage mosfet transistors. Figure 11 shows a single-stage two-phase charge pump circuit, compatible with low-voltage transistors [15]. The charge pump circuit is a cascade of voltage doubler stages, each of which can be realized with four low voltage transistors and a pair of capacitors. The circuit is operated using a two-phase clocking scheme, and no specific output stage is required. Following an initial transient state, the circuit enters a stationary state. During the first half-cycle of this clocking scheme, clk^+ equals Vdd, and clk^- equals zero, so that the transistors MN1 and MP2 are switched on, and MN2 and MP1 are cut off approximately simultaneously. Accordingly, the capacitor C2 is charged to V_{low}, and V_{high} is charged to the voltage stored on C2 plus Vdd. During the second half-cycle, clk^+ equals zero and clk^- equals Vdd; MN1 and MP1 are switched on; C2 is charged to V_{low}, and V_{high} is charged to V_{low} plus Vdd. Consequently, a voltage gain is obtained between V_{high} and V_{low}. Figure 12 shows the simulated results of the single-stage charge pump. The output voltage is approximately 9.5 V at 1.12 μ, as the input voltage remains constant at 5 V. The output voltage (9.5 V) is not sufficient for driving the micromirror switch. Consequently, a four-stage two-phase charge pump is used to augment the output voltage. Figure 13 shows the four-stage two-phase charge pump circuit, which has four single-stage two-phase charge pumps in series. Moreover, Fig. 14 displays the simulation results of the four-stage charge pump. The output voltage is around 24 V at 8 μ, for input of 5 V.

Each output port in the 1 × 8 demultiplexer is connected to a four-stage charge pump. The output voltage of the 1 × 8 demultiplexer can be increased to 24 V using the four-stage charge pump circuit.

3 Process

A foundry service TSMC (Taiwan Semiconductor Manufacture Company) with the 0.35 μm SPFM CMOS process performs the fabrication of a micromirror array chip. A post-CMOS process is used to release the suspended structures of the micromirror array following the CMOS process. The post-CMOS process involves two steps. Figure 15 indicates the flow of the post-CMOS process. Figure 15(a) illustrates cross-sections of the micromirror switch after completion of the CMOS process. The

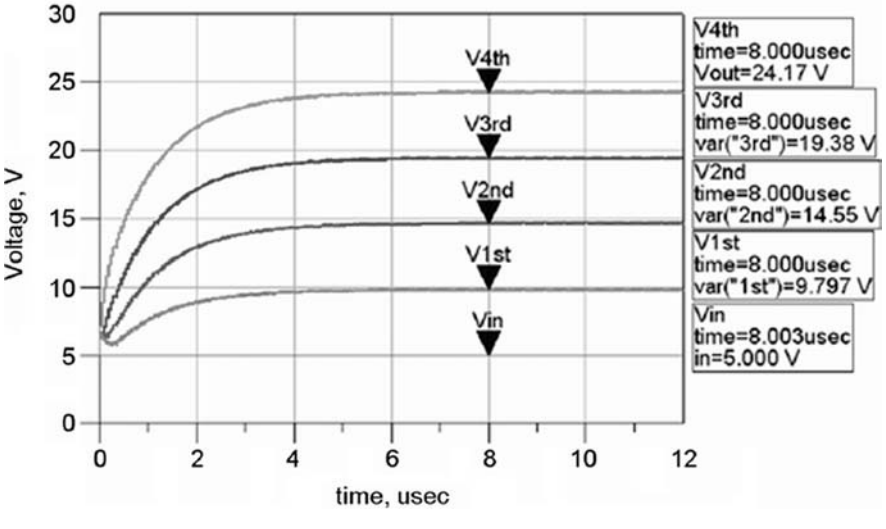

Fig. 14. Simulated signals obtained using four-stage charge pump circuit

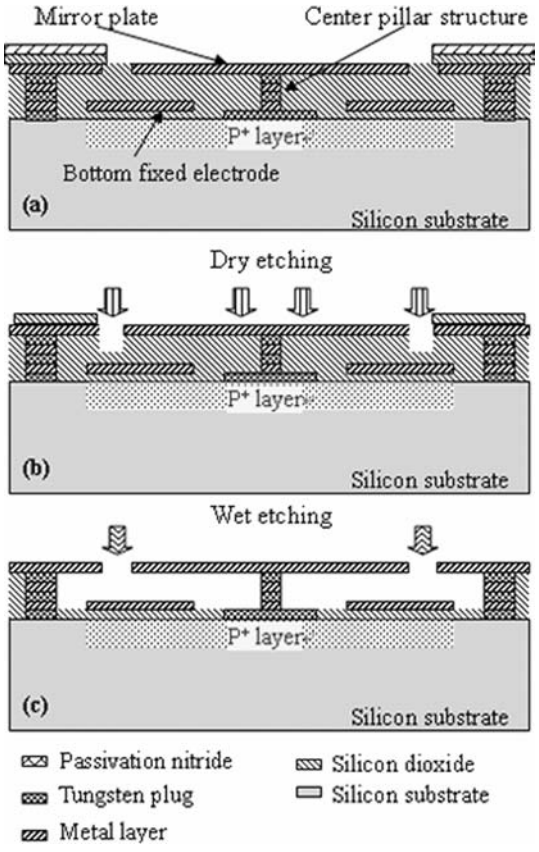

Fig. 15a–c. Flow of the post-process, **a** completion of the CMOS process; **b** etching silicon dioxide layer by RIE; **c** removing silicon dioxide layer by BOE

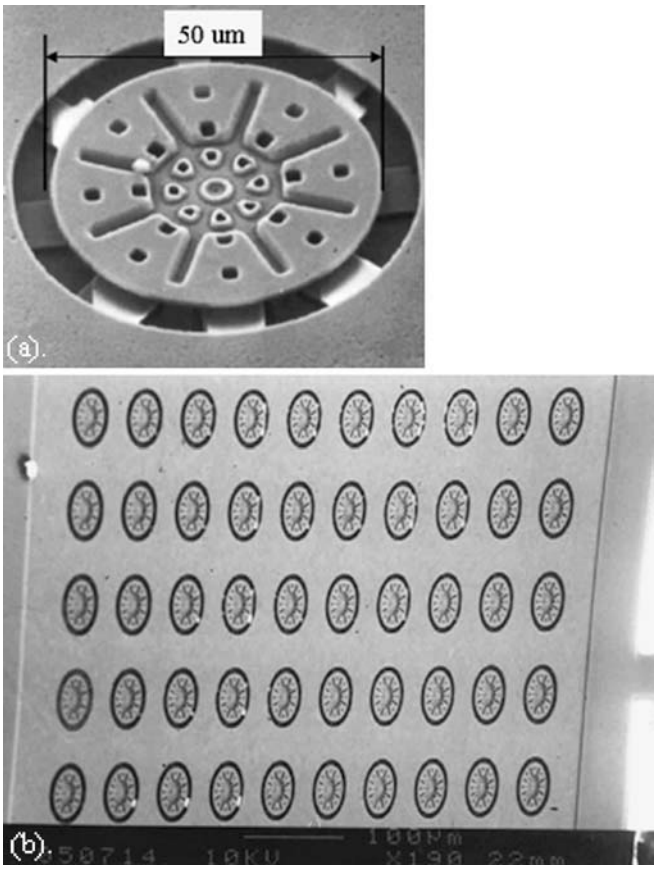

Fig. 16a, b. SEM picture of the released micromirror device; **a** a micromirror which violated the design rules; **b** mirror array of the device

passivation nitride on the surface of the chip was removed and the top metal layer was exposed. The silicon dioxide layers beneath the mirror plate were sacrificial layers. The mirror plate was released by removal of the sacrificial layers. Figure 15(b) illustrates that CF_4/O_2 RIE is used to etch the sacrificial layers. This step removes some of the silicon dioxide below the top metal layer and produces some cavities through the etching channels. The suspended structures of the micromirror switch are not all released. Consequently, isotropic wet etching of silicon dioxide must be performed to release the incomplete suspended parts, as shown in Fig. 15(c). This step was performed using BOE solution (6 parts 40% NH_4F and 1 part 49% HF). Critically, this post-process enhances the etching selectivity between Al alloy and silicon dioxide during wet etching. The suspended structures of the micromirror switch are released completely, and no sticking occurs following the overall post-CMOS processing. However, the etch time must be precisely controlled, to prevent short circuit by leaving a thin oxide layer to cover the fixed-electrode plates.

In the CMOS foundry service adopted here, the vias interlayer constitutes a tunnel in the oxide layer between the two metal layers. The use of this layer to connect each metal layer not only expands the electrode, but also acts as an anchor fixing the microstructures to the silicon substrate. The fixed electrodes in the micromirror array are covered with an insulating a thin oxide layer, which prevents a short circuit. The suspended micromirror is made of the top metal layer. Many etching channels around mirror plates are designed to reduce the etching time during the release of the suspended structures.

4
Results and discussion

This work fabricates a fully CMOS process compatible optical mirror switch. The surface quality of micromirror

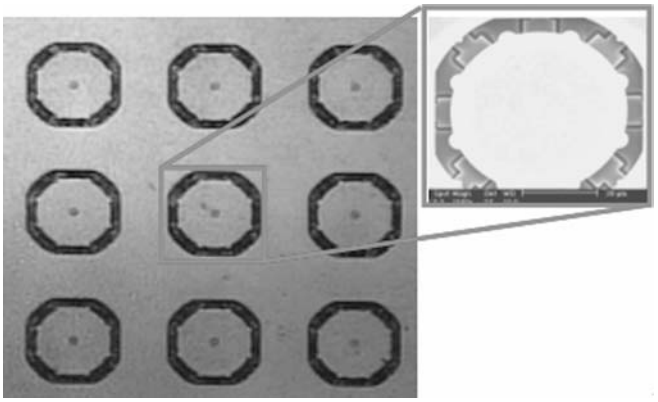

Fig. 17. SEM photograph of the micromirror switch following the post-process

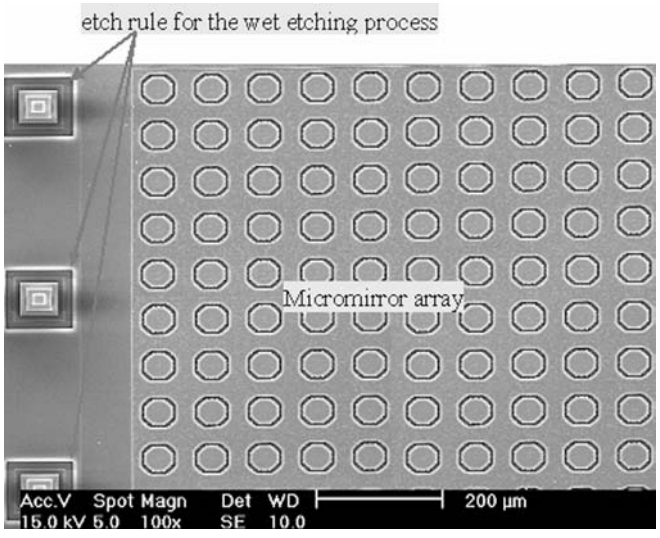

Fig. 18. SEM photograph of micromirror array following the post-process

plate and the experiment on actuation of micromirror switch are both discussed below.

4.1
Measurement of surface qualities of micromirror switch

The surface qualities of the micromirror are the most important determinants of the success of various optical applications that require micromirrors with a surface roughness better than one tenth of the wavelength and a large curvature radius, to ensure mirror flatness. In the previous design, owing to the violating of design rule which provided by IC foundry, several caved or grooves are located on the top mirror plate, and this design clearly is not suitable for the reflective type mirror. Figures 16(a) and 16(b) show the rugged surface quality of a mirror plate and a portion of mirror switch array of our previously design. Consequently, this study modified the flatness and surface quality of the CMOS micromirror further to improve the optical filling factor and reflection efficiency. Figure 17 shows the modified micromirror following the post-CMOS micromachining process. Figure 18 displays part of the modified micromirror array by SEM. Furthermore, Figure 19 shows the measurement results and the interferometric image of the modified micromirror. The measured data indicates that the CMOS compatible optical device can perform consistently with the requirements of commonly used reflecting type optical components. This investigation step determined the optical characteristics of the mirror surface roughness using an instrumental interferometer, the WYKO MHT III system–a non-contact, three-dimensional optical profiler. The root-mean-square (RMS) and average roughness (Ra) of the surface are measured at 15.31 nm and 12.58 nm, respectively. Additionally, the first and the second modes of the natural frequency of proposed mirror switch are around 492 KHz and 508 KHz, respectively. This information ensures the applicability of the CMOS micromirror switch against damage at the operation frequency within the range of kilohertz. These measurements reveal that the surface scattering and the natural frequencies are acceptable for optical applications and verify the compatibility between the standard CMOS process and the post-CMOS micromachining process.

4.2
Actuation of CMOS-MEMS micromirror switch

Figure 20 shows the sketch and photograph of a commercial LDV (laser-doppler vibrometer) system for used to measure the dynamic response of the micromirror array. The top metal plate and bottom-fixed electrode plate of the micromirror switch are connected to the negative grounded pad and the positive power pad, respectively, of the power supply system. The power supply system applies a voltage to the micromirror structures to generate an electrostatic driving force to deflect the micromirror. The experiment conducted here only revealed minimal motion by the variation of interference stripes of the optical inspection system throughout the experimental conditions. Figure 21 shows the switching time of the micromirror at an applying voltage 24 V_{pp} with 25 Hz square wave. The initial actuation of the micromirror has a transient state response before 15 ms. The rise time and fall time of the micromirror are 18.9 ms and 20.9 ms, respectively. However, the device may be destroyed owing to application of excessive voltage, and most of the mirror structures are burned down at about 45 V under a microscope.

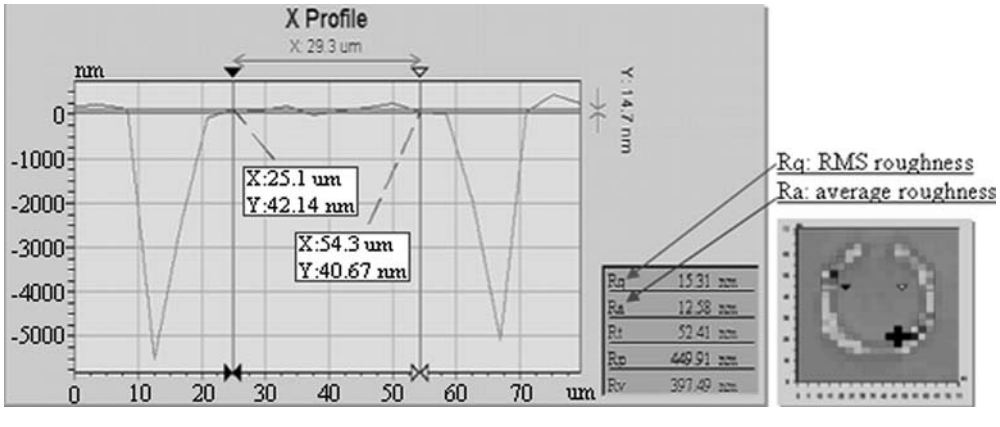

Fig. 19. Surface qualities of the mirror plate obtained using the WYKO interference measurement system

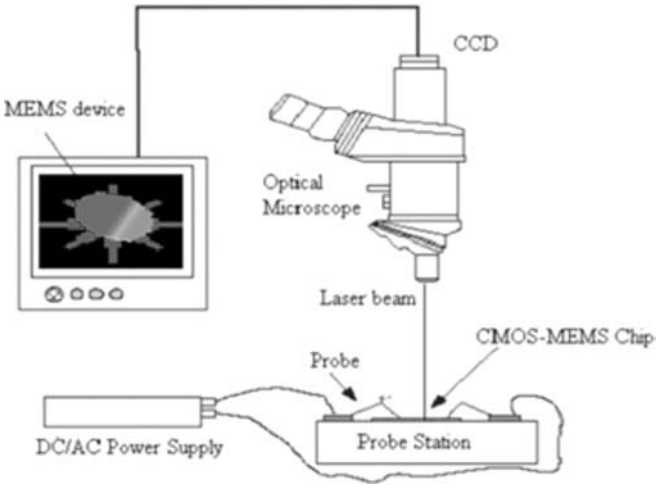

Fig. 20. Laser-Doppler vibrometer system for dynamic response inspection of the micromirror switch

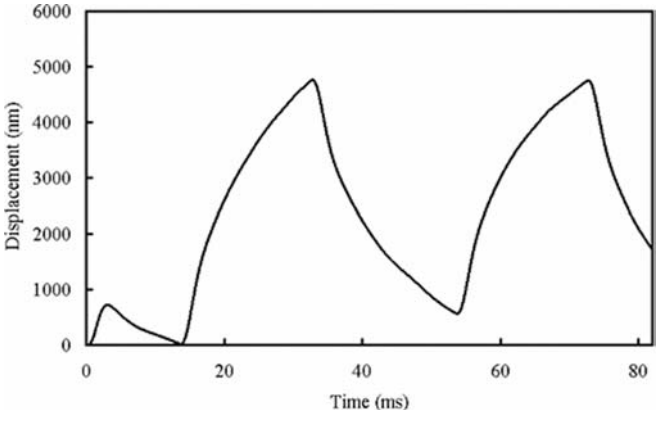

Fig. 21. The switching time of the micromirror measured by the LDV

5 Conclusion

A micromirror array integrated with circuits on a chip was implemented using the CMOS process. The post-CMOS micromachining process is completely compatible with the standard CMOS process. This study proposed the simulation and the experimental results of the circular micromirror array. The advantage of the micromachined optical device is that it can be mass-produced at low cost. Moreover, Experimental results indicate that the micromirrors have a tilting angle of 9° at a driving voltage of 30 V. The first natural frequency simulated by a finite element method is around 492 KHz. The root-mean-square (RMS) and average surface roughness (Ra) of the mirror are measured at 15.31 nm and 12.58 nm, respectively.

References

1. **Helin P; Mita M; Fujita H** (2000) Self-aligned mirror and V-grooves in freespace micromachined optical switches. Electron Lett 36: 563–564
2. **Shen G; Cheng TH; Bose SK; Chao Lu; Chai TY** (2002) Architectural design for multistage 2-D MEMS optical switches. J Lightwave Technol 20: 178–187
3. **Lin LY; Goldstein EL; Tkach RW** (1998) Free-space micromachined optical switches with submillisecond switching time for large-scale optical crossconnects. IEEE Photonics Technol Lett 10: 525–527
4. **Lin LY; Goldstein EL** (1999) MEMS for free-space optical switching. In: 12th IEEE Annual Meeting Lasers and Electro-Optics Society, pp 483–484
5. **Lin LY** (1999) Free-space micromachined optical-switching technologies and architectures. In: Optical Fiber Communication Conference and the International Conference on Integrated Optics and Optical Fiber Communication 2: 154–156
6. **Lee SS; Motamedi E; Wu MC** (1997) Surface-micromachined free-space fiber optic switches with integrated microactuators for optical fiber communication systems. In: Int Conf Solid State Sensors and Actuators, Chicago, USA. pp 85–88
7. **Lin LY; Goldstein EL; Tkach RW** (1999) Free-space micromachined optical switches for optical networking. IEEE J 5: 4–9
8. **Hah D; Choi CA; Jun CH; Kim YT** (2003) A self-aligned vertical comb-drive actuator using surface micromachining for scanning micromirrors. In: IEEE/LEOS Int Conf Optical MEMS, pp 151–152
9. **Hornbeck LJ** (1996) Digital Light Processing and MEMS: an overview advanced applications of lasers in materials processing. In: Summer topical meetings: Broadband Optical Networks/Smart Pixels/Optical MEMS and their applications, pp 7–8
10. **Kim CH; Park N; Kim YK** (2002) Reflective type variable optical attenuator using off-axis misalignment. In: IEEE/LEOS Int Conf Optical MEMS, pp 55–56
11. **Tuantranont A; Bright VM; Liew LA; Zhang W; Lee YC** (2000) Smart phase-only micromirror array fabricated by standard CMOS process. In: The 13th Annual Int Conf Micro Electro Mechanical Systems, pp 455–460
12. **Fischer M; Nagele M; Eichner D; Schollhorn C; Strobel R** (1995) Integration of Surface Micromachined Polysilicon Mirrors and a Standard Cmos Process. In: The 8th Int Conf Solid-State Sensors and Actuators, pp 305–307
13. **Houlet L; Helin P; Bourouina T; Reyne G; Diffour-Gergam E; Fujita H** (2002) Movable vertical mirror arrays for optical microswitch matrixes and their electromagnetic actuation. IEEE J 8: 58–63
14. **Toshiyoshi H; Fujita H** (1995) An Electrostatically Operated Torsion Mirror For Optical Switching Device. In: The 8th Int. Conf Solid-State Sensors and Actuators, pp 297–300
15. **Lauterbach C; Weber W; Romer D** (2000) Charge sharing concept and new clocking scheme for power efficiency and electromagnetic emission improvement of boosted charge pumps. IEEE J Solid-State Circuits 35: 719–723