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OPERATIONAL TRANSRESISTANCE AMPLIFIER USING CMOS TECHNOLOGY

J.-J. Chen, H.-W. Tsao and C.-C. Chen

Indexing term: Operational amplifiers

The Letter describes the design of a versatile analogue building block, termed an operational transresistance amplifier (OTRA). An operational transresistance amplifier has two low-input-impedance terminals and one low-output-impedance terminal. It is found to have a constant bandwidth independent of the gain in most closed-loop configurations. Simulation results are presented to demonstrate the constant-bandwidth performance. As an application example, this amplifier is used to implement a MOSFET-C differentiator, of which analysis and simulation results are also presented.

Introduction: As signal processing extends to higher frequencies, circuit designers are finding that traditional design methods based on voltage op-amps are no longer adequate. It is well known that a traditional operational amplifier has a bandwidth which is dependent on the closed-loop voltage gain. The attempt to overcome this problem has led to a renewed interest in circuits which operate in current mode [1]. A related device—the current-feedback op-amp—has recently become commercially available [2–4]. The circuits using this device employ current-processing techniques to improve dynamic speed capability, and a particular feature of these designs is their ability to provide a constant bandwidth virtually independent of gain. In this letter a two-port general-purpose analogue building block is described, termed an operational transresistance amplifier. It has similar transmission properties to the current-feedback op-amp, but with two low-impedance inputs and one low-impedance output. Simulation has been carried out to verify the constant-bandwidth performance. We also use this amplifier to implement a MOSFET-C differentiator, of which analysis and simulation results are also presented in this letter.

Operational transresistance amplifier and its applications: The operational transresistance amplifier (see Fig. 1*a*) can be described by the matrix

$$\begin{bmatrix} V_+ \\ V_- \\ V_0 \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ R_m & -R_m & 0 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_0 \end{bmatrix} \tag{1}$$

Obviously, both input terminals are virtually grounded, and the output voltage is the difference of the two input currents multiplied by transresistance R_m. We propose the circuit in Fig. 1*b* to construct this building block. If all current mirrors with bias current I_{bias} are simple current mirrors [5] implemented by CMOS transistors, and the channel length modulation factor λ and transconductance parameter β [5] of the PMOS transistors are equal to those of the NMOS transistors, then the transresistance R_m can be found as

$$R_m \simeq \frac{1}{2\lambda I_{bias}} \tag{2}$$

If all current mirrors are cascode current mirrors [5], R_m will be obtained as

$$R_m \simeq \frac{(0{\cdot}5\beta I_{bias})^{0{\cdot}5}}{(\lambda I_{bias})^2} \tag{3}$$

R_m is a large value, and can be considered as infinity in most applications. This amplifier, connected as a noninverting amplifier, is shown as Fig. 2. The voltage gain can be obtained as

$$\frac{V_0}{V_{in}} = \frac{R_m y_1}{1 + R_m y_2} \tag{4}$$

where $y_1 = 1/z_1$ and $y_2 = 1/z_2$.

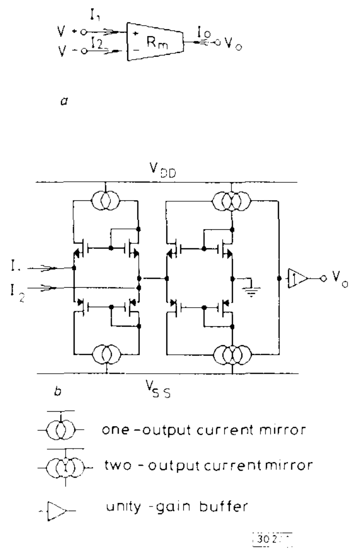

Fig. 1
a Symbol of an OTRA
b Actual circuit of an OTRA

If $R_m y_2$ is much greater than 1, the voltage gain approaches G, which is the ideal voltage gain and equal to z_2/z_1. If R_m can be represented by $N(s)/D(s)$, eqn. 3 can be derived as

$$\frac{V_0}{V_{in}} = G\,\frac{N(s)}{N(s) + z_2 D(s)} \tag{5}$$

If z_2 does not change, the poles and zeros of the voltage gain are always the same. So, the bandwidth of this circuit is a constant. An inverting amplifier is shown in Fig. 3 and its voltage gain can be obtained as

$$\frac{V_0}{V_{in}} = -\frac{R_m y_1}{1 + R_m y_2} \tag{6}$$

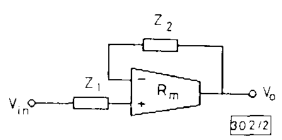

Fig. 2 *Noninverting amplifier*

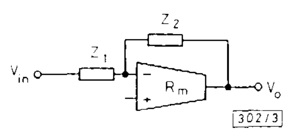

Fig. 3 *Inverting amplifier*

Its bandwidth is also nearly independent of the resulting voltage gain.

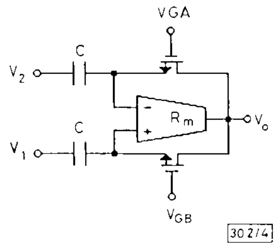

Fig. 4 *MOSFET-C differentiator*

Furthermore, we propose a MOSFET-C differentiator shown as Fig. 4 by using a single OTRA. The transfer function can be derived as the following by direct analysis:

$$\frac{V_0}{V_1 - V_2} = sC\left[\mu_n C_{ox} \frac{W}{L}(V_{GA} - V_{GB})\right]^{-1} \qquad (7)$$

where W and L are, respectively, the channel width and length of the two NMOS transistors in Fig. 4, μ_n is the carrier mobility and C_{ox} is the gate oxide capacitance. This circuit is an exact differentiator. The above circuits are simulated using PSPICE with $3{\cdot}5\,\mu m$ CMOS process parameters in the following Section.

Simulation results: To verify the constant-bandwidth performance the inverting amplifier shown in Fig. 3 is selected to

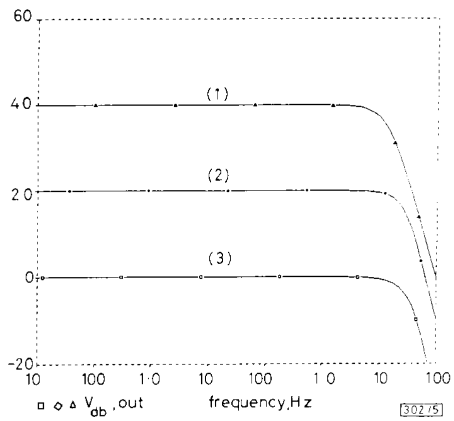

Fig. 5 *Simulation results of inverting amplifier of Fig. 3*

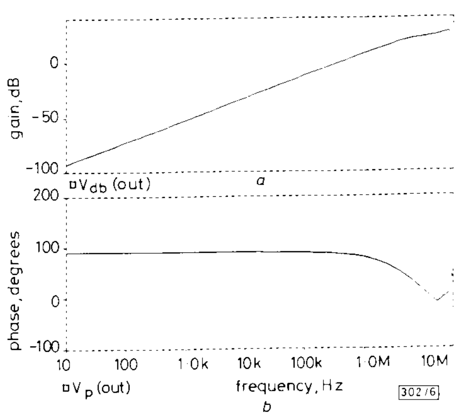

Fig. 6

a Gain amplitude simulation of Fig. 4
b Phase simulation of Fig. 4

be simulated. We choose a $100\,k\Omega$ resistor to be z_2, and let the resistance of z_1 be $1\,k\Omega$, $10\,k\Omega$ and $100\,k\Omega$. The simulation results are shown in Fig. 5, and the voltage gains of curves (1), (2) and (3) are 100, 10 and 1, respectively. Obviously, the bandwidths are nearly independent of the resulting gains. The simulation results of the MOSFET-C differentiator which confirmed the theoretical analysis are shown in Figs 6 and 7, which are results of frequency-domain and time-domain analysis with $V_{GA} = 1{\cdot}7\,V$, $V_{GB} = 1{\cdot}3\,V$ and $C = 1{\cdot}5\,pF$.

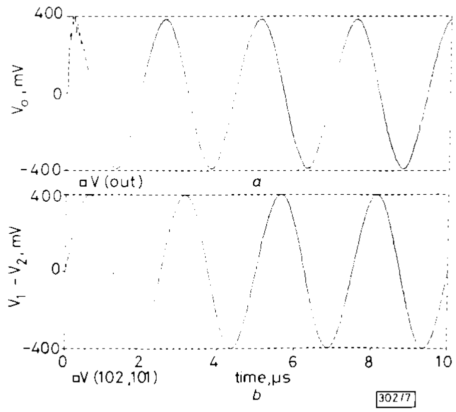

Fig. 7

a Output signal V_0 of Fig. 4
b Input signal V_1–V_2 of Fig. 4

Conclusion: A new operational transresistance amplifier is presented. The signal processing circuits derived from this amplifier usually have a constant bandwidth by using current-feedback configurations. These circuits are all cascadable, because of the low output impedance of an OTRA. Simulation results which confirm theoretical analysis have been obtained.

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J.-J. Chen, H.-W. Tsao and C.-C. Chen (*Department of Electrical Engineering, National Taiwan University, Taipei, Taiwan, 10764 ROC*)

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SINGLE-ARM SPIRAL SLOT ANTENNA FED BY A TRIPLATE TRANSMISSION LINE

H. Nakano, K. Nakayama, H. Mimaki, J. Yamauchi and K. Hirose

Indexing terms: Antennas, Slot antennas, Antenna arrays

A spiral slot antenna consisting of a single arm is etched into the upper plate of a triplate transmission line. Power on a feed strip line located between the upper and lower plates of the triplate is electromagnetically coupled to the spiral slot. The configuration of the spiral slot is optimised for radiation of a circularly polarised wave. An array antenna consisting of spiral slots, to which a pair-element technique is applied, shows wideband characteristics for the return loss and axial ratio.

Introduction: A dual-spiral slot antenna has the advantage that two radiation elements can be excited by a single feed line