CMOS 2.4-GHz Receiver Front End with Area-Efficient Inductors and Digitally Calibrated 90° Delay Network

Chih-Chun Tang, Chia-Hsin Wu, Kun-Hsien Li, Tai-Cheng Lee, and Shen-Iuan Liu

Electronic Circuits Lab., Department of Electrical Engineering and Graduate Institute of Electronics Engineering, National Taiwan University, Taipei, Taiwan.

ABSTRACT

A 2.4-GHz CMOS Hartley image-reject receiver utilizes the miniature 3D inductor and the digitally calibrated 90° delay network is proposed. Compared with the conventional planar inductor, the proposed miniature 3D inductor saves 80 % silicon area without degrading the quality factor. In addition, employing the digitally calibrated 90° delay network rather than the RC-CR network, which is used in the traditional Hartley receiver, can tune the delay dynamically such that insensitive to the temperature and process variations. A prototype chip with a fully integrated low-noise amplifier (LNA) followed by the proposed image-reject mixer was fabricated in a 0.35-μm single-poly-four-metal (1P4M) CMOS technology and the active area is 3.13mm^2. While operating in 2.4GHz, this receiver achieves 30 dB image-rejection ratio (IRR), -3 dB third-order input inter-modulation intercept point (IIP3), and 11 dB noise figure (NF) with 54 mW power consumption from a 3.3-V supply.

1. INTRODUCTION

Due to the tremendous demands of the portable wireless devices, providing the low cost solution is more and more important and emergent. For the non-zero IF receiver systems, the image signal may corrupt the desired signal. Several new techniques [1] and receiver architectures [2] have been proposed to suppress the image signal in the recently published papers.

In this work, Hartley receiver [3] is studied because of its simpler architecture and no second image problem. Two main non-idealities cause the incomplete image cancellation. One is the gain and phase imbalances due to the inaccurate quadrature LO signals and mismatched I/Q signal paths. Fortunately, these mismatches and imbalances can be minimized through the careful circuit placement and layout. However, the other factor, the inaccurate absolute values of R and C in the RC-CR network due to the temperature and process variations, cannot be well controlled by only using the simple circuit technique. Hence, developing an accurate shift-by-90° stage to replace the RC-CR network in Hartley image-reject receiver is our motivation.

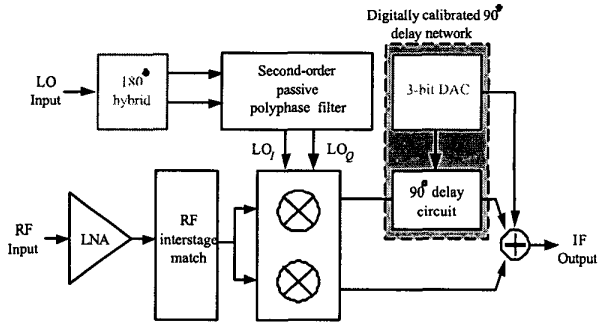

Fig. 1 Proposed image-reject receiver architecture with digitally calibrated 90-degree delay network.

2. ARCHITECTURE

Our proposed modified Hartley image-reject receiver architecture is shown in Fig. 1. RF input signal is amplified by a single-ended low-noise amplifier (LNA). Mixers are responsible for translating the amplified RF signal to the intermediate frequency (IF) band. The digitally calibrated 90° delay network, which consists of a 90° delay circuit and an off-chip 3-bit digital-to-analog converter (DAC), is used to replace the RC-CR network and to perform 90-degree signal delay. This proposed circuit allows the system to adjust the 90° delay network to compensate inaccurate delay results from the temperature and the process variations.

3. CIRCUITS DESIGN

Figure 2 is the schematic of the single-ended LNA. An on-chip LC matching network provides 50-Ω real input impedance. Compared to the conventional LNA, this LNA only occupies a small area because it utilizes the proposed miniature 3D inductors [4]. The conventional stacked inductor [5] consists of the series connected spiral

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inductors in the different metal layers. Every spiral inductor in the different metal layers may have the same or different turns. And the wires wind downward from the top metal layer to the bottom one. Our proposed miniature 3D inductor consists of at least two or above stacked inductors by series connections and every stacked inductor has only one turn in every metal layer. Figure 3 shows the structure of the proposed miniature 3D inductor. Compared with the planar inductor, the miniature 3D inductor saves 80 % die area without degrading the inductance and the quality factor, as shown in Fig. 4. In addition, the miniature 3D inductor also has the higher self-resonant frequency than the stacked inductor has, as shown in Fig. 5. This LNA was fabricated in a 0.35-μm 1P4M CMOS technology and its die size is 280 X 640 μm^2. Experimental results show the S11, S22, and S21 at 2.4-GHz are -14 dB, -13 dB, and 10 dB, respectively. The measured NF is 4.8 dB.

Two identical double-balance mixers are chosen to downconvert 2.4-GHz RF to 1.5-MHz IF in the quadrature phase. At the RF port, a series capacitor performs AC coupling and a shunt inductor acts as a RF choke to give the bias voltage. Quadrature LO signals are generated by passing the differential LO signals through an on-chip second-order passive polyphase filter. An off-chip 180° hybrid is used to generate the differential LO signals.

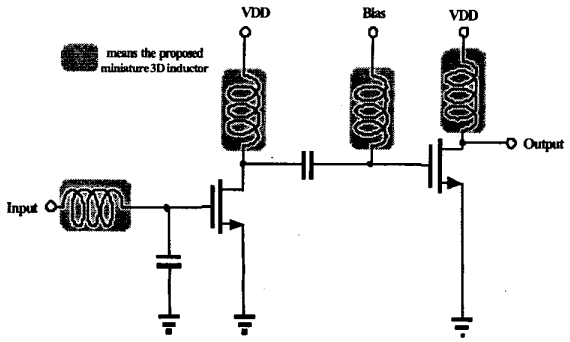

Fig. 2 Schematic of the single-ended double stage LNA.

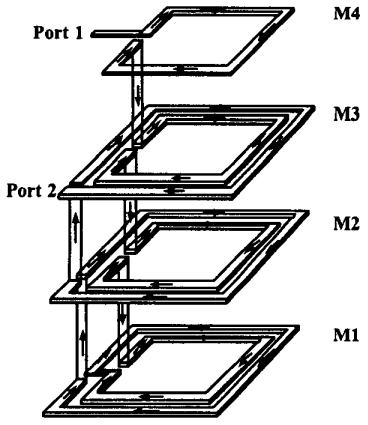

Fig. 3 Structure of the miniature 3D inductor.

90-degree delay circuit consists of two cascaded delay cells as shown in Fig. 6. Based on the conventional delay cell circuit [6], two additional MOS capacitors are added at the output terminals symmetrically to achieve the enough phase delay at 1.5-MHz. An off-chip control circuit, which includes the DAC, fine tunes the delay phase by adjusting the voltage of the terminal V_{bp}.

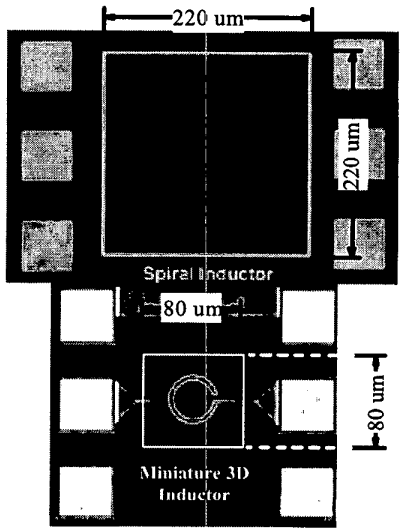

Fig. 4(a) Comparisons between the planar and the proposed miniature 3D inductor in the sizes

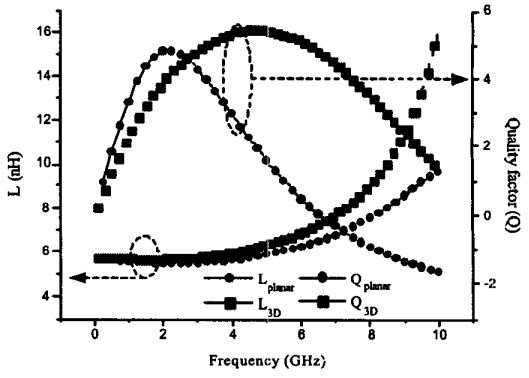

Fig. 4(b) Comparisons between the planar and the proposed miniature 3D inductor in inductance and quality factor.

After passing through the 90-degree delay circuit, the desired signals in I and Q channels are in phase but the image signals are out of phase. A combiner, shown in Fig. 7, adds the signals from I and Q channels together to cancel the image signal. MC1 and MC2 are added to control the bias current to adjust the amplitude balance and the control signal comes from the off-chip control circuit. Tuning the voltage of the control terminal, say *bbc1*, then the amplitude of the signal at *out+* can be adjusted and vice versa.

4. EXPERIMENTAL RESULTS

This proposed image-reject receiver was fabricated in a 0.35-μm 1P4M CMOS technology. Total active area is 3.13mm^2 without the test-keys and the die photo is shown in Fig. 8. The circuits have been tested in a chip-on-board assembly while operating under a 3.3-V power supply. Applying -40 dBm 2.4-GHz RF signal, -40 dBm 2.397-GHz RF image signal and -10 dBm 2.3985-GHz LO signal, the signal gain at 1.5-MHz IF is 0 dB and the image rejection ratio is 30 dB without any off-chip preselect filter. Measured gain is low because no amplifiers compensate the loss of the delay cells and the combiner. In spite of gain, this circuit indeed performs the image-rejection function. The measured IIP3 is -3 dBm and the total NF is 11 dB with 54 mW power consumption. At last, this receiver can correctly downconvert a 2.4-GHz GFSK signal to 1.5-MHz IF band. The GFSK signal emulates a Bluetooth RF signal with the modulation index 0.35, 200-kHz frequency deviation, and 1-MHz symbol rate. Figure 9 shows the GFSK spectrum at IF frequency. Table 1 summarizes the characteristics of this 2.4-GHz receiver.

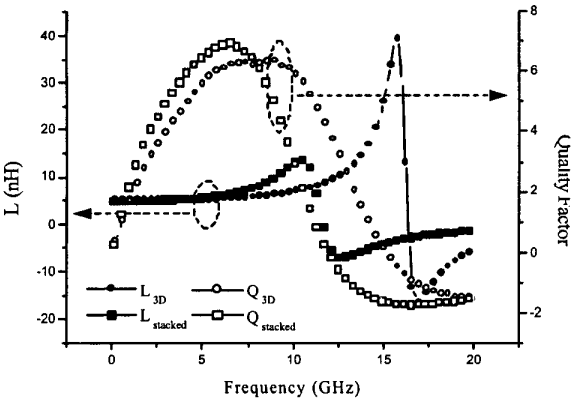

Fig. 5 Miniature 3D inductor improves 33 % self-resonant frequency of the stacked inductor in the same inductance.

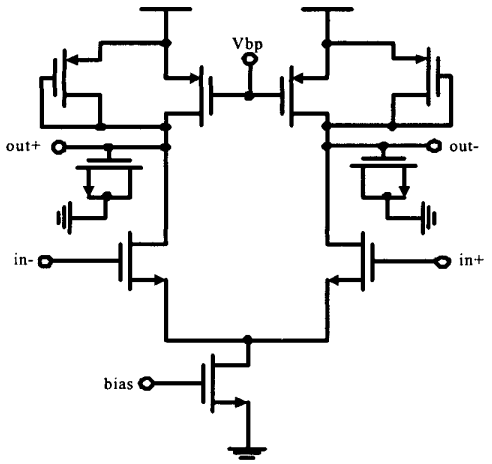

Fig. 6 Schematic of the delay cell.

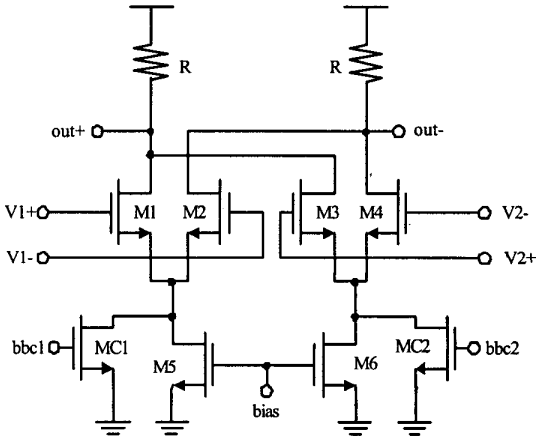

Fig. 7 Schematic of the combiner.

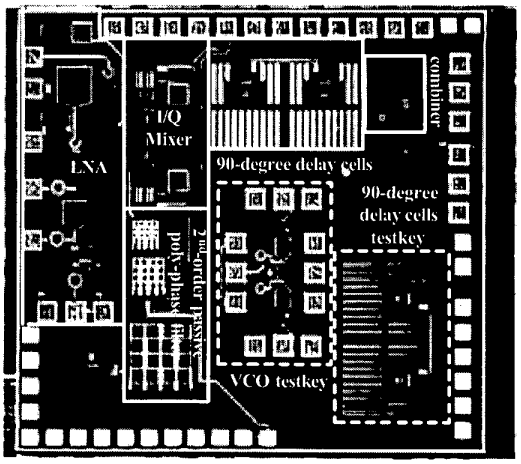

Fig. 8 Die photo of the test chip.

5. CONCLUSIONS

In this paper, an image-reject receiver is proposed. Inaccurate delay results from the temperature and process variations can be mitigated through the digitally calibrated 90° delay network. In addition, the chip also adopts the proposed miniature 3D inductor to save the silicon area significantly. According to the experimental results, this receiver can meet the in-band image rejection specification of Bluetooth.

6. REFERENCES

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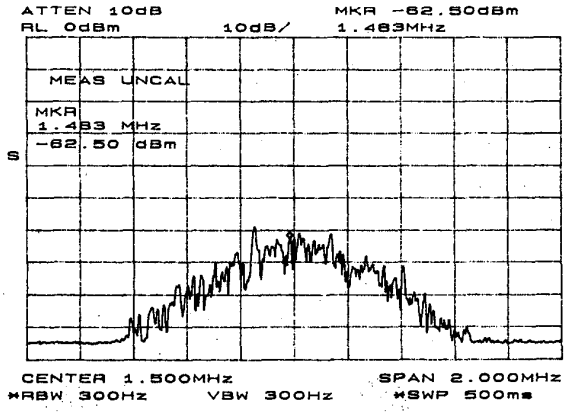

Fig. 9 GFSK output spectrum at IF .

Table 1 Performances summary of the test chip.

	Value
RF	2.4-GHz
LO	-10 dBm@2.3985-GHz
IF	1.5-MHz
IF Gain	0 dB
IIP3	-3 dBm
IRR	30 dB
NF	11 dB
Power Consumption	54 mW @ 3.3-V
Process	TSMC 0.35-μm 1P4M CMOS
Area	3.13 mm^2