Growth of strained Si on high-quality relaxed $Si_{1-x}Ge_x$ with an intermediate $Si_{1-y}C_y$ layer

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An intermediate $Si_{1-y}C_y$ layer in the $Si_{1-x}Ge_x$ film, replacing the conventionally graded buffer layer, was used to form the high-quality relaxed SiGe substrate. With the 700 nm thick $Si_{0.8}Ge_{0.2}$ overlayer, such a $Si_{1-x}Ge_x/Si_{1-y}C_y/Si_{1-x}Ge_x$ ($x=0.2$, $y-0.014$) heterostructure has a threading dislocation density of 5.5×10^5 cm^{-2} and a residual strain of only 2%. The surface roughness was measured to be about 4.2 nm. The long-range misfit dislocation array was formed mainly at the interface of top $Si_{1-x}Ge_x$ and $Si_{1-y}C_y$. Strained-Si *n*-channel metal-oxide-semiconductor transistors with various buffer layers were fabricated and examined. Effective electron mobility for the strained-Si device with this substrate technology was found to be 95% higher than that of Si control device. The scheme for the formation of the relaxed $Si_{1-x}Ge_x$ film serving as a virtual substrate shall be applicable to high-speed strained-Si devices. © *2005 American Vacuum Society.*
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I. INTRODUCTION

The use of tensile-strained Si has attracted considerable attention for high-speed transistors because of the enhanced in-plane carrier mobility as compared to bulk Si.[1–3] In order to introduce tensile strain into Si, relaxed $Si_{1-x}Ge_x$ epilayers grown on Si substrates are required to serve as "virtual substrates." The conventional method for obtaining relaxed $Si_{1-x}Ge_x$ epilayers with low threading dislocation densities is to grow thick compositionally graded buffer layers, in which mismatch strain is gradually relaxed by a modified Frank–Reed (MFR) mechanism.[4] However, such a graded buffer structure has many disadvantages, including long deposition time, surface roughness, and partial strain relaxation, for its practical applications.[5] Therefore, a thin buffer layer that relaxes the strain and reduces the defects in epilayers effectively is much desired for sub-100-nm complementary metal oxide silicon. To achieve this objective, several methods, such as those using a low-temperature Si, ion-implanted Si or compliant substrates, have been employed.[6–8] In this work, we demonstrate a simple method to grow high-quality relaxed $Si_{1-x}Ge_x$ films with the use of a $Si_{1-x}Ge_x/Si_{1-y}C_y/Si_{1-x}Ge_x$ ($x=0.2$, $y=0.014$) multilayer structure, where dislocation formation is favored or confined at the interface of top $Si_{1-x}Ge_x$ and $Si_{1-y}C_y$. Strained-Si *n*-channel metal-oxide-semiconductor field-effect transistors (*n*-MOSFETs) using this substrate technology were fabricated and their electrical characteristics were examined.

II. EXPERIMENTAL PROCEDURES

Four-inch diameter, 10–25 Ω cm, *p*-type (001)-oriented Si wafers were used as starting substrates. All structures investigated in this work were grown at 600 °C in a commercially available ultrahigh vacuum chemical vapor deposition (UHV/CVD) system. Pure SiH_4, $SiCH_6$, and 5% GeH_4 diluted in He were used as precursors. Before epitaxial growth, the Si wafers were dipped in a 10% HF solution to achieve the H passivation. A 60 nm thick Si buffer layer was first grown to cover the wafer surface. An 800 nm thick $Si_{0.8}Ge_{0.2}$ film with and without a 50 nm thick intermediate $Si_{0.986}C_{0.014}$ layer was then grown on the Si buffer. The intermediate $Si_{0.986}C_{0.014}$ layer was sandwiched between 100 and 700 nm thick $Si_{0.8}Ge_{0.2}$ underlayer and overlayer, respectively. Finally, a 20 nm thick strained Si cap layer was deposited. For comparison, the similar multilayer structures with a 200 nm thick $Si_{0.8}Ge_{0.2}$ overlayer, and the 800 nm thick $Si_{0.8}Ge_{0.2}$ films grown on a 2 μm thick compositionally graded buffer layer were also prepared. The surface morphology was characterized using Normaski microscopy and atomic force microscopy (AFM). The microstructures were investigated by cross-sectional transmission electron microscopy (XTEM), and the threading dislocation density of SiGe films was determined by Schimmel etch pit method.[9] The degree of strain relaxation and the Ge composition were determined by Raman scattering and high-resolution x-ray rocking curves. After epitaxial growth, strained-Si long-channel (gate length $L_g=100$ μm) *n*-MOSFETs with various $Si_{0.8}Ge_{0.2}$ substrates were fabricated by a standard MOS process, modified slightly for reduced temperature exposure. Control devices were also fabricated on bulk Si substrates. All devices have a channel doping (boron) of 3×10^{16} atoms/cm^3.

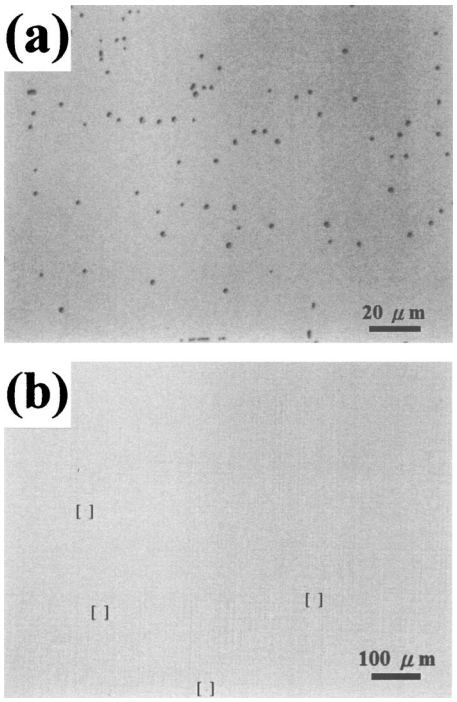

FIG. 1. Normaski images of the samples (a) without and (b) with an intermediate $Si_{0.986}C_{0.014}$ layer. The shallow pits are marked by the brackets.

III. RESULTS AND DISCUSSION

Figure 1 shows the Normaski images of the 800 nm thick $Si_{0.8}Ge_{0.2}$ films with and without an intermediate $Si_{0.986}C_{0.014}$ layer. The numerous shallow pits were found to form on the surface of the samples without an intermediate $Si_{1-y}C_y$ layer in order to relax the enormous mismatch strain accumulated during the growth, as shown in Fig. 1(a).[10] These shallow pits have the mean size of several microns and the density as high as 7×10^5 cm^{-2}. For applications requiring photolithography processes, such an epilayer could be problematic. On the other hand, in samples with an intermediate $Si_{1-y}C_y$ layer, almost pit-free surface was observed as shown in Fig. 1(b). This observation implies that the $Si_{0.986}C_{0.014}$ layer in the $Si_{0.8}Ge_{0.2}$ film indeed changes the strain relaxation mechanism during the growth. As a result, it is not necessary to induce pits to reduce the strain energy and maintain a smooth surface. The result is similar to that of a previous study using the relaxed $Si_{1-x}Ge_x/Si/Si_{1-x}Ge_x$ structures.[11] Figure 2 shows the AFM image of a sample with an intermediate $Si_{1-y}C_y$ layer. It is evident that sample displays the clear crosshatch pattern along ⟨110⟩ directions with uniform surface undulation. The rms roughness was measured to be about 4.2 nm, which is smaller than that of the sample with step-graded buffer layer measured in the present study (~6.4 nm). In the samples with step-graded buffer layer, strain is expected to be relaxed by the MFR mechanism giving rise to a large undulation of crosshatch pattern due to the pile-ups of dislocations.[12]

Figure 3(a) shows an XTEM image of the $Si_{0.8}Ge_{0.2}$ film with an intermediate $Si_{0.986}C_{0.014}$ layer. It was found that most of the threading dislocations were prevented from

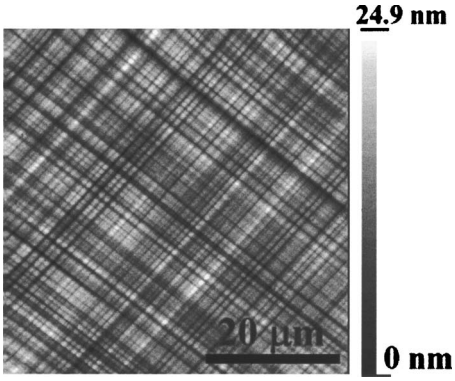

FIG. 2. AFM image showing the surface morphology of 800 nm thick $Si_{0.8}Ge_{0.2}$ film with an intermediate $Si_{0.986}C_{0.014}$ layer.

propagating into the top $Si_{1-x}Ge_x$ layer and remain trapped near the intermediate $Si_{1-y}C_y$ layer. However, the characteristic feature of the MFR mechanism, that is, pile-ups of dislocations several microns deep into Si substrate, is completely absent in the observed images. This indicates the MFR mechanism no longer played an important role during the strain relief in this $Si_{1-x}Ge_x/Si_{1-y}C_y/Si_{1-x}Ge_x$ heterostructure. By Schimmel etch method, the threading dislocation density was measured to be about 5.5×10^5 cm^{-2}.

Figure 3(b) shows the magnified view of a selected region near the $Si_{0.986}C_{0.014}$ layer. The long-range misfit dislocation array was found to form at the interface of top $Si_{1-x}Ge_x$ and $Si_{1-y}C_y$, maintaining a defect-free top SiGe layer. Compared with a previous study using the $Si_{1-x}Ge_x/Si/Si_{1-x}Ge_x$ structures, in which the strain was mainly relaxed by the formation of {113} dislocation loops in the Si layer, the introduction of a $Si_{1-y}C_y$ layer into the $Si_{1-x}Ge_x$ layer apparently

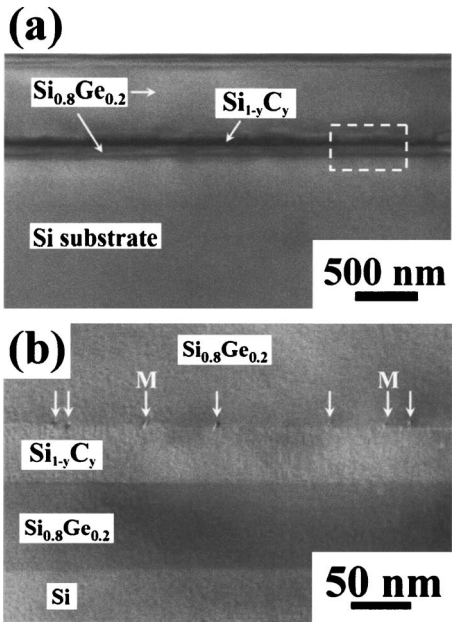

FIG. 3. XTEM images of (a) the 800 nm thick SiGe epilayer with an intermediate $Si_{0.986}C_{0.014}$ layer, (b) magnified view of a selected region of the $Si_{1-y}C_y$ layer, where M indicates the misfit dislocation array.

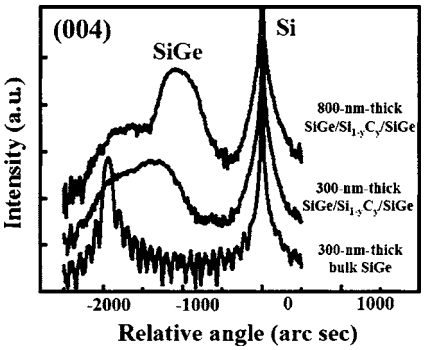

FIG. 4. X-ray (004) rocking curves of the samples with $Si_{1-x}Ge_x$ and $Si_{1-x}Ge_x/Si_{1-y}C_y/Si_{1-x}Ge_x$ (x=0.2, y=0.014) structures of different thickness.

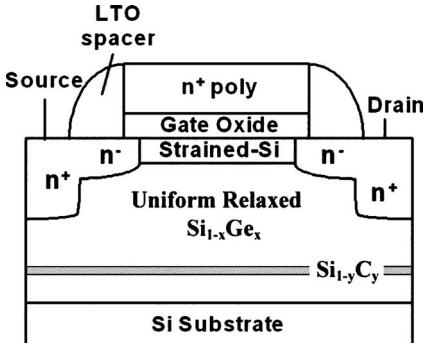

FIG. 6. Schematic presentation of strained-Si n-MOSFETs on relaxed $Si_{1-x}Ge_x$ with an intermediate $Si_{1-y}C_y$ layer (gate length/width =100/200 μm, gate oxide=30 nm).

exhibits a different relaxation mechanism.[11] Due to the much smaller lattice constant of SiC, the equilibrium critical thickness of the $Si_{1-x}Ge_x/Si_{1-y}C_y/Si_{1-x}Ge_x$ structure was reduced drastically with the carbon incorporation into Si. In the meanwhile, the interface of top $Si_{1-x}Ge_x$ and $Si_{1-y}C_y$ acted as effective nucleation sites for the misfit dislocations due to the large lattice mismatch. Therefore, strain-relieving glide of threading dislocation was facilitated during the initial epitaxial growth, preventing accumulation of the mismatch strain. This possibility involves the strain relaxation by the introduction of new misfit dislocations at the $Si_{1-x}Ge_x/Si_{1-y}C_y$ interface rather than the formation of {113} dislocation loops in the intermediate Si layer or the multiplication of preexisting dislocations via MFR mechanism in compositionally graded buffer layers. The scenario is consistent with the surface morphology observation.

High-resolution x-ray (004) rocking curves were performed to characterize the strain status of the $Si_{0.8}Ge_{0.2}$ epilayers. As shown in Fig. 4, the 300 nm thick $Si_{1-x}Ge_x/Si_{1-y}C_y/Si_{1-x}Ge_x$ structure shows an observable relaxation of about 70% as compared with the slightly relaxed bulk $Si_{1-x}Ge_x$ of 300 nm on Si. This result is consistent with our TEM observation that an intermediate $Si_{1-y}C_y$ layer serves as preferential nucleation sites for the formation of misfit dislocations to enhance the strain relaxation during the initial SiGe overgrowth. With an increase of total $Si_{0.8}Ge_{0.2}$ thickness to 800 nm, the $Si_{0.8}Ge_{0.2}$ overlayer was further found to be almost fully relaxed. From the measured frequencies of Si-Si and Si-Ge in the Raman spectrum as shown in Fig. 5,[13] the SiGe overlayer was found to possess a residual strain of merely 2%. On the other hand, the control sample without a $Si_{1-y}C_y$ layer has a residual strain up to 25%.

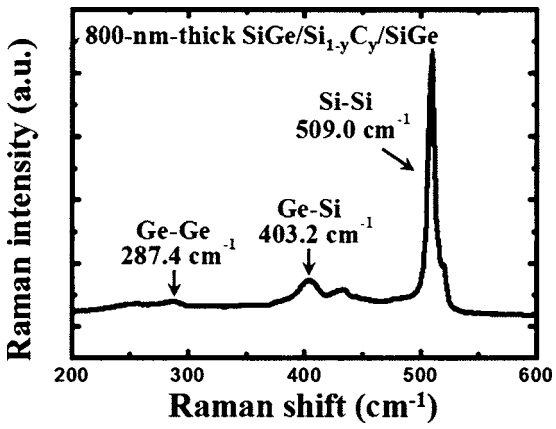

FIG. 5. Raman spectrum of a sample with the 800 nm thick $Si_{1-x}Ge_x/Si_{1-y}C_y/Si_{1-x}Ge_x$ (x=0.2, y=0.014) structure. The measurements were carried out in air at room temperature.

Comparison of experimental data for the samples with different relaxed structures and their possible relaxation mechanisms are summarized in Table I. The data show that surface morphology, threading dislocation density, and strain relaxation can be considerably improved by introducing an intermediate $Si_{1-y}C_y$ layer into the $Si_{1-x}Ge_x$ film. Furthermore, the relaxed $Si_{1-x}Ge_x/Si_{1-y}C_y/Si_{1-x}Ge_x$ structure shows almost complete strain relaxation and low threading discation density comparing favorably with the $Si_{1-x}Ge_x/Si/Si_{1-x}Ge_x$ sample in a previous study,[11] although the intermediate layers in the heterostructures play different roles during the strain relaxation.

For possible practical application, the relationships between $Si_{1-x}Ge_x$ and $Si_{1-y}C_y$ growth parameters are addressed. When Ge composition (x) of $Si_{1-x}Ge_x$ layer increases, the carbon concentration (y) in $Si_{1-y}C_y$ layer needs to be reduced to keep the same strain profile in the system. On the other hand, the carbon concentration used is also limited by the inherent characteristics using UHV/CVD system. For example, the y, 0.014, used in this work is the maximum carbon concentration to prepare defect-free $Si_{1-y}C_y$ layer in our system. The further increase of carbon concentration could results in a poor-quality $Si_{1-y}C_y$ film. In a previous study on the $Si_{0.8}Ge_{0.2}/Si/Si_{0.8}Ge_{0.2}$ structures, it was found that a thinner (<25 nm) or thicker (>100 nm) Si layer could lead to poor strain relaxation.[11] Similarly, an optimal thickness of $Si_{1-y}C_y$ layer should exist for a given $Si_{1-x}Ge_x/Si_{1-y}C_y/Si_{1-x}Ge_x$ structure. If the buffer layer is too thin or too thick, the surface would act as bulk SiGe or bulk Si so that the effectiveness to relax the strain is reduced. In view of the critical thickness of total system, the $Si_{1-y}C_y$ thickness is predicted to be reduced to avoid local strain

TABLE I. Comparison of experimental data and relaxation mechanism for the 800 nm thick $Si_{1-x}Ge_x$ ($x=0.2$) epilayers with the different relaxed structures.

Samples	Relaxation (%)	TD[b] density (cm^{-2})	Roughness (nm)	Shallow pit density (cm^{-2})	Main relaxation mechanism
$Si_{1-x}Ge_x/Si_{1-y}C_y/Si_{1-x}Ge_x$	98±2	$(5.5\pm2.5)\times10^5$	4.2	$<10^3$	Misfit dislocation array
$Si_{1-x}Ge_x$ on bulk Si	75±5	$>10^8$	13.2	$(7\pm2.4)\times10^5$	Surface modulation
$Si_{1-x}Ge_x/Si/Si_{1-x}Ge_x$[a]	97±2	$(8.9\pm2.6)\times10^5$	3.0	$<10^3$	{113} dislocation loops in Si
Graded buffer structure	88±4	$(5.1\pm2.0)\times10^5$	6.4	$<10^3$	MFR mechanism

[a]Reference 11.
[b]Threading dislocations.

relaxation during $Si_{1-y}C_y$ growth as the thickness and Ge composition of $Si_{1-x}Ge_x$ layer increases. However, the precise correlation between the optimal $Si_{1-y}C_y$ thickness and the composition of $Si_{1-x}Ge_x$ layer is still under investigation.

Long-channel strained-Si *n*-MOSFETs with various relaxed $Si_{1-x}Ge_x$ substrates as well as Si control devices were fabricated to extract the effective electron mobility μ_{eff} in the strained-Si channel. Figure 6 shows the schematic diagram of surface-channel strained-Si *n*-MOSFETs with the relaxed $Si_{1-x}Ge_x/Si_{1-y}C_y/Si_{1-x}Ge_x$ structure in this work. As shown in Fig. 7(a), both strained-Si and bulk Si control devices show the excellent subthreshold behavior and low off-state leakage. The effective mobility μ_{eff} calculated from the split capacitance-voltage measurements and a universal mobility representing an *n*-MOSFET is shown in Fig. 7(b).[14] The peak electron mobility for the device with the 800 nm thick $Si_{1-x}Ge_x/Si_{1-y}C_y/Si_{1-x}Ge_x$ structure was found to be 95% higher than that of Si control device, and slightly higher than that of device with a graded buffer layer. This is due to the preferential occupation of electrons in the lower-energy Δ_2 conduction band valleys with reduced effective mass and higher mobility in strained Si. It is worthwhile to point out that the device with the 300 nm thick $Si_{1-x}Ge_x/Si_{1-y}C_y/Si_{1-x}Ge_x$ structure also shows 55% higher mobility than that of the Si control device due to the apparent relaxation. In addition, these strained-Si devices exhibit the similar enhancement of the output current in the drain current I_d versus drain-source voltage V_{ds} characteristics. These results highlight the potential of the $Si_{1-x}Ge_x/Si_{1-y}C_y/Si_{1-x}Ge_x$ multilayer structures replacing the much thicker graded buffer layer to fabricate high-speed strained-Si devices.

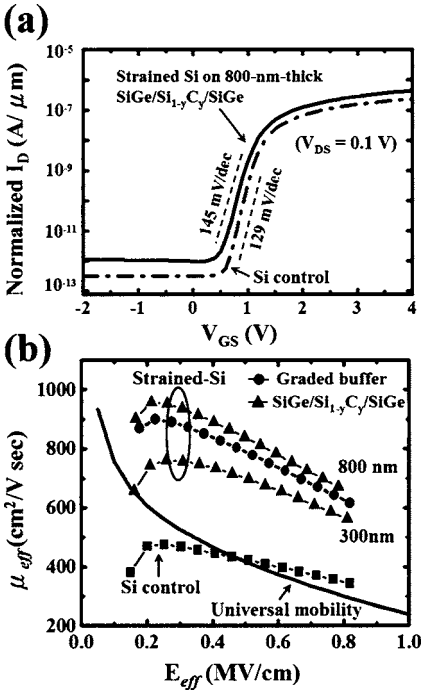

FIG. 7. (a) Subthreshold characteristics of strained-Si and Si control *n*-MOSFETs. (b) Effective electron mobility μ_{eff} of strained-Si *n*-MOSFETs with various relaxed $Si_{0.8}Ge_{0.2}$ structures as a function of effective electric field E_{eff}.

IV. SUMMARY AND CONCLUSIONS

In summary, a simple method using a $Si_{1-x}Ge_x/Si_{1-y}C_y/Si_{1-x}Ge_x$ multilayer structure to grow the high-quality relaxed $Si_{1-x}Ge_x$ has been demonstrated. The results indicate that the $Si_{1-y}C_y$ layer serves as preferential nucleation sites for misfit dislocation array to relax the mismatch strain during the initial SiGe overgrowth. The 800 nm thick $Si_{1-x}Ge_x/Si_{1-y}C_y/Si_{1-x}Ge_x$ ($x=0.2$, $y=0.014$) heterostructure was demonstrated to be almost fully relaxed with a low threading dislocation density. Effective electron mobility for the strained-Si device using this novel substrate technology was found to be 95% higher than that of Si control device. The work demonstrates a useful way to fabricate high-quality relaxed epilayers with large lattice mismatch.

ACKNOWLEDGMENTS

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