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A new transferred ultra-thin silicon micropackaging

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Abstract
We report on a novel device-scale packaging by transferring an ultra-thin silicon (UTSi) capping structure, which may encapsulate microdevices. The UTSi was fabricated to form a recessed structure on the carrier glass, and then transferred on to a host substrate, thus forming a micro encapsulation. In this approach, the flip-chip assembly and tether-broken techniques are successfully utilized in demonstrating the transferred microcap on the selective area of the host substrate that is aligned through the transparent glass. Furthermore, the robustness of the UTSi microcap is even superior to those used in the poly-Si surface micromachining technique due to the high stiffness structure. As a result, the micro encapsulation presents a new packaging technique with advantages of area-selective three-dimensional micropackaging, hermetic sealing, robustness, integrated circuit packaging process compatibility and, potentially, wafer level packaging.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Ultra-thin silicon (UTSi) chips have recently been driven in mobile electronic products such as 'Smart Lebels' or flexible electronics [1]. With the development of wafer thinning techniques, the 20–50 μm thin chips have exhibited feasibility, compactness and excellent mechanical flexure, which is particularly beneficial for conforming nonplanar surfaces and allowing stacking for a three-dimensional (3D) micropackaging [2]. Such a thin chip opens up a wide range of possibilities and applications at all levels of miniaturization.

In this paper we attempt to integrate ultra-thin chips into the emerging microelectromechanical systems (MEMS) applications due to their ultra-thin characteristics. In the field of MEMS, the packaging of micromachined devices presents significant challenges that have been notorious in a non-standard procedure for diverse applications [3–6]. As a result, MEMS packaging still accounts for 50–80% of manufacturing costs [7, 8]. If the MEMS packaging procedure is able to be compatible with conventional integrated circuit (IC) packaging techniques, a learning curve of device commercial realization can be greatly reduced.

In this paper, by taking advantage of UTSi wafers as microcaps, we report on a micromachined device-scale micropackaging, as shown in figure 1. This approach to micromachining UTSi is able to encapsulate movable, 3D elements in hermetic sealing, protecting from the damage of back-end processes, and undesirable physical attacks. Moreover, the subsequent procedures are capable of utilizing conventional IC packaging techniques, minimizing changes with an introduction of integrated MEMS devices.

2. Fabrication and assembly

The microcap is accomplished using a flip-chip solder-bonded assembly that is transferred from a glass carrier to a target substrate. The carrier Pyrex glass is first lithographically patterned and etched in depth to form the pits (figure 2(*a*)). The UTSi wafer is anodically bonded to a Pyrex glass (figure 2(*b*)).

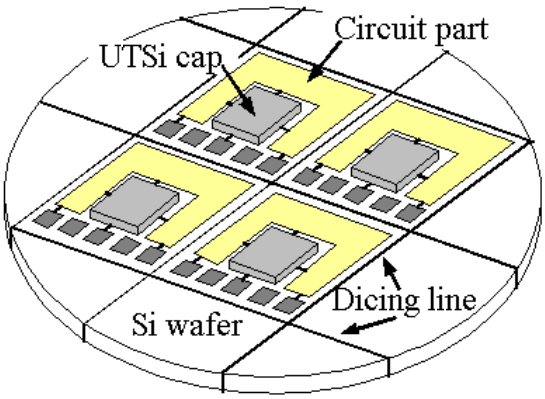

Figure 1. A device-scale encapsulation for MEMS device whose subsequent procedures can align to a standard IC packaging.

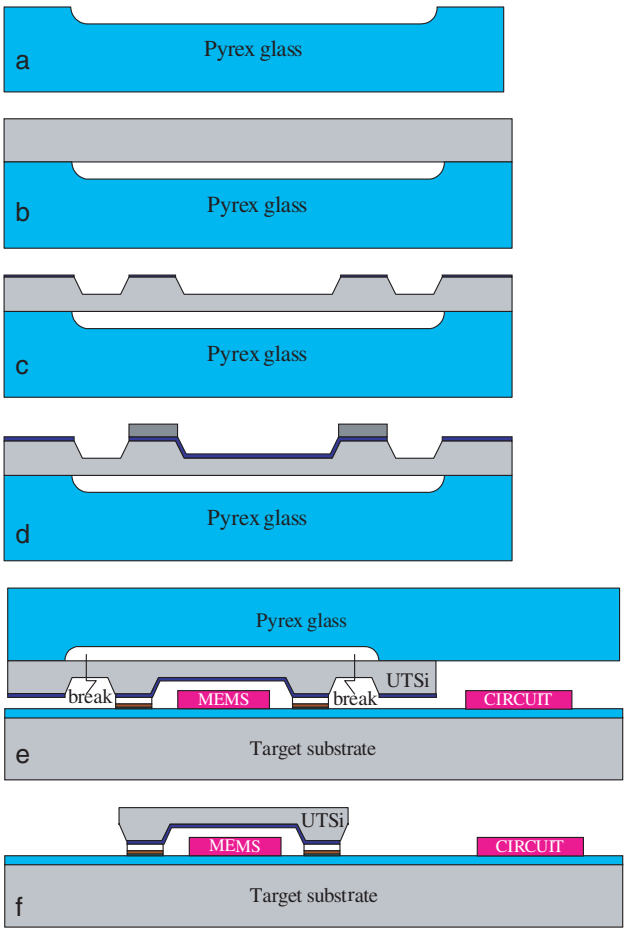

Figure 2. Process of the device-scale UTSi micropackaging: (*a*) BOE etches a pit on a Pyrex glass, (*b*) UTSi and glass anodic bonding, (*c*) capping structure KOH-etching, (*d*) solders electroplating and reactive ion etching, (*e*) alignment and bonding to a host device/substrate and (*f*) separation of UTSi microcaps and a glass carrier.

A nickel film is then deposited and serves as an etching mask. After a precise time-controlled etch, the Si housing structure is then formed (figure 2(*c*)). A second nickel film is deposited to define the capping structure. Afterwards, the PbSn solder bumps are formed by electroplating. By using reactive ion

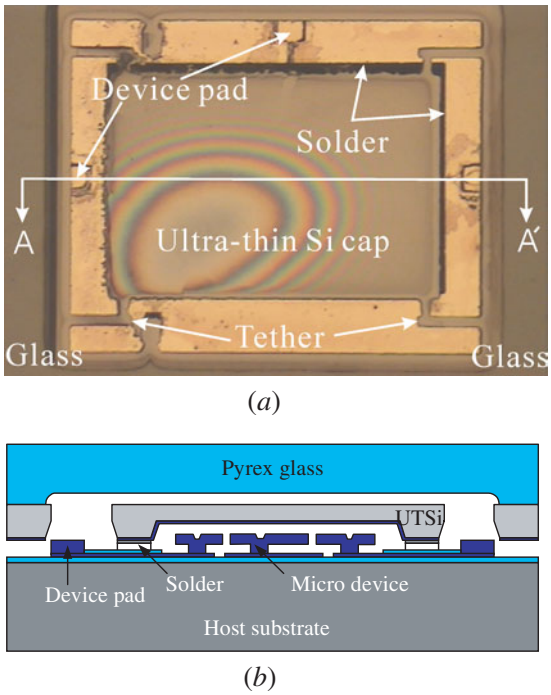

Figure 3. Visual alignment of the flip-chip assembly is achieved through the transparent Pyrex glass: (*a*) top view photo, (*b*) side view along AA′.

etching (RIE), the resultant UTSi cap is freed and suspended through four long tethers attached on the carrier glass (figure 2(*d*)). The capping structure is then visually aligned through the transparent carrier glass and bonded to a target device wafer in a heated vacuum oven with a low temperature of around 200 °C (figure 2(*e*)). The final procedure is to remove the carrier glass from the bonded area. The carrier glass is pulled upwards such that the tethers are all fractured, leaving the UTSi microcap on the host substrate (figure 2(*f*)) [9].

Figures 3(*a*) and (*b*) show the top and side views when manufactured UTSi microstructures are bonded on to a host substrate before the separation of the glass carrier and host substrate. As shown in the top view of figure 3(*a*), the visible alignment through the transparent carrier glass is demonstrated from the top UTSi structures to the bottom device pads of the host substrate. The concentric rings occur due to the optical interference of non-planar separation between the UTSi cap structure and carrier glass.

3. Results and discussion

The transferred microcap has been successfully demonstrated, as shown in figure 4. This approach has the significant advantage of post-processes being compatible with conventional IC packaging. The present UTSi microcap that encloses an area of 740 × 1140 μm is sufficiently large to encapsulate most micromachined devices.

The solder reflow technique of the bonding mechanism is chosen to be a hermetic sealing approach because of its wettability in its molten state. A practical, simple test of

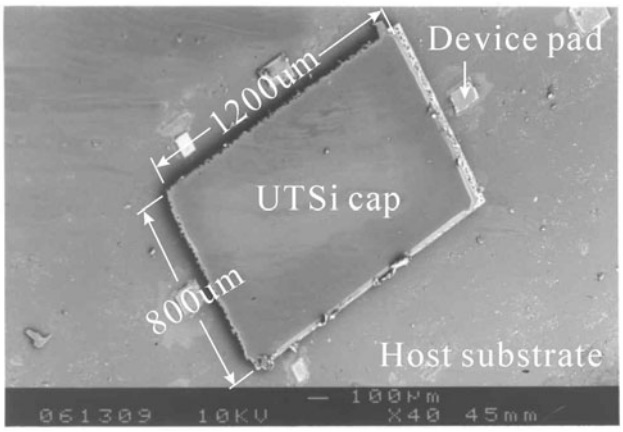

Figure 4. The UTSi (20 μm) microcaps are bonded to the host wafer.

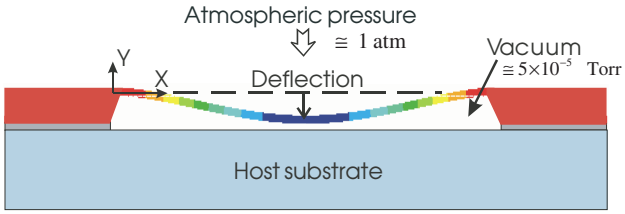

Figure 5. The hermetically sealed UTSi microcap in vacuum is deformed under an ambient environment.

a vacuum sealing is developed. Figure 5 shows that the capping Si membrane under the externally ambient pressure of around 1 atm may result in a recess deflection. An appropriate mechanical design is required to sustain mechanical strength. The membrane thickness required for a vacuum sealing can be derived from the relation of pressure versus central deflection. The peripherial condition is a clamped edge retangular plate [10]. The following relationship is derived:

$$w_{\max} = (Pa^4b^4)/[384D(a^4 + b^4)] \quad (1)$$

where P represents the ambient pressure, and a, b, D and $w_{\max}$ are the length, width, plate flexual rigidity and maximum deflection of the plate, respectively. The expression of plate flexual rigidity is

$$\mathrm{D} = \mathrm{Eh}^3/12(1 - \nu^2) \quad (2)$$

where h is the plate thickness, E represents Young's modulus and ν is Poisson's ratio. Figure 6 shows that the calculation and experimental data of the maximal membrane deflection in the center are well fitted. The present results also confirm that the encapsulation is vacuumed and hermetically sealed.

With the visual aid of the half microcap as shown in figure 7, it is evident that the microcap successfully forms a house on the host substrate and encapsulates a microdevice simultaneously. The thickness of the UTSi membrane is 10 μm, which is robust compared to that using the poly-Si surface micromachining technique [5].

Another advantage of the technique that uses a transparent glass as a carrier is the alleviation of the critical alignment problem, which avoids vast capital investment of high precision equipment. The glass substrate can be reused in the process.

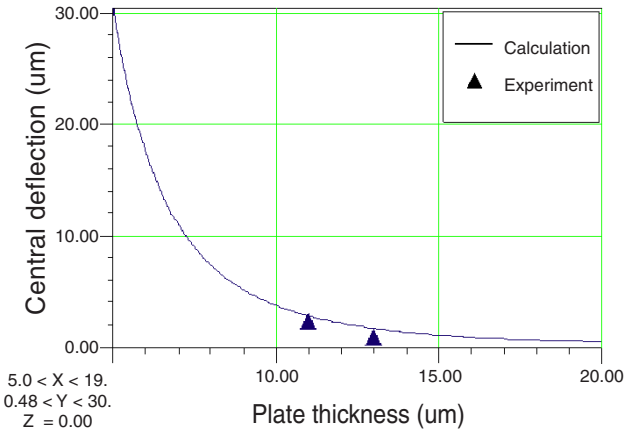

Figure 6. The central deflection of vacuum-sealed capping plate with size of 740 μm × 1140 μm.

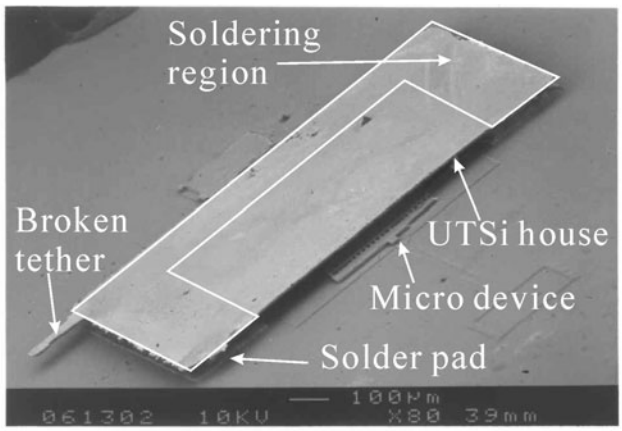

Figure 7. A mechanical resonator is housed in the transferred UTSi structure.

4. Summary

The new, transferred ultra-thin chip for micropackaging has been successfully demonstrated by flip-chip assembly and tether-broken techniques. The results can confirm a novel 3D micropackaging. With the appropriate mechanical design, the fracture can be controlled without damage to the transferred cap structure. In addition to the novel processes, the calculation of the membrane strength has also been conducted in understanding the maximal deflection due to the externally ambient pressure. The UTSi micropackaging possesses significant advantages, such as ease of alignment, low temperature bonding, high compatibility of conventional IC packaging and 3D mechanical element sealing capability. Finally, the new encapsulation approach provides a feasible process for an ultra-thin silicon wafer, and a device-scale micropackaging with a hermetic sealing.

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