Mechanical Behavior of Flip Chip Packages under Thermal Loading

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Abstract

Concern on stresses in solder bumps/underfill and warpage of flip chip BGA packages increases recently because reliability of flip chip packages relates directly to the corresponding stresses and warpage. In addition, when die size increases, the problem becomes more annoying. This problem is mainly due to mismatch in the coefficient of thermal expansion (CTE) and Young's modulus for materials made of substrate, silicon chip, underfill, and solder joints. In this paper, CTE for BT substrates were measured using electronic speckle pattern interferometry (ESPI) in different manufacturing stages to understand the effect of via drilling, Cu plating and patterning, and solder mask coating. The effect due to solder mask coating on CTE change was found to the most significant. Further, the CTE of BT substrates used in wire bond BGA packages and flip chip BGA packages varied significantly due to use of different core materials and different thickness of solder mask. On warpage measurement, 40x40 mm FCBGA with die size equal to 10x10, 20x20, and 26x26mm and thickness equal to 730 and 400um were employed and the measurement was performed from room temperature up to 225^{o}C. The phase-shifted shadow moiré technique was adopted for this warpage measurement. 2D and 3D finite element models were also constructed to analyze the warpage and stresses of these FC BGA packages. It was found that with accurate CTE data of the substrate as the input the predicted warpage was in excellent agreement with the experimental data, which made it possible to perform meaningful parametric analyses and optimal design of large-sized FC BGA packages.

1. Introduction

The mechanical behavior of a flip chip package under temperature change is always important as warpage and stresses are generated due to mismatch of the mechanical properties of the materials used to make the package. A flip chip package is usually composed of a silicon chip, solder joints, an organic substrate, and underfill. In order to understand the behavior of flip chip packages under thermal loading, numerous numerical and theoretical methods have been employed. For finite element analysis, two-dimensional and three dimensional finite element models have been constructed to study packaging deformation [1], interfacial stresses [2], solder joint shapes and stresses [3], and underfill behaviors and stresses [4] to determine the reliability of packages [5]. Parametric studies have also been presented to determine the optimal properties and dimensions of the materials and devices in packages [1-6]. On the other hand, experimental tools have been adopted to directly measure the behavior of flip chip packages at different temperatures. Full field optics methods, such as the shadow moiré, moiré interferometry, reflection moiré, or electronic speckle pattern interferometry (ESPI) schemes, have frequently been adopted. The shadow moiré method has been employed to measure the out-of-plane deformation of flip chip packages [7], and organic substrates. The resolution for shadow moiré can be enhanced by an order of magnitude if the phase shifting setup and subsequent algorithms for phase diagram construction are employed. Moiré interferometry, on the other hand, has frequently been adopted to measure the in-plane deformation of the cross sections of solder joints and flip chip packages after the temperature cools down. Because a package subjected to moiré interferometry measurement has to be cross-sectioned, the deformation on the cross section is disturbed. As a result, the measurement result may not reflect the true deformation conditions in the package. This disadvantage can be avoided by using ESPI, where the experimental setup can be arranged to measure either the in-plane or the out-of-plane deformation of the package [8-9].

In this study, we will discuss use of both the ESPI and phased shifted shadow moiré methods to measure the mechanical behavior of flip chip packages. We will also discuss how the coefficients of thermal expansion of flip chip BGA substrates at different fabrication stages are measured using ESPI, and how the out-of-plane deformation of different types of flip chip packages is measured using the phased-shifted shadow moiré and the ESPI methods. The use of two-dimensional and three-dimensional finite element models to perform parametric analyses of flip chip packages will also be discussed.

2. Flip Chip Packages

A typical picture of a flip chip package is shown in Figure 1. The flip chip packaging process generally includes wafer bumping and flip chip assembly. In the wafer bumping process, the peripheral pads on each chip in a wafer are redistributed to form area array pads. Under bump metallurgy and solder bumps are then deposited on the redistributed pads. In the flip chip assembly process, bumped chips, after being diced from a wafer, are placed on a substrate and undergo a subsequent reflow process. Underfill is then deposited to reinforce the solder bumps and enhance the reliability of the flip chip package.

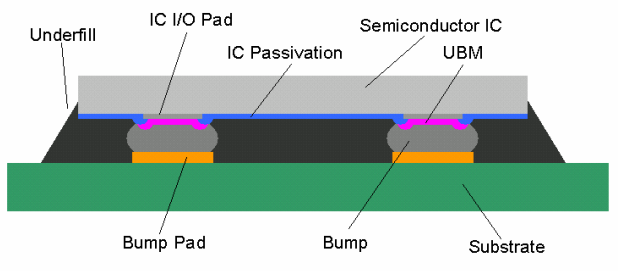


Figure 1. Schematic diagram of a typical flip-chip package

In this study, we will focus on the mechanical behavior of flip chip packages when they are subjected to different temperature conditions. Flip chip packages used for warpage measurement can be divided into four groups, as listed in Table 1. The chip sizes used are 10x10mm, 20x20mm, and 26x26mm. The thicknesses of the chips are 0.73mm and 0.40mm. The solder bump height and the pitch are 70um and 500um, respectively. The mechanical properties of the silicon chip, the solder bump and the underfill are listed in Table 2. For these flip chip packages, the substrates used are 40x40x1.12mm in size and are made of 1+4+1 build-up layers. The material data are listed in Table 3. and were provided by manufacturers. The coefficient of thermal expansion (CTE) will be verified in Section 4. Figure 2. shows pictures of Group 1, 2, 3, and 4 flip chip packages. In this chapter, we will also discuss the use of other types of substrates for CTE measurement. The results will be given in Section 4.

Table 1. Dimensions in mm of flip chip packages and the number of samples used

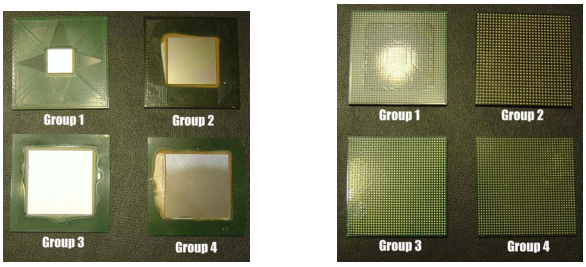
Group	1	2	3	4
Chip Size	10x10	20x20	26x26	26x26
Chip Thickness	0.73	0.73	0.73	0.40
Solder Bump Pitch	0.5	0.5	0.5	0.5
Bump Height	0.07	0.07	0.07	0.07
Substrate Size	40x40	40x40	40x40	40x40
Sub. Thickness	1.12	1.12	1.12	1.12
Sample No.	3	3	2	2

Table 2. Mechanical properties of chip, solder bump and underfill

	E (GPa)	CTE (ppm/℃)	Poisson Ratio
Chip	156	2.7	0.278
Solder Bump	57.4	24.5	0.4
Underfill	5.5	45	0.35

Table 3. Mechanical properties of the substrate used for the flip chip packages listed in Table 2.

	E (GPa)	CTE (ppm/℃)	Poisson Ratio
In-plane	24.5	12	0.143
Out-of-Plane	9.81	50	0.02



(a) (b)

Figure 2. Photographs of Group 1, 2, 3, and 4 flip chip packages. (a) Chip side; and (b) substrate side.

3. Substrate CTE Measurement

The in-plane ESPI was employed to perform in-plane deformation measurement of substrates. The specimen to be measured was supported by a small tripod inside an oven. Once the in-plane deformation had been recorded, with knowledge of the temperature change, the equivalent CTE value was calculated.

In this study, two types of BT substrates were used to perform CTE measurement. In the first group of CTE measurements, six specimens were employed. The purposes of this group of measurements were (a) to verify the accuracy of the ESPI method by measuring the CTE values of aluminum and copper; and (b) to study the change of CTE values for BT substrates in different fabrication stages. Table 4. lists the specimens and their dimensions.

Table 4. Specimens used for CTE measurement

	Specimen	Dimensions (mm)
A	Aluminum	31.0x30.1x1.0
B	Copper	30.6x29.7x1.5
C	BT Laminates	35.0x35.0x0.45
D	BT Laminates with via	35.0x35.0x0.45
E	BT Laminates with via and Copper Trace	35.0x35.0x0.50
F	BT substrate	35.0x35.0x0.55

To fabricate a BT substrate for use in electronic packages, glass/BT composite laminates need to undergo drilling, via filling, trace forming, and solder mask forming processes. In this part of study, the BT substrate used in Table 4. was for BGA packaging. The final thickness of the BT substrate was 0.55mm. The in-plane dimensions of the BT substrate were 35x35mm.

For each measurement, the temperature range was 10.0oC. For each specimen, the temperature varied within the range of 50oC to 70oC. Four measurements were performed for each specimen. The results are plotted in Figure 4.1. The recorded values for aluminum and copper were 24.2ppm/oC and 18.2ppm/oC, respectively. The previously published values are 23.6ppm/oC and 18.7ppm/oC, respectively [10]. The deviation is less than 3%, which shows that the measurement method is accurate.

The measured average CTE for the BT/glass laminates was 15.86ppm/oC. This value is very close to that provided by the manufacturer, which is 15.0ppm/^{o}C (Mitsubishi Gas Chemical Co.). After the BT/glass laminates were drilled to form vias, the CTE value became 13.71ppm/^{o}C, a reduction of approximately 14%. This reduction was mainly due to the

effect of the drilled vias that served as a "cushion," enabling the BT/glass laminates to expand when the temperature was increased. Once the copper foil was plated, the CTE value increased to 14.71ppm/^{o}C, approximately a 7% increase. This increase of the CTE value occurred because the CTE value of the copper was 18.2ppm/^{o}C, i.e., 33% higher than the recorded CTE of the BT/glass laminates. The last process in substrate fabrication was deposition of the solder mask. The CTE value was found to jump to 17.45ppm/^{o}C, a 19% increase. This significant increase of the CTE value indicated that the CTE value of the solder mask is much higher than that of the BT/glass laminates. As a result, significant stresses were induced at the interfaces among the BT/glass laminates, copper foil, and solder mask. The results for CTE measurement performed at different manufacturing stages for BT substrates are shown in Figure 3.

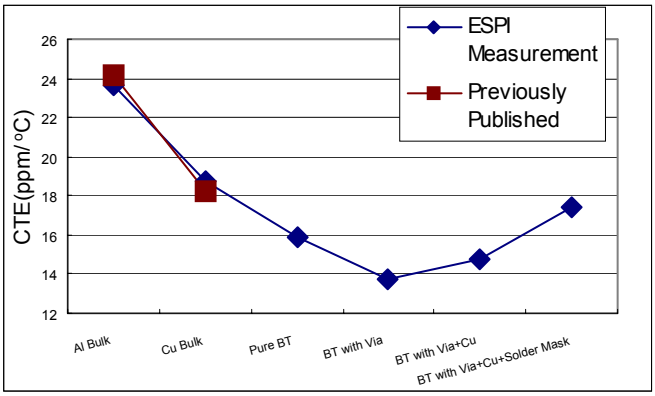


Figure 3. Measured CTE values for aluminum, copper, and BT substrates at different fabrication stages

4. Behavior of Flip Chip Packages under Thermal Loading

4.1 Warpage at Room Temperature

Figure 4. shows the warpage measurement results obtained using the shadow moiré. The flip chip packages were divided into four groups. The dimensions of the each group of flip chip packages are listed in Table 1. The plots in Figures 4.(a) are the warpage profiles measured on the chip side. Therefore, the linear dimensions of Groups 1, 2, 3, and 4 were 10mm, 20mm, 26mm, and 26mm, respectively. On the other hand, the plots in Figures 4.(b) are the warpage profiles measured on the substrate side. Therefore, the linear dimension was always 40mm. The warpage profiles of the chips in all four groups show an axisymmetrical pattern regardless of the difference for the chip size used. This axisymmetrical pattern was not observed in the warpage profile measured on the substrate side (Figure 4.(b)). In addition, when the chip size became larger, such as 20x20 mm and 26x26 mm, the warpage profiles had rhombus shapes.

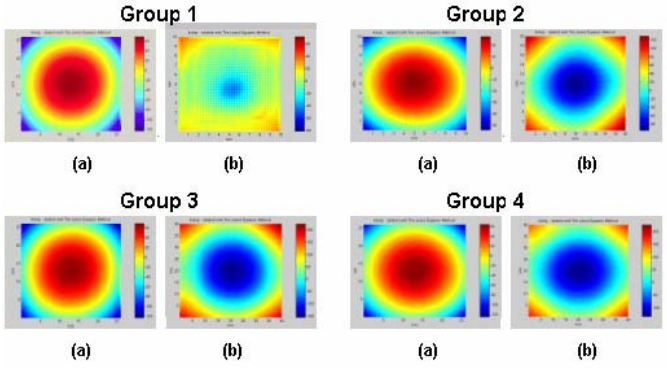


Figure 4. Warpage of flip chip packages measured at room temperature. (a) Measured on the chip side; and (b) measured on the substrate side

Table 5. lists the warpage data for the four groups of flip chip packages obtained at room temperature. The chip center was the reference point used to calculate the warpage values. Warpage 1 refers to the average warpage measured in the horizontal and vertical directions, and warpage 2 refers to the average warpage measured in the ±45 degree directions. The warpage values of the chips were smaller than the warpage values of the substrates, and the values corresponding to warpage 1 were always smaller than the values corresponding to warpage 2, as expected. On the other hand, a comparison of the Group 1, 2, and 3 results reveals that the amount of warpage increased as the chip size increased. A comparison of the Group 3 and Group 4 results also shows that warpage increased as the chip thickness decreased.

Table 5. Warpage measured at room temperature for chip and substrate of flip chip packages

	Chip		Substrate	
	Warp. 1	Warp. 2	Warp. 1	Warp. 2
Group 1	12.6	21.2	48.4	65.0
Group 2	41.9	79.1	118	205
Group 3	75.2	143	159	271
Group 4	98.6	188	193	336

4.2 Warpage at Elevated Temperatures

The maximum warpage value at each temperature for each flip chip package in Groups, 1, 2, 3, and 4 are shown in Figures 5., 6., 7., and 8., respectively. The warpage measurements on the chip side were performed at temperatures lower than 150^{o}C, mainly to keep the package from being damaged due to excessive heating at elevated temperatures. A linear relationship between the warpage measured on the chip side and the corresponding temperatures was observed in all four groups of packages. Furthermore, the chip warpage was found to approach to zero at approximately 150^{o}C. Comparing the results for Group 1, 2, and 3, one can see that the warpage increased as the chip size increased. On the other hand, a comparison of the results for Group 3 and 4 reveals that the warpage remained the same regardless of the change of the chip thickness.

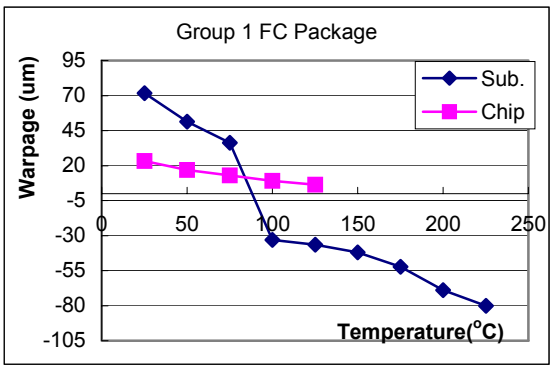


Figure 5. Warpage of the chip and substrate in the flip chip packages in Group 1

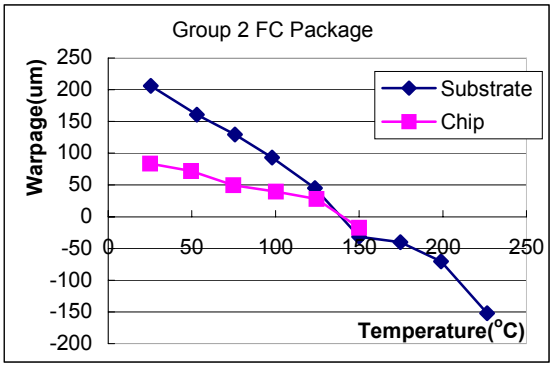


Figure 6. Warpage of the chip and substrate in the flip chip packages in Group 2

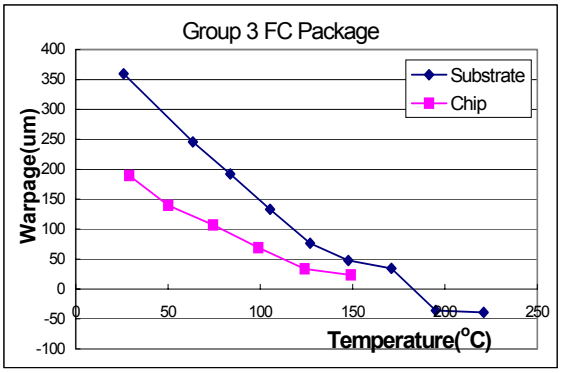


Figure 7. Warpage of the chip and substrate in the flip chip packages in Group 3

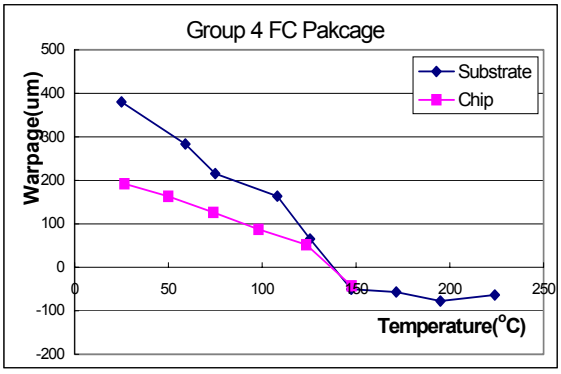
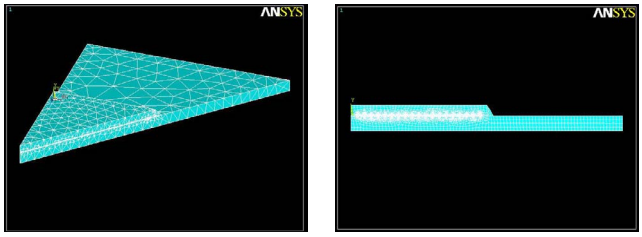


Figure 8. Warpage of the chip and substrate in the flip chip packages in Group 4

A linear relationship was also observed between the warpage measured on the substrate side and the corresponding temperatures. For the flip chip packages with 10x10mm and 20x20mm chips (Group 1 and 2), this linear relationship was found for a temperature range of from room temperature to 225°C. On the other hand, due to the constraint from the 26x26mm chips on the flip chip packages in Group 3 and 4, the substrate warpage remained unchanged as the temperature passed the glass transition temperature of the BT substrate, as shown in Figures 7. and 8. When the temperature dropped to room temperature, it was found that the warpage values measured on the substrate side became larger when the chip size increased and the chip thickness decreased.

5. Finite Element Analysis of Flip Chip Packages under Thermal Loading

Both two-dimensional and three-dimensional finite element models were constructed using ANSYS for warpage analysis of a flip chip package. The material properties adopted in these models are listed in Table 2. and Table 3. The CTE value and the Young's modulus for the 1+4+1 build-up substrate were the two most sensitive properties used in analysis. The CTE value was verified by measurement, as described in Section 4. For 3D analyses, a 1/8 model was constructed using a 10-node tetrahedral element (SOLID45) to avoid erroneous spurious shear strain [11]. The total number of elements used was 69,659. For 2D analyses, a 1/2 model was constructed. The element used was PLANE82. The total number of elements was 11,571. The finite element models discussed in this section were constructed based on the geometry of a flip chip package assembled using a 20x20mm chip. The underfill at the edge of the chip, called the fillet, was modeled so that the height would be equal to a chip thickness of 730 um and a tail length of 500um. According to the experimental results discussed in Section 5, the stress free temperature was 150°C. Therefore, the thermal loading applied in the finite element models was based on a temperature change from 150°C to 26°C. The material properties were assumed to remain constant during the change of temperature. Figure 9.(a) and (b) plot the constructed 3D and 2D finite element models, respectively.



(a) (b)

Figure 9. Plots of finite element models for (a) 3D and (b) 2D analyses. The flip chip package had a 20x20mm chip

A comparison of the experimental and numerical data for the maximum warpage values, i.e., at warpage 1 and warpage 2, is shown in Table 6. The definitions of warpage 1 and warpage 2 are the same as those given in Section 4.1. The

correlation is considered to be satisfactory. Therefore, both the 2D and 3D finite element models are considered to be accurate when adopted for warpage analysis purposes.

Table 6. Comparison of the measured data and numerical warpage predictions obtained using 2D and 3D finite element models

		Shadow Moiré	3D FEM		2D FEM	
		Result	**Result**	**Difference**	**Result**	**Difference**
Chip	**Warp.1**	41.9	45.7	8.84%	43.5	3.60%
	Warp.2	79.0	87.5	10.7%	N/A	N/A
Substrate	**Warp.1**	118	118	0%	109	-7.63%
	Warp.2	205	203	-0.86%	N/A	N/A

6. Parametric Study of Warpage for Flip Chip Packages

In this section, the results of the parametric analysis will be used to evaluate the effects of the (a) Young's modulus of the underfill, and (b) CTE of the underfill on the warpage behavior of flip chip packages. The Young's modulus and CTE of the underfill ranged from 5.0 GPa to 30GPa and from 15.0ppm/^{o}C and 52.5ppm/^{o}C, respectively. The 2D finite element model described in Section 6 was employed in this study. The analyzed chip and the substrate had square in-plane dimensions, which were 20x20mm and 40x40mm, respectively. The analyses were performed while the temperature of the flip chip package changed from 150^{o}C to 26^{o}C. The baseline model had chip and substrate thicknesses of 0.73mm and 1.12mm, respectively, and the Young's modulus and CTE of the underfill were 5 GPa and 45 ppm/^{o}C, respectively. For each parametric analysis, only one parameter was changed.

6.1 Change of the Young's Modulus of the Underfill

The Young's modulus of the underfill used in the baseline analysis was 5GPa. In this part of the study, the Young's modulus changed from 5GPa to 30GPa, i.e., a six-fold increase. The results are plotted in Figure 10. The warpage on both the chip and substrate sides increased almost linearly with the increase of the Young's modulus of the underfill. When the temperature increased, the warpage of the package with underfill increase more than the warpage of the package without underfill. This was because the solder joints functioned as cushions, absorbing the deformation due to the CTE mismatch between the substrate and chip. Once the underfill filled the gap between the chip and substrate, the deformation of the solder joints was constrained. As a result, the deformation induced by the CTE mismatch between the chip and substrate resulted in global warpage of the package because the deformation of the solder joints was now constrained by the surrounding underfill. Therefore, if the Young's modulus of the underfill increased, the warpage of both the chip and substrate in the flip chip package also had to increase, as evidenced by the results shown in Figure 10.

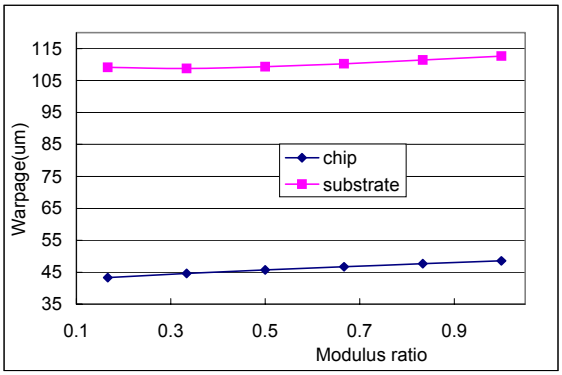


Figure 10. Effect of the change of the Young's modulus of the underfill on the flip chip warpage

6.2 Change of the CTE of the Underfill

The CTE value for baseline analysis was 45ppm/^{o}C. The analysis covered CTE values ranging from 15ppm/^{o}C to 52.5ppm/^{o}C. The results are plotted in Figure 11. The change of the flip chip warpage was not significant. However, it is interesting that the warpage change trends of the chip and substrate were different. This was due to the underfill at the edge of the chip, i.e., at the fillet location. The fillet was modeled so as to have an inclined surface. The height and tail length of the fillet were 0.732mm and 0.5mm, respectively. When the CTE of the underfill increased, due to the temperature change from 150^{o}C to room temperature, the tensile force induced by contraction at the fillet increased. As a result, the substrate warpage decreased and the chip warpage increased.

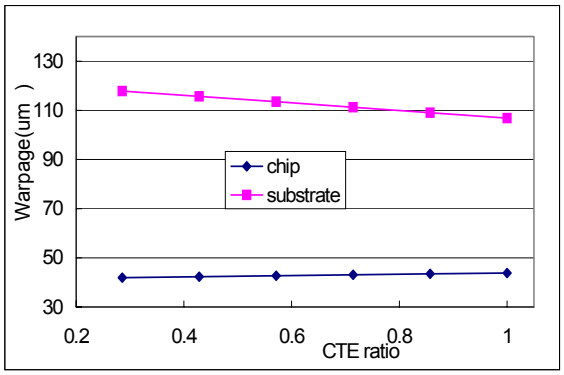


Figure 11. Effect of the change of the CTE of the underfill on the flip chip warpage

7. Summary

In this chapter, the mechanical behavior of flip chip packages has been reported in detail. The phase shifted shadow moiré approach was adopted to measure the warpage of flip chip packages, and both the in-plane and out-of-plane ESPI methods were adopted to measure the CTE values of the substrate and the warpage of flip chip packages. Meanwhile, two-dimensional and three-dimensional finite elements models were constructed for numerical analysis of flip chip packages. It was found that:

(a) The substrate CTE values varied significantly due to the use of different BT cores, numbers of vias drilled in the

substrate, and thicknesses of the copper and the solder mask. Therefore, the CTE of each substrate needs to be carefully measured so that the mechanical behavior of the corresponding flip chip package can be accurately determined.

(b) At room temperature, warpage of flip chip packages increased with increasing chip size and decreasing chip thickness. The warpage of the flip chip package also increased after the underfill reinforcement, and the relationship between the package warpage and the temperature changed from nonlinear to linear.

(c) The flip chip warpage was found to decrease to zero when the temperature increased to around 150^{o}C. Linear relationships between the warpage values, for both the chip and the substrate, and the corresponding temperatures were observed. When the temperature increased further, the amount of substrate warpage gradually approached to the amount of chip warpage, especially when the chip size became large, as in the packages with 20x20mm and 26x26mm chips.

(d) The parametric analysis showed that a minimum warpage value for a flip chip package could be obtained by choosing underfill materials with small Young's modulus and large CTE values.

Acknowledgments

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