A V-Band MMIC SPDT Passive HEMT Switch Using Impedance Transformation Networks

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***Abstract* — A V-Band MMIC single pole double throw (SPDT) switch using GaAs PHEMT process is designed, fabricated and tested. In contrast to the conventional resonant-type switch design method, this passive FET switch circuit utilizes impedance transformation to compensate the drain-source capacitance effect for the off-state in millimeter-wave frequency range. This SPDT switch has a measured isolation better than 30 dB for the off-state and 4 dB insertion loss for the on-state from 53 GHz to 61 GHz. The isolation performance of this design approach outmatches previously published FET switches in this frequency range.**

Index Terms- **V-Band, PHEMT, SPDT, MMIC, switches**

I. Introduction

Switches are important components in millimeter-wave (MMW) systems. Monolithic PIN diode switches has demonstrated good performance at MMW frequency [1]. However, since PIN diode process is not compatible with HEMT MMIC process, passive HEMT (or FET) switches are still very popular [2]-[6], because they can be integrated with the other major building blocks in a MMW transmit/receive (T/R) module, which are mostly fabricated using HEMT MMIC process. Most MMW monolithic passive HEMT switches reported to date were resonant-type FET switches [2]-[4], with the isolation performance lower than 30 dB. High isolation Q-band HEMT switches reported in [5], utilized two-stage un-terminated quarter wavelength shunt design to achieve up to 50 dB isolation. However, a huge chip area is required in such design. Recently, compact dc-60 GHz HJFET MMIC switches [6] were reported with reasonable isolation performance, but they required special process/layout for the ohmic electrode-sharing technology in the HEMT devices.

In this paper, a new HEMT switch design using impedance transformation concept is proposed in contrast to the conventional resonant-type design for the MMW frequency. A V-band single pole double throw (SPDT) MMIC switch using standard 0.15-□m GaAs PHEMT foundry process is designed, fabricated, and tested to verify this design concept. It demonstrated a measured on-state insertion loss of less than 4 dB with an off-state isolation of better than 30 dB from 53 to 61 GHz. The isolation performance outmatches the reported V-band MMIC FET switches [4],[6], with a slightly higher on-state insertion loss.

II. Device Characteristics and MMIC Process

The HEMT device used in this design is TRW standard 0.15-□m high linearity InGaAs/AlGaAs/GaAs PHEMT MMIC process. The HEMT device has a typical unit current gain cutoff frequency (f_T) of 70 GHz and maximum oscillation frequency (f_{max}) of 110 GHz, with a peak dc transconductance (G_m) of 580 mS/mm. The gate-drain breakdown voltage is 8 V, and the drain current at peak G_m (I_{dspk}) at 5-V drain-source voltage is 280 mA/mm. Other passive components include thin-film resistors, MIM capacitors, spiral inductors, and air-bridges. The wafer is thinned to 4-mil for the gold plating of the backside and reactive ion etching via holes are used for dc grounding.

III. Circuit Design

The dimension of HEMT device selected for this MMIC design is 200-□m total gate width with four finger. The equivalent on-state (V_{gs} = +0.5 V) series resistance of this passive HEMT is 2.9 □ while the off-state (V_{gs} = -3 V) series capacitance is 27 fF. In previously reported MMW designs, the FET with a resonant inductor was either directly shunt to ground [2]-[4], or shunt with a quarter-wave length line [5], as shown in Fig. 1. In our design, the resonant inductor is replaced by a series impedance transformation network to the HEMT device and then the HEMT with the transformation network is

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shunt to ground to serve the switching function. The schematic diagram is presented in Fig. 2.

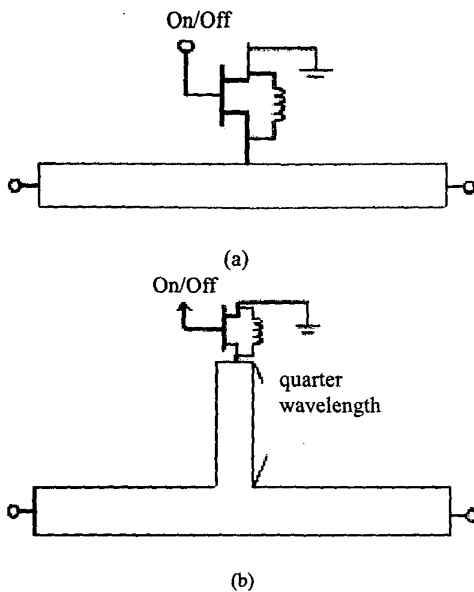

Fig. 1. (a) The schematic representations of shunt resonant FET, and (b) shunt resonant FET with quarter-wave length line.

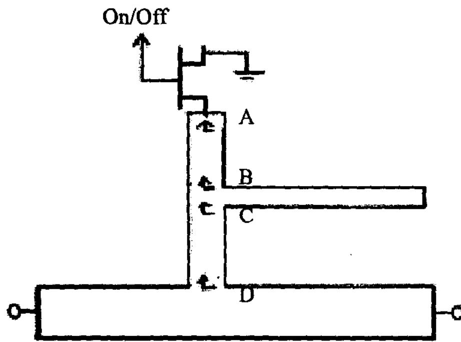

Fig. 2. Schematic diagram of a shunt reactively matched passive FET switch with impedance transformation network.

To design the impedance transformation network for the passive HEMT switch, the input impedance of both on and off-states need to be considered simultaneously. The matching network shown in Fig. 2 is composed with a series high impedance line, followed by an open stub and another series high impedance line. The input impedance values at 60 GHz looking into points A, B, C, D in Fig. 2 for both on- and off-states were indicated on the Smith chart shown in Fig. 3. As observed on the Smith chart, the input impedance values of both the on- and off-states for a non-resonant shunt FET (point A's) can be successfully transferred to a near short (small resistor) and near open (point D's), respectively, through the same impedance transformation network by carefully selecting the length of each high impedance line.

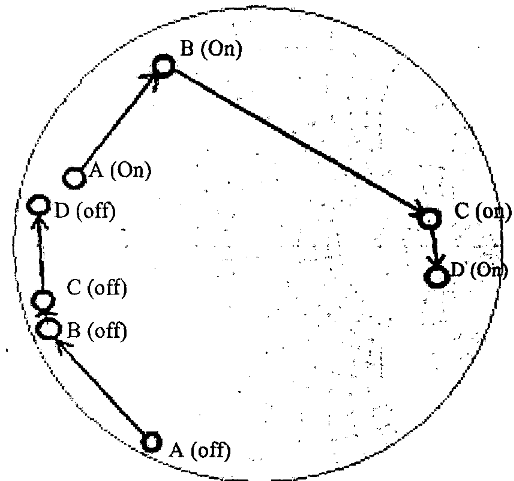

Fig. 3. The input impedances looking into points A, B, C, D of the passive switch with impedance transformation network in Fig. 2 on the Smith chart for both on- and off-states at 60 GHz

The complete SPDT switch circuit schematic diagram is shown in Fig. 4. In each path, two cascaded shunt passive HEMTs devices with the impedance transformation networks were used to enhance the isolation. The chip photograph is shown in Fig. 5, with a chip size of 2 mm x 1 mm.

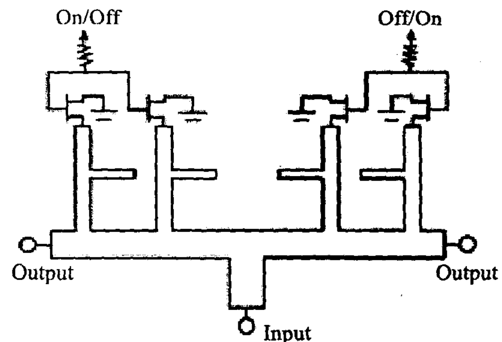

Fig. 4. The complete schematic diagram of the V-band SPDT switch using shunt passive HEMT with impedance transformation network.

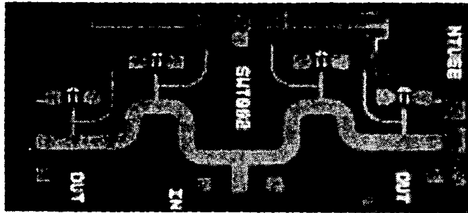

Fig. 5. Chip photograph of the V-band MMIC SPDT switch, with a chip size of 2 mm x 1mm.

IV. CIRCUIT MEASUREMENT

The V-band SPDT MMIC switch is measured via on-wafer probing. The on- and off-states two-port small-signal S-parameters of each path were obtained by terminating the output port of the other path. Both on-state insertion loss and off-state isolation from 50 to 70 GHz are plotted in Fig. 6. The control voltage for each path is +0.5 V for the on-state and –3 V for the off-state. The insertion loss is between 3.5 and 4 dB and the isolation is better than 30 dB from 53 to 61GHz. The best isolation is 35 dB at around 56.5 GHz.

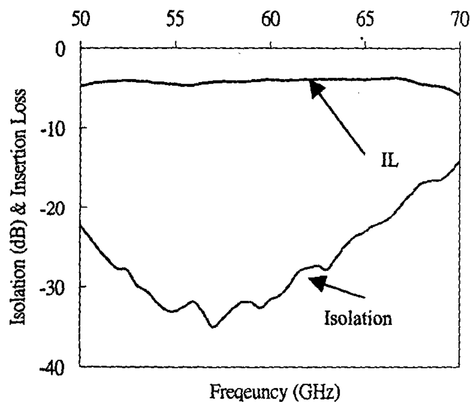

Fig. 6. Measured on-state (V_{ds} = 0, V_{gs} = +0.5 V) insertion loss and off-state (V_{ds} = 0, V_{gs} = -3 V) isolation of the V-band MMIC SPDT chip from 50 to 70 GHz.

Table 1 summarizes the previously reported performance and features of passive FET MMIC switches from Ka- to V-band. The isolation of the Q-band switches [5] achieved the best isolation at the cost of large chip area. For V-band switches, the isolation performance in this work outmatches the other designs at similar frequencies [4], [6] with a comparable chip size of [4], and a slightly higher on-state insertion loss. It is also observed that the isolation of this passive FET switch using impedance transformation is better than those of the resonant type MMIC FET switches [2]-[4].

V. SUMMARY

We have demonstrated a passive FET design using impedance transformation in MMW frequency range. A V-band SPDT MMIC switch using HEMT process was designed and fabricated to verify this design concept. The MMIC chip has a measured isolation of better than 30 dB from 53-61 GHz, which outmatches the conventional resonant type FET MMIC switches at similar frequencies.

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Author	Schindler et al. (Raytheon) [2]	Bernkopf et al. (Raytheon) [3]	Lan et al. (Hughes) [4]	Ingram et al (TRW) [5]	Mizutani (NEC) [6]	This work
Device	MESFET	MESFET	MESFET	GaAs HEMT	HJFET	GaAs HEMT
Design Approach	Shunt	Shunt	Shunt	Quarter wave-length Shunt	Series-shunt; Ohmic Electrode-Sharing Technology (special process/ layout required)	Shunt with impedance transformation network
Number of stages	2	2	2	2	-	2
Freq. Range (GHz)	20-40	15-30	56-64	42-46	DC-40 (SPDT) DC-60 (SPSP)	53-61
Insertion Loss (dB)	2 @ 40GHz	2-3	<3.2	<1.6	<3.5 (SPDT)	<4
Isolation (dB)	25-28	>20	>23	35-50	>25 (SPDT)	>30
Chip Size (mm^2)	-	2x2.2	0.8 x 2.45	5x2	0.86x0.64	2x1

Table 1. Summary of the performance and features of previously reported passive HEMT MMIC switches and this work from Ka- to V-band.