DESIGN AND IMPLEMENTATION OF AN ALL-DIGITAL QPSK DIRECT-SEQUENCE SPREAD-SPECTRUM TRANSCEIVER IC

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Abstract

In this paper, an all-digital differentially encoded quaternary phase shift keying (DEQPSK) direct sequence spread-spectrum (DSSS) transceiver is proposed. It consists of two parts: a baseband/IF spread-spectrum transmitter and a coherent intermediate frequency (IF) receiver. The center frequency of this IF receiver is 11MHz and the sampling rate is 44 Msamples/second. Modulation/demodulation, carrier recovery, PN code acquisition, and differential coding are all provided within a single chip. Functional optimization and architecture design have been done before layout implementation. Furthermore, we added testing circuits in this chip and thus each functional block is easily tested. The chip was fabricated through TSMC 0.8μm n-well CMOS SPDM technology. The maximum operational clock rate is measured at over 90MHz (5V, over 4Mbps), and the minimum supply voltage for 2Mbps (44MHz) rated speed is 2.6V.

I. Introduction

Wireless communication becomes an obvious trend in personal communication system in recent years. It also encourages extensive research in communication techniques and VLSI technology in order to implement the underlying radio components, such as increasing the utilization of channel bandwidth and the high demand in capacity for many applications, improving the technology to obtain a small size, low power dissipation, high speed processor, and so on. Unlike wired transmission, there are many factors that affect the quality of wireless communication, such as multipath fading and co-channel interference. All of them will degrade the communication quality and reliability.

Spread-spectrum is a technique that can solve these non-ideal problems, besides it can increase the bandwidth utilization and the system capacity. The known advantages of spread-spectrum are as follows: (a) anti-jamming, (b) interference rejection, (c) multipath protection, (d) low probability of intercept, and (e) multiple access. Spread-spectrum systems can be classified by their modulation methods. The most common modulation techniques employed are: direct sequence, frequency hopping, time hopping, and so on.

Today, a trend related to the spread-spectrum techniques is based on the commercial applications in wireless local area network (WLAN) and personal communication network (PCN). All of these products have one key component, that is, a spread-spectrum transceiver. Its speed and reliability will directly affect the overall performance. Consequently, increasing demands on transmission rate, communication quality, and security make a high speed and high performance spread-spectrum transceiver necessary.

In this paper, a transceiver for direct sequence spread-spectrum (DSSS) and differentially encoded quaternary phase shift keying (DEQPSK) modulation scheme is presented. This chip includes an IF transmitter (DSSS + DEQPSK), a direct digital frequency synthesizer, a Costas loop demodulator, and a high speed digital matched filter. It has the following properties:

- Complete 0.8μm CMOS digital direct sequence spread-spectrum transceiver.
- Ideal for wireless local area networks (WLANs) at 2Mbps, operation up to 4Mbps possible.
- Operates at 11 Mchips/sec. (44 MHz clock rate) in transmit and receive modes at a supply voltage of 2.6V.
- Programmable loop filter in order to meet different requirements or environments.
- High performance digital matched filter results in a very low acquisition overhead.
- Full duplex operation.
- Input of the receiver can be either real or complex.

II. System Architecture

The proposed architecture consists of a baseband/IF transmitter and a coherent IF receiver. The transmitter includes five parts: a serial-to-parallel converter, a differential encoder, two spreaders, a sine/cosine waveform generator, and a QPSK modulator, as shown in Fig. 1. In our architecture, the spreading code is a barker code with a length of 11 chips, thus the processing gain is about 10.4 dB.

The receiver, as shown in Fig. 2, consists of a complex multiplier, two integrate-and-dump filters, a differential decoder, a parallel-to-serial converter, a numerically controlled oscillator (NCO), a Costas estimation loop for carrier recovery, and a matched filter for PN code acquisition. For the flexibility of our system, we use a complex multiplier as the down-converter that can process either real or complex signals.

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The overall function of DSSS DEQPSK demodulation is to down-convert the input signal from IF to baseband using the complex multiplier, compute the summation of all the samples within one symbol time using integrate-and-dump filters, decode the signal dumped out using differential decoder, and finally convert the outputs of the I and Q channels into a single bit stream. However, error probability will increase if the receiver does not have correct carrier recovery because there will be interference between the I and Q channels when the phase error of the sine/cosine waves generated from the NCO becomes large. In our design, we use a Costas estimation loop to perform the carrier recovery. There exists a first order loop filter in the carrier recovery loop, and it has two programmable parameters to tune the bandwidth or the damping ratio of the loop. It can be shown that the phase error will converge to 0°, 90°, 180°, or 270° in QPSK demodulation when we use Costas estimation loop to synchronize the carrier contained in the input signal. A differential coder is then necessary for solving the phase ambiguity problem. Furthermore, in a spread spectrum system, we use the low correlation property of the sidelobe to reject noise and delayed versions of the signal. If the code within the receiver does not synchronize with the input signal, it will cause the input signal be spread out and no correct output generated. So an acquisition loop for code synchronization is mandatory. In the PN code acquisition loop, a digital matched filter was adopted to locate the position where the maximum correlation occurs and a pipeline architecture allows it to complete all operations in one symbol time. From the position computed by the matched filter, we may align the PN code and the input signal on the fly, thus reducing the bit error rate.

III. Simulation Result

Before circuit design, we used the word-length optimization method as mentioned in [8] to reduce the complexity of additional hardware required for coherent demodulation. Thus the word-lengths of several important signals in this transceiver were reduced without degrading the system performance and a smaller chip area was obtained. In our design, the A/D quantization level adopted is 6 bits; the sine/cosine waves' resolution is 6 bits; the Costas estimation loop input word-length is 12 bits; and the view port size of the digital matched filter is 4 bits.

Overall gate-level simulation results of our receiver are shown in Fig. 3 and Fig. 4. At the beginning of the simulation, our receiver is initialized with a phase error and a nonsynchronized PN code, hence the outputs of integrate-and-dump filters become small since the input signal is not synchronized. In 5μs, the matched filter locates the instant with the maximum correlation as shown inside the dash-lined circle in Fig. 3. Furthermore, one can find that the carrier is not synchronized in the first 10μs, so there is some small-scale fluctuation at the outputs of the complex multiplier. From Fig. 4, which shows a convergence curve of phase error, we see that the phase error reduces to near zero in 10μs.

IV. Layout Design and Testing Result

This transceiver was fabricated through the TSMC 0.8μm n-well CMOS technology. The die size is 4800x4800 μm^2 and its microphotograph is shown in Fig. 5. To prevent the clock skew problem, we laid out the clock buffers at the center of the chip and routed the clock signal along the opposite direction of data signals. In view of testing, we added a test bus across the whole chip vertically, making it easy to observe and control several significant nodes in the chip.

We divided our testing strategy into two parts: (a) functional test and (b) performance test. For functional testing, we implemented a test board connected to a PC and used a program we developed to verify the functionality of the chip. In addition, we used this test board to do some other measurements, such as BER and frequency-error tolerance. To simulate the channel effects, we wrote a pseudo transmitter and a pseudo fading channel to generate the contaminated input signal at the receiver. The algorithm we chose is Monte Carlo method with 10^6 input bits. Fig. 6 and Fig. 7 show the measured results of BER under AWGN and frequency error, respectively.

In addition to functional testing, we used an IMS tester to verify AC and DC performance of our chip. We measured the supply current and computed power dissipation. Fig. 8 shows maximum speed of the chip at different supply voltages. Fig. 9 illustrates power consumption of the chip running at maximum speed for different supply voltages. From these two figures, we can see that the maximum operating speed is 93 MHz, 65 MHz, 44 MHz at 5V, 3.3V, 2.6V supply voltage, respectively. At these three speeds, the power consumption of the chip is 850 mW, 234 mW, and 92 mW, respectively. Our chip outperforms all previous spread-spectrum transceiver chips in terms of speed and power dissipation (see Table 1).

V. Conclusion

In this paper, an architecture for DSSS DEQPSK baseband/IF transceiver is presented. This architecture is suitable for all-digital implementation. We have integrated the DSSS DEQPSK modulator/demodulator, the Costas carrier recovery loop, the PN sequence acquisition loop using a full digital matched filter in a single chip. This approach greatly reduces communication time between modules and increases system performance. The complexity of the hardware required at IF demodulator was minimized through word-length optimization and the functionality was verified through functional and gate-level simulations. This transceiver was fabricated through TSMC 0.8μm n-well CMOS SPDM technology. The fabricated chip was tested and proven to be functionally correct. Furthermore, the chip can work at a speed of 4Mbps at 5V supply voltage. For low power applications, this chip can be slowed down to 2Mbps (compatible to IEEE 802.11), when it draws 92mW from a 2.6V voltage supply (an 85% saving in power dissipation).

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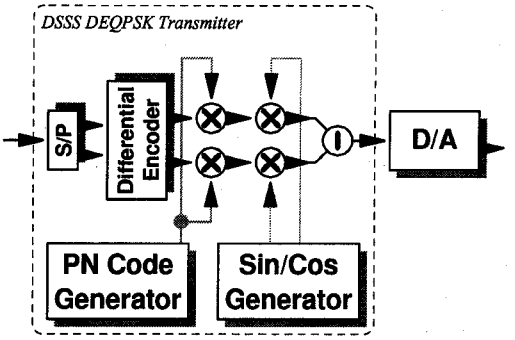

Fig.1 : Block diagram of the proposed DSSS DEQPSK transmitter.

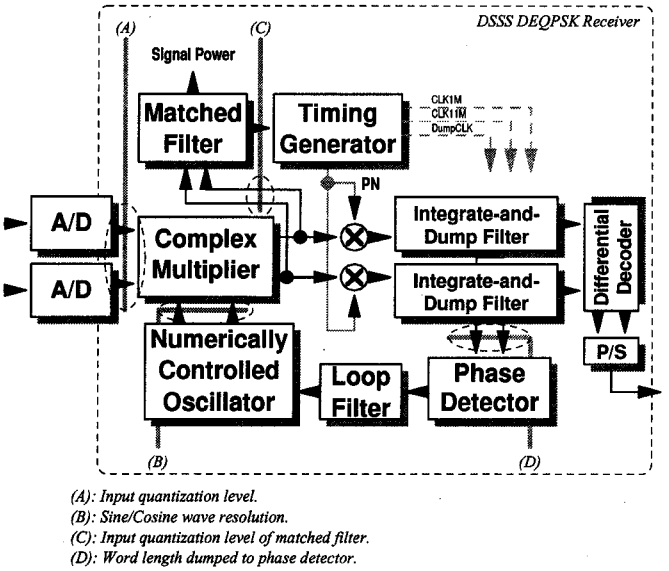

Fig. 2: Block diagram of the proposed DSSS DEQPSK receiver.

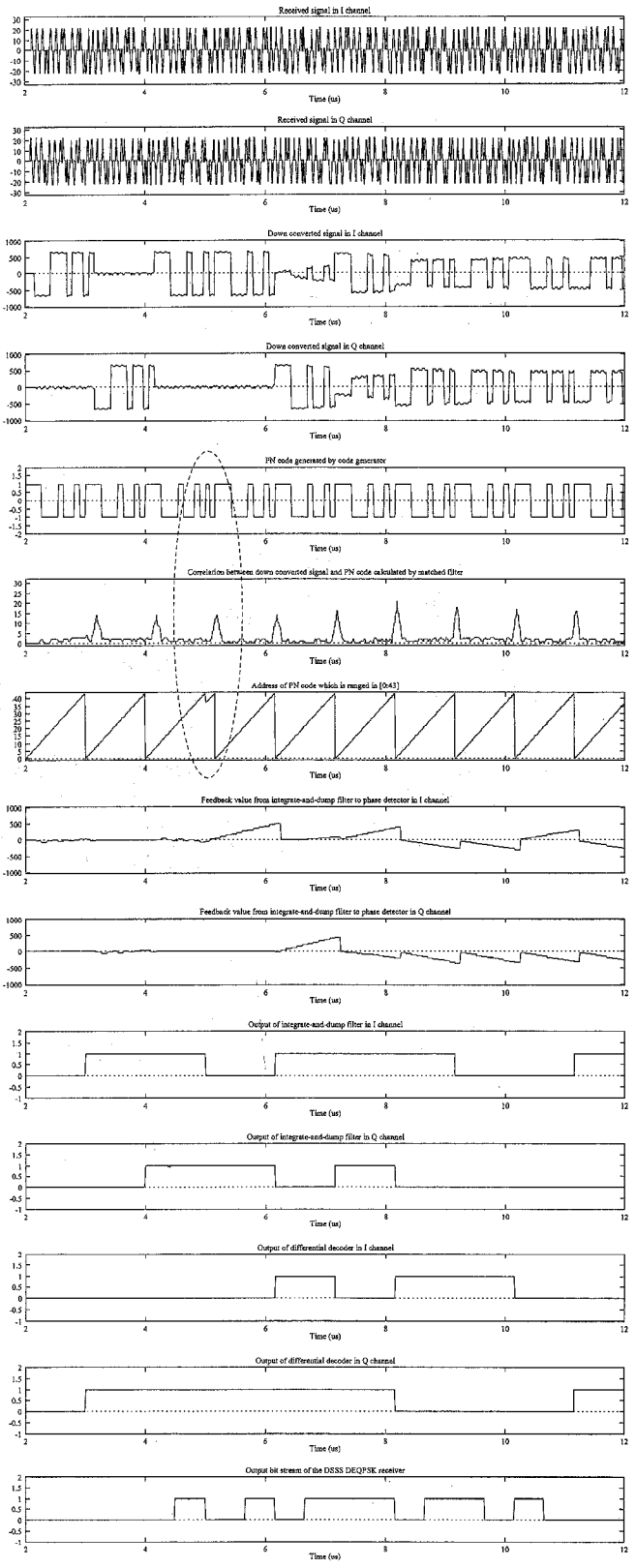

Fig. 3: Gate-level simulation result of DSSS DEQPSK transceiver (from the received signals to the demodulated result).

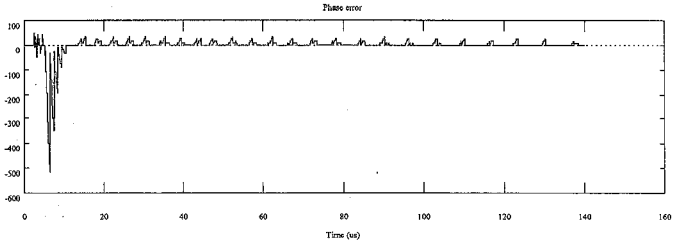

Fig. 4: Convergence curve of the phase error in the Costas estimation loop.

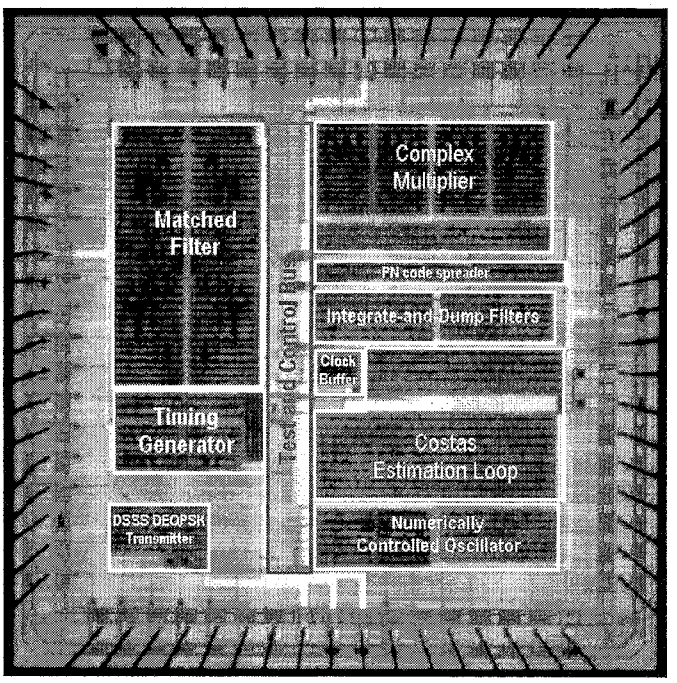

Fig. 5: DSSS DEQPSK transceiver die photo.

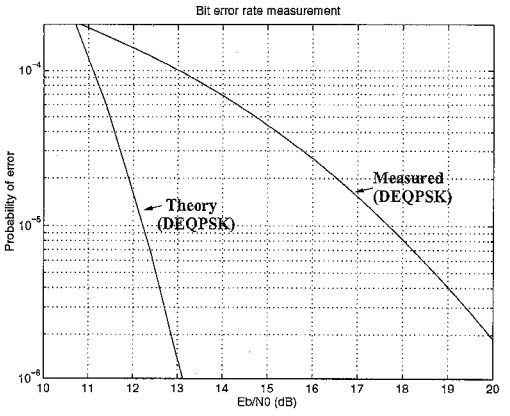

Fig. 6: Measured bit error rate.

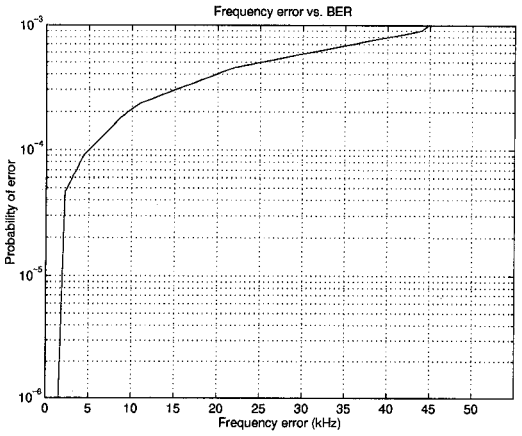

Fig. 7: Measured bit error rate for different frequency errors.

TABLE I

Comparison with other DSSS transceivers

	CYChip	STEL-2000	PA-100	MSM	SSRX	Proposed IC
Chip Rate	1 Mcps	10 Mcps	32 Mcps	1.228 Mcps	12.7 Mcps	22/11 Mcps
Porcessing Gain	12 dB at 16 kbps	18 dB at 160 kbps	48 dB at 0.5 kbps	21 dB at 9.6 kbps	21 dB at at 100 kbps	10.4 dB at 4/2 Mbps
External Components	NONE	NONE	NCO	NONE	NONE	NONE
Power Efficiency (mW/MS/s)	37.5	44	N/A	23.8	21.7	9.2 (5V, 88MHz) 2.1 (2.6V, 44MHz)
Complexity	60000 trans.	180000	N/A	450000	51000	56000
Technology	0.7um gate array	1 um CMOS	1 um gate array	0.8 um CMOS	1.2 um CMOS	0.8 um CMOS

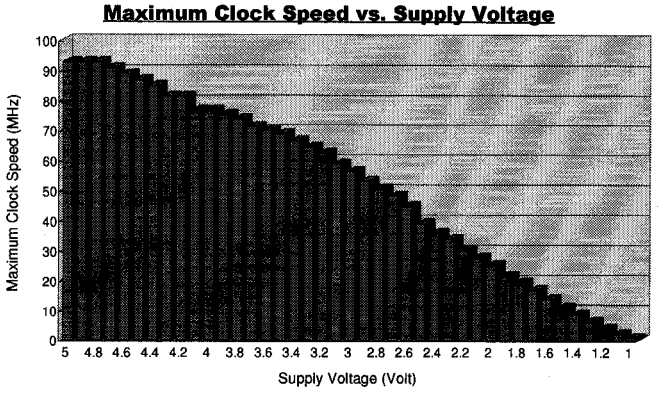

Fig. 8: Maximum clock rate vs. supply voltage.

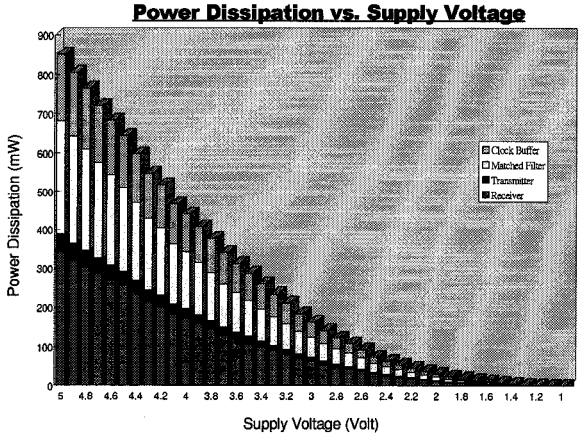

Fig. 9: Power consumption at various different supply voltages.