A V-Band GaAs HEMT Uniplanar Monolithic Integrated Antenna and Receiver Front End

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Abstract — **A V-band monolithic integrated folded-slot balanced mixer with LO source on the same chip is presented for the first time. The circuit is designed based on the uniplanar structures such as coplanar waveguide (CPW) and slotline. The embedding impedance of the folded-slot antenna is calculated by finite-difference time-domain (FDTD) method and compared with the impedance of the Schottky-Barrier diode at 60 GHz to design the mixer. The V-band voltage control oscillator (VCO) is developed based on the 0.15 μm GaAs HEMT technology. A reduced-size CPW-to-slotline transition is designed for the LO pumping network. The measured results of the VCO, transition, and mixer are included.**

I. Introduction

In recent years, the integrated antenna receiver has been used to replace traditional waveguide-based Schottky diode mixer to reduce the size, weight, and cost. Some quasi-optical mixers designed at various frequencies have previously been introduced [1]-[8]. A coupled slot antenna was used in [1] and [2] to incorporate with a local oscillator (LO) source to form a self-contained receiver at X-band. A slot ring antenna loaded by two diodes formed a balanced mixer at X-band was presented in [3]. A folded-slot antenna was investigated in [4] and two diodes mounted in the slots of the antenna to provide mixing between the received RF and injected LO signals was shown in [5] at X-band. A slot and a twin-slot antennas were used with a matching network and a HFET or a diode to form the uniplanar receiver in [6] and [7] at 40 and 90 GHz, respectively. And a modified rectangular loop slot antenna was introduced to replace the twin-slot antenna at 65 GHz in [8]. In these previous works [3]-[8], external LO circuits were used for the mixers. In [3], and [6]-[8], a waveguide horn was used to irradiate LO power to the mixers. This technique involves substantial loss of LO power. In [5], the LO signal was fed by a waveguide at X-band. Difficulties arise when one tries to feed LO power to the mixer at V-band from external LO source.

In this work, the realization of a self-contained V-band monolithic integrated receiver which employs a folded-slot antenna and a balanced Schottky diode mixer with HEMT VCO built on the same GaAs chip is presented. First, the embedding impedance of the folded-slot antenna is calculated by the FDTD method. The result is compared with the simulated impedance result of the diode to design the folded-slot balanced mixer. Then a VCO is designed based on 0.15 μm HEMT technology to provide the source of LO signal, using a similar circuit architecture reported in [9]. For the LO pumping network, a reduced-size CPW-to-slotline transition is designed based on the concept proposed in [10]. The circuit schematic diagram is shown in Fig. 1. The circuit exhibits a 9.3 dBm output power of the VCO, 50 to 70 GHz bandwidth of the transition, and 18 dB isotropic conversion loss of the integrated folded-slot balanced mixer. The circuit is suitable for applications where compact size and light weight are required.

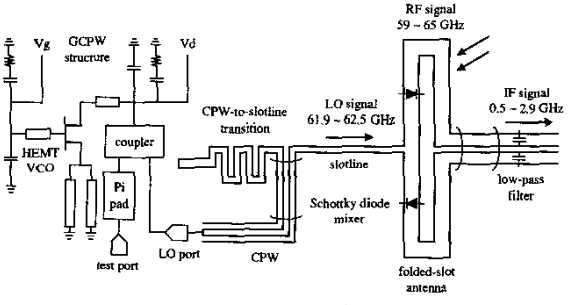

Fig. 1. The schematic diagram of the integrated antenna and receiver front end.

II. Folded-Slot Balanced Mixer Design

The architecture of the folded-slot balanced mixer is based on that described in [5]. Two diodes are mounted in the slots of the antenna to mix the LO signal injected from the slotline and RF signal received by the antenna.

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The photo of the chip is shown in Fig. 2. The CPW-to-slotline transition can be seen in the middle of the figure, where the VCO is on the left and the integrated folded-slot balanced mixer is on the right.

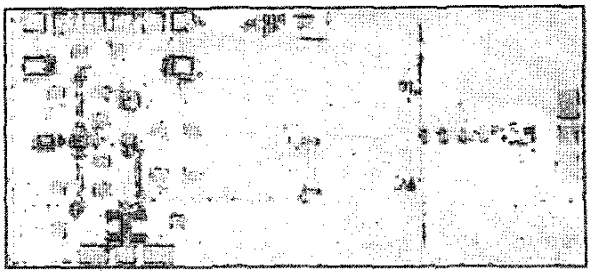

Fig. 2. The chip photo of the integrated antenna and receiver front end. Chip size is 3x1.5 mm^2.

To begin the mixer design, the diode impedance is simulated by the circuit design software Libra HP EEsof. The scaled model is used for the simulation of the two-finger 30 μm diode. The frequencies are swept form 10 to 150 GHz with 6 dBm LO power. The diode impedance can be read from the results in Fig. 3. At 60 GHz, the diode can be modeled as a *RC* parallel connection equivalent circuit, where $R = 10\ \Omega$ and $C = 0.05$ pF.

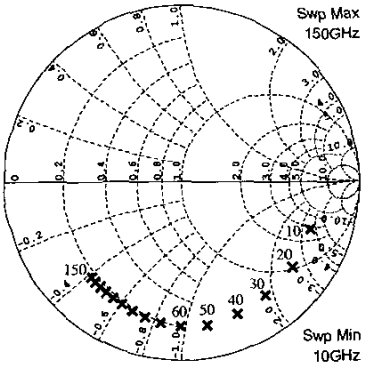

Fig. 3. Simulated diode impedance.

For the feeding of LO power to the diodes, an in-house FDTD program is written to calculate the return loss at the slotline input port. The CPW-fed folded slot antenna was previously analyzed by the FDTD method in [11]. Similar program is developed and the lumped-element modeling technique in [12] is applied here to calculate the return losses at the LO port by changing the positions of the diodes. Besides, the embedding impedances of the folded-slot antenna with diodes placed at different positions are also calculated for the RF signal matching consideration.

The quasi-optical mixer [6]-[8] are mounted on the planar surface of a dielectric lens. Since the lens is electrically large, the antenna elements act as if they are at the interface of an air-dielectric half-space. So the simulation environment is a half-space GaAs substrate in which the antenna is printed at the interface. From the simulation results, it is difficult to match the LO and RF signals to the diode at the same time. The length of the folded-slot antenna is chosen to be 1250 μm. Both the metal strip and the slot widths are 15 μm. Diodes are placed symmetrically about the LO feeding slotline and at the middle from center to edge. The simulated results of return loss and embedding impedance are shown in Figs. 4 and 5, respectively.

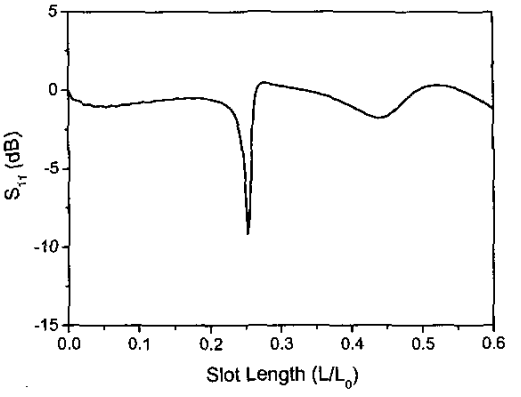

Fig. 4. Simulated return loss of LO input port.

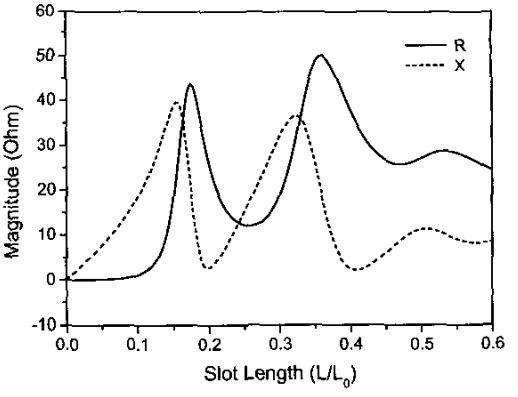

Fig. 5. Simulated embedding impedance.

The IF frequency is 0.5 to 2.9 GHz, which is much lower than the RF frequency, so it is impractical to make a low pass filter (LPF) by waveguide sections as that presented in [5] on the chip. Instead, an on-chip LPF is implemented by a 0.5 pF shunt capacitor.

III. V-BAND VCO DESIGN

A V-band VCO is designed to provide the LO power on chip based on the same architecture and design procedure as those in [9]. In order to make the circuit accommodate to the balanced mixer structure, the VCO is designed on a grounded coplanar waveguide (GCPW) structure. The GCPW is used instead of CPW to prevent the LO signal from being injection-locked to the RF signal. A four-finger 200 μm HEMT device is used. The oscillation frequency is adjusted by the gate bias voltage. The output power is coupled out of the drain terminal via GCPW edge coupled lines. A Pi pad which causes 14 dB attenuation is implemented before the test port as an isolator. A test port is used here to test the VCO operating frequency and the output power. The test port will be left open when measuring the integrated antenna mixer, so an isolator is needed to suppress the influence. The coupler is designed to have a 6 dB insertion loss at LO port and 10 dB insertion loss at test port. All the passive structures are characterized by the full-wave EM analysis.

IV. CPW-TO-SLOTLINE TRANSITION DESIGN

From the integrated antenna mixer design, the LO power is fed into the circuit from a slotline. From the VCO design, the output of VCO is a GCPW structure. So the GCPW is first transformed into CPW. Then a CPW-to-slotline transition is needed for the LO pumping network. To reduce the transition size, a planar parallel *LC* circuit composed of an interdigital capacitor and a shorted slotline stub is utilized to replace the conventional λ/4 transformer structure [10]. Based on the same design principle, the lumped-element CPW-to-slotline transition structure is implemented in V-band. The center frequency is designed at 60 GHz. To characterize the performance of such a transition, a test circuit consisting of the back-to-back connection of two such transitions is fabricated.

V. MEASUREMENT RESULTS

The chip is mounted on a 1.0 mm thick FR4 substrate (ε_r = 4.3). The on chip VCO performance is measured from the test port by the probe station and spectrum analyzer. From the relationship between LO port and test port, the output power at LO port is known. The bias voltage is V_D = 4 V and V_G varies from –0.5 to 0.1 V. The oscillation frequency is about 62 GHz. Output power is about 8~9 dBm. The results are shown in Fig. 6. A phase noise of –78.28 dB/Hz for an offset frequency of 1 MHz is read from the spectrum analyzer. And the CPW-to-slotline transition test circuit is tested via on-wafer probing and network analyzer. Measured S-parameters are shown in Fig. 7. The return losses S_{11} and S_{22} are more than 10 dB from 50 to 70 GHz. The insertion losses S_{21} and S_{12} are less than 0.7 dB in the same frequency band.

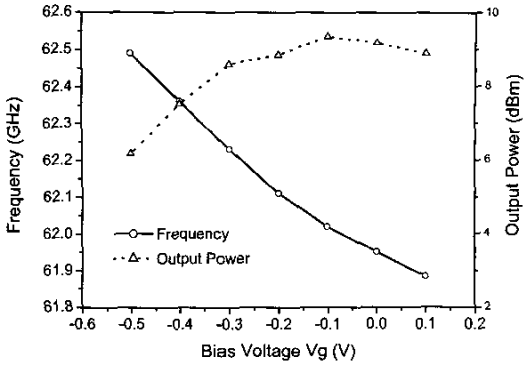

Fig. 6. The VCO oscillation frequency and output power at LO port as functions of gate voltage.

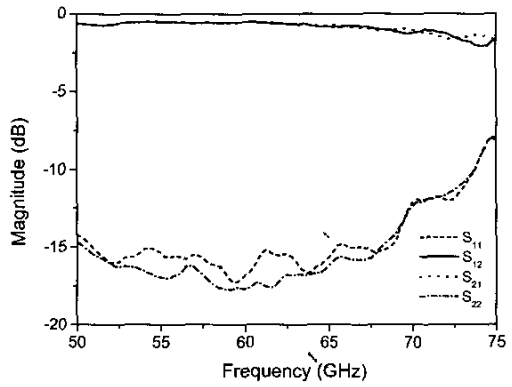

Fig. 7. Measured S parameters of the CPW-to-slotline transition test circuit.

The integrated folded-slot balanced mixer is designed as a quasi-optical mixer mounted on a silicon dielectric lens. Because the lens is not available, the chip is preliminarily mounted on the FR4 substrate. Then a V-band standard gain horn antenna is used to irradiate the RF signal to the chip. The VCO is operating at 62.0 GHz. The IF signal is picked out from the chip through the bond wires which connect the pads on the chip and the CPW line on the printed circuit board. An SMA connector and a coaxial cable are used to guide the IF signal from the printed circuit board to the spectrum analyzer. The setup is shown in Fig. 8. For simplicity, the definition of the isotropic conversion loss [1] is used to characterize the performance of the integrated folded-slot balanced mixer. Both the upper sideband and lower sideband isotropic conversion

losses are shown in Fig. 9. The conversion losses of both sidebands decrease first to a minimum level as the IF frequency increases and then increase as the IF frequency increases.

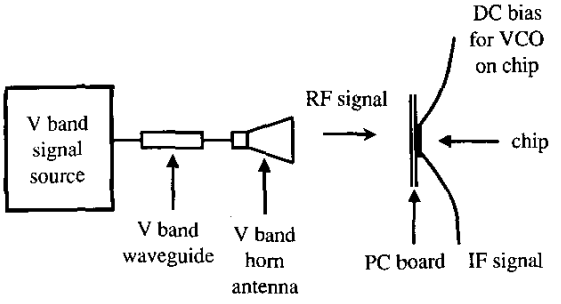

Fig. 8. The mixer measurement setup for the integrated folded-slot balanced mixer.

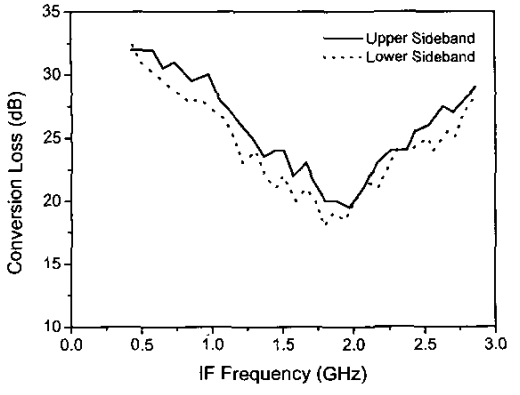

Fig. 9. The isotropic conversion losses of upper sideband and lower sideband signal versus IF frequency.

VI. Conclusion

To the best of our knowledge, this circuit is the first monolithic receiver that integrates an antenna and a mixer with a VCO built on the same chip. The chip has been designed and demonstrated at V-band. The circuit is compact and self-contained. This receiver could be mounted on a dielectric lens for millimeter-wave detector applications. It is suggested that several parameters of the antenna can be adjusted for RF signal matching to achieve further performance improvement.

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