行政院國家科學委員會專題研究計畫 成果報告

矽金氧半超薄閘極絕緣層製程研發及新型元件應用(3/3)
研究成果報告(完整版)

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行政院國家科學委員會補助專題研究計畫期末成果報告

矽金氧半超薄閘極絕緣層製程研發及新型元件應用(3/3)

第三年(95/8~96/7)期末成果報告

計畫編號:NSC95-2221-E-002-375

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一、　摘要：

本計畫在三年度之研究主要成果可分為陽極氧化生長 SiO_2 絕緣層於 SiC 基板、以硝酸氧化 Hf 金屬備製 HfO_2/SiO_2 金氧半元件結構、以硝酸氧化 Al 金屬備製 Al_2O_3/SiO_2 金氧半元件結構、及利用低功率散逸因素區域之電容特性擷取超薄氧化層厚度技術研發等四大項目。

在陽極氧化生長 SiO_2 絕緣層於 SiC 基板部份，提出將 SiC 置於純水中給予陽極氧化生長氧化層，可得到甚快之氧化層生長速率，經 850^{o}C 短時間退火後，崩潰電場達 5 MV/cm 以上，飽和電流溫度響應呈現與 n_i 值相關，對 SiC 之絕緣層備製技術改進相當有用。

在以硝酸氧化 Hf 金屬備製 HfO_2/SiO_2 金氧半元件結構部份，利用濺鍍沉積 Hf 金屬於超薄 SiO_2 上，再以硝酸將 Hf 氧化成 HfO_2，經 380~450^{o}C 之溫度處理，所得之堆疊結構呈現可達 EOT=1.5 nm 之厚度，在 2.3 nm 範圍內呈現甚佳之高介電常數絕緣層電流特性，於 1.8 nm 下等效崩潰電場可達 12 MV/cm，t_{BD} 特性顯示於 1.8V 下可達 10 年之壽命，可靠度表現佳。

在以硝酸氧化 Al 金屬備製 Al_2O_3/SiO_2 金氧半元件結構部份，利用蒸鍍沉積 Al 金屬於超薄 SiO_2 上，再以硝酸將 Al 氧化成 Al_2O_3，經 650^{o}C 之溫度處理，所得之堆疊結構呈現於 EOT=1.9 nm 下較 SiO_2 漏電流小三個數量級之高介電常數絕緣層特性，於 10K~1MHz 範圍 C-V 之變化甚小，遲滯現象可忽略，於平能帶處利用 1MHz 與 1KHz 電容所擷取之界面陷阱密度 D_{it} 約為 1.25×10^{12} $cm^{-2}ev^{-1}$，對 EOT=1.7 nm 元件經 100mA/cm^2 定電流 500 sec 施壓後，平能帶電壓移為 46 mV 之電子抓陷，施壓前後之元件電流特性變化不大，為低成本發展潛力大之高介電常數絕緣層製程。在利用低功率散逸因素區域之電容特性擷取超薄氧化層厚度技術研發部份，提出測量金氧半元件 C-V 特性時，同時測量電阻值，分析不同頻率下於不同偏壓下之供率散逸因素 D (Dissipation Factor)分布，可得知 D 值最小之區域，該區域之 C-V 特性最接近元件原有電容值，經與理論值之該區域電容隨電壓變化之回歸斜率值比對，可得知氧化層厚度。分析指出，在該區域之回歸斜率值相當敏感於氧化層厚度，借此技術可得 1.6 nm 之氧化層厚度，此厚度無法利用先前之雙頻率修正技術得之。

關鍵詞：SiC 氧化層、高介電常數絕緣層、HfO_2、Al_2O_3、超薄氧化層厚度

Abstract:

In the third year research work, there are four main subjects studied. The first is the technology of oxidation of SiO_2 by anodization in D.I. water on SiC substrate. The second is the preparation of HfO_2/SiO_2 stacked MOS structure by HNO_3 oxidation of sputtered Hf metal on SiO_2. The third is the preparation of Al_2O_3/SiO_2 stacked MOS structure by HNO_3 oxidation of evaporated Al metal on SiO_2. The fourth is the extraction of ultra-thin oxide thickness based on the portion of C-V curve with low dissipation factor.

In the first subject of the technology of oxidation of SiO_2 by anodization in D.I. water on SiC substrate, it was found that SiO_2 can be quickly grown on SiC substrate by room temperature process. After 850^{o}C anneal for 10 sec, the prepared oxides exhibit breakdown field of over 5 MV/cm. The temperature dependency of saturated current is related to n_i value. It is of importance for the preparation of insulator on SiC.

In the second subject of the preparation of HfO_2/SiO_2 stacked MOS structure by HNO_3 oxidation of sputtered Hf metal on SiO_2, the sputtered Hf was oxidized in HNO_3 to become HfO_2. The HfO_2 was the annealed at 380 ~ 450^{o}C. The samples exhibit an EOT of 1.5 nm

for the thinnest devices. Under 2.3 nm region, the structures exhibit excellent high-*k* gate dielectric performance in gate leakage current characteristic. The effective oxide breakdown field for 1.8 nm samples is larger than 12 MV/cm. The prediction of lifetime for 1.8 nm samples stressed at 1.8 V is 10 years.

In the third subject of the preparation of Al_2O_3/SiO_2 stacked MOS structure by HNO_3 oxidation of evaporated Al metal on SiO_2, the evaporated Al metal was oxidized in HNO_3 to become Al_2O_3. The Al_2O_3 was annealed at 650°C. The current is smaller than SiO_2 for the Al_2O_3/SiO_2 stacked structure with an EOT of 1.9 nm. The frequency dispersion of C-V curves measured under the region of 10K~1MHz is small and the hysteresis phenomena of the curves are also negligible. The extracted D_{it} at flat-band voltage from 1 M and 1KHz C-V curves is around 1.25×10^{12} $cm^{-2}ev^{-1}$. The flat-band voltage shift for 1.7 nm sample stressed under 100 mA/cm^2 for 500 sec is 46 mV. The electron trapping during current stress was found. The I-V curves before and after stress are almost the same. This process is cost-effective and is potential for the development of high-*k* gate dielectrics.

In the fourth subject of the extraction of ultra-thin oxide thickness based on the portion of C-V curve with low dissipation factor, it was suggested that resistance in accompany with capacitance are recorded during C-V measurement. From the analyses of the distribution of dissipation factor D versus bias voltage under various measurement frequencies, one can obtain the region with lowest D values. At these regions, the measured capacitances are close to the original capacitances without much attenuation. From the comparison of the regression slopes of capacitance versus voltage between measured data and theoretical ones, one can obtain the oxide thickness. It is noted that the regression slopes in these low D region is very sensitive to oxide thickness. The experimental observation of 1.6 nm oxide thickness was demonstrated which is unavailable to obtain via the conventional two-frequency correction method.

Keywords: SiC oxidation, High-*k* insulator, HfO_2, Al_2O_3, Ultra-thin oxide thickness.

二、緣由與目的：

在高功率元件應用中，SiC 基板具有絕佳之熱穩定性及應用性，如何生長絕緣層以便進一步做成 MOS 元件是相當重要的課題，一般而言需要甚高溫度(比如~1175°C)及甚長之時間(比如 2 hr)來進行氧化層熱生長。本計畫利用室溫下純水中以陽極氧化法即可生長得到氧化層，經證實具甚佳之絕緣特性，對 SiC 相關元件技術提供特殊之參考。

積體電路製程中，高介電常數絕緣層是相當重要的課題，許多先進的技術包括 ALD (atomic layer deposition)或 PLD (Pulsed Laser Deposition)等被相繼提出來製作超薄絕緣層，相關特性亦被詳細探討著，其中 HfO_2 與 Al_2O_3 兩者被視為重要材料之一，相關設備均相當昂貴。在本計畫中我們提出低成本之製程技術，利用先高溫生長超薄 SiO_2 界面層，再接著沉積 Hf 或 Al 薄金屬層，然後以 HNO_3 氧化金屬轉換成 HfO_2 或 Al_2O_3，再予以適當溫度之退火處理，所得之 HfO_2/SiO_2 或 Al_2O_3/SiO_2 堆疊結構經實驗證明有相當佳之電特性，由於成本低且製程容易，相當具實用價值。

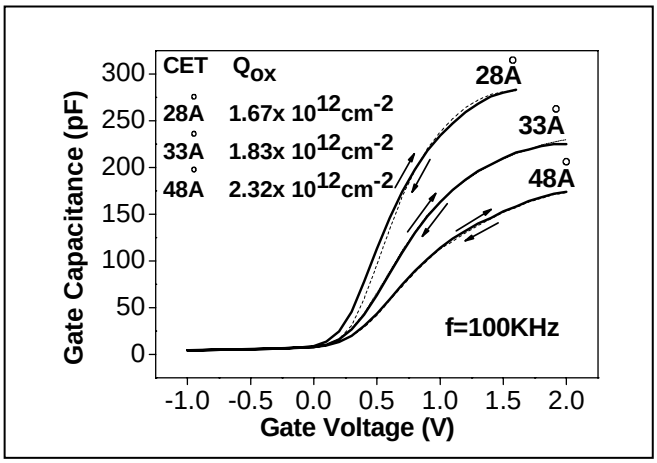
在現今 SiO_2 厚度已進入小於 2 nm 範圍內，由於漏電嚴重，在測量 C-V 時會因漏電嚴重而使電容失真，這時需經各種方式將電容修正為無漏電之電容值，才可從電容換算出氧化層正確之厚度。但因越薄之漏電越嚴重，在聚集區之修正不易，因此厚度換算之範圍有所限制。本計畫則提出利用偏壓較小之區域，漏電相對較小，元件之功率散逸因素較小，此時電容值相對失真少，再利用理論之 C-V 曲線比對，可得知氧化層之厚度。由理論分析發現，在低功率散逸因素區之電容對電壓回歸斜率是相當敏感於氧化層厚度的，只要功率散逸因素不要太大，厚度擷取之準確性甚高，本計畫研究證實可得到 1.6 nm 的氧化層厚，本研究之後續發展空間甚大，值得深入探討。

三、研究方法與成果：

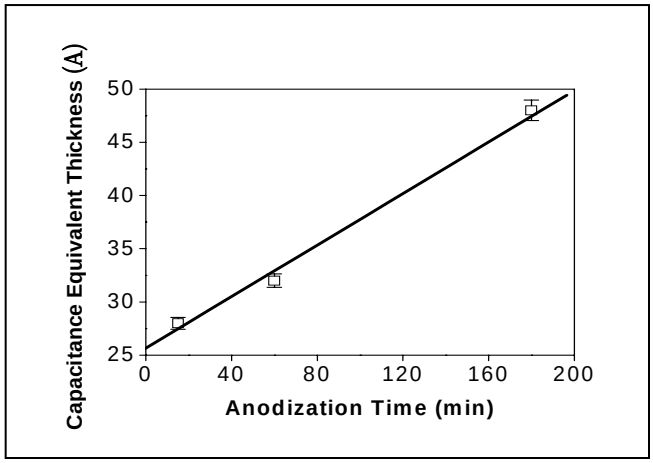
(A).陽極氧化生長 SiO_2 絕緣層於 SiC 基板

將 SiC 放置在純水中並加上電壓，經過不同時間生長厚度，之後再給予 850oC 約 10 sec

之退火處理，做成 MOS 電容元件觀察其特性，由圖一之 100 KHz C-V 特性可看出厚度有所差異，在三分鐘內即可生長得到約 5 nm 之氧化層，如圖二所示，生長速度甚快。

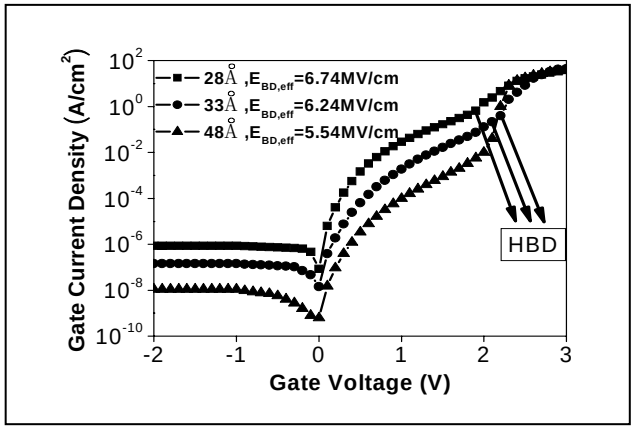


圖一



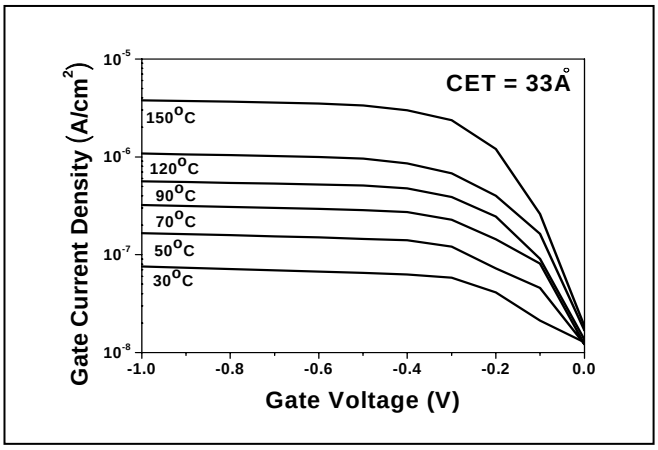
圖二

圖三為三個不同厚度元件之 I-V 曲線，可清楚看出電流隨厚度增加而漸減，氧化層之崩潰電場均達 5 MV/cm 以上。

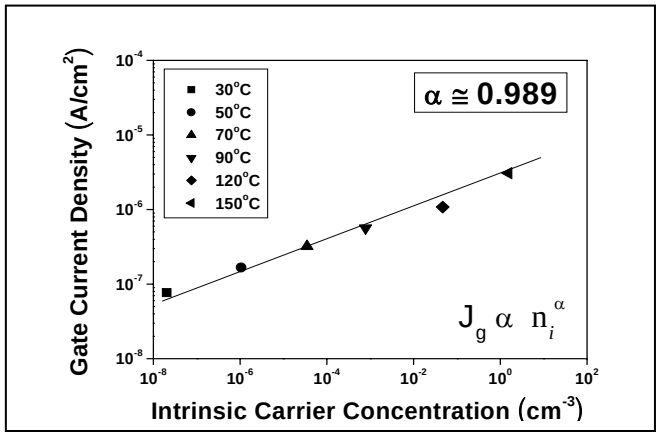


圖三

圖四為厚度 3.3 nm 元件工作於飽和電流區之溫度變化特性，可清楚看出電流隨溫度靈敏變化，為一甚佳的溫度感應器。經分析得知該電流之溫度變化可用 n_i 之值與溫度之相關性來連結，如圖五所示。

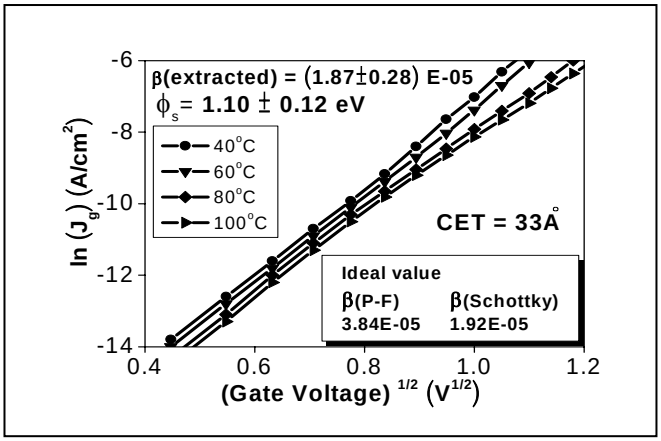


圖四

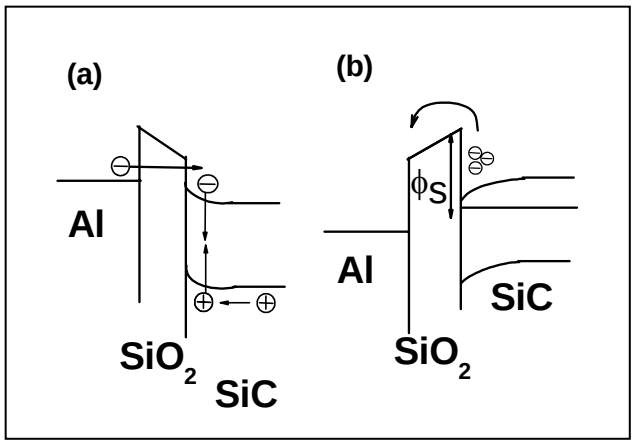


圖五

圖六為正偏壓下電流之特性分析，經比對得知與 P-F 機制不符，該電流機制是與電子之 Schottky emission 機制相關，能帶圖如圖七之(b)所示，所擷取之位障約為 1.1 eV。



圖六



圖七

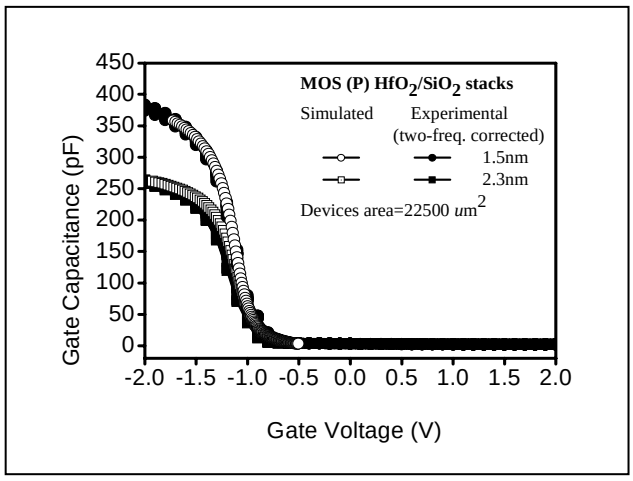
(B). 以硝酸氧化 Hf 金屬備製 HfO_2/SiO_2 金氧半元件結構

在本部份提出低成本但特性佳之高介電常數絕緣層製程技術，表一為 HO1~4 元件之製程參數，製程溫度在 HNO_3 氧化後，控制在 450°C 以下，避免 HfO2 結晶造成漏流變大。

表一

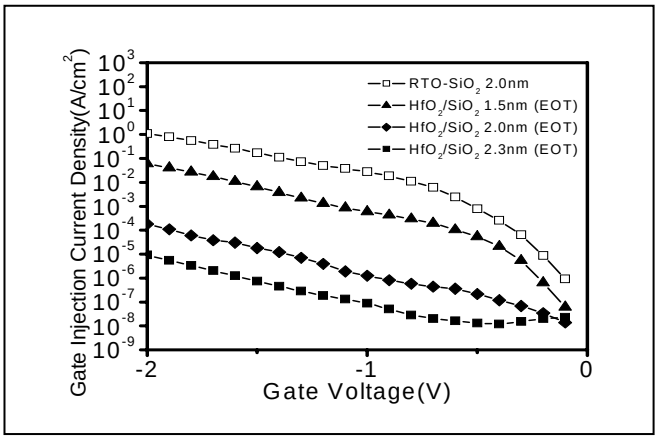
Samples	Temp. (I.L. SiO_2)	Hf sputtered thickness	HNO_3 dipped concentration and time (HNO_3:H$_2$O)	RTA Temp.	Gate material & thickness
HO1	650 °C, O2	0.5 nm	1 : 10, 30 sec	350 °C, N_2	Al, 500 nm
HO2	650 °C, O2	0.5 nm	1 : 10, 30 sec	400 °C, N_2	Al, 500 nm
HO3	650 °C, O2	0.5 nm	1 : 10, 30 sec	450 °C, N_2	Al, 500 nm
HO4	650 °C, O2	0.5 nm	1 : 10, 30 sec	450 °C, N_2	Al, 500 nm

圖八為等效厚度為 1.5 及 2.3 nm 之 HfO_2/SiO_2 堆疊結構 C-V 特性，可看出實驗與理論之特性幾乎一致，相當良好。

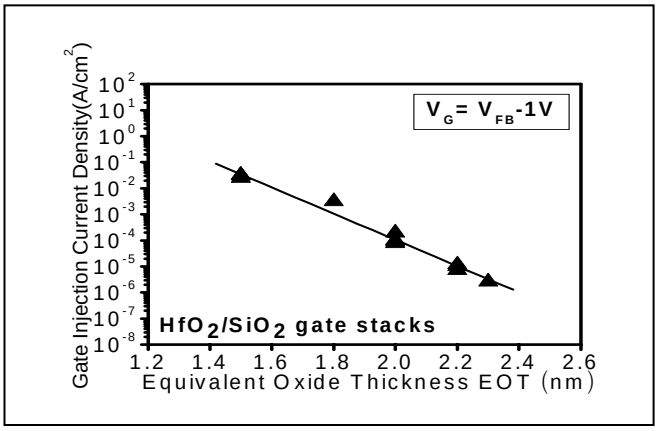


圖八

圖九為不同 EOT 之 HfO_2/SiO_2 堆疊結構與 RTO-SiO_2 之電流特性比較，可看出高介電特性相當明顯，電流較 RTO-SiO_2 為小，其 $V_G=V_{FB}$-1V 下之電流與 EOT 之關係如圖十所示，目前可得 1.5 nm 之等效厚度。

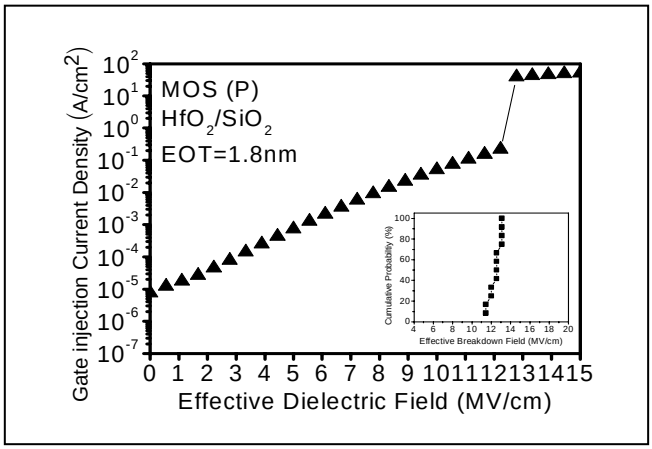


圖九



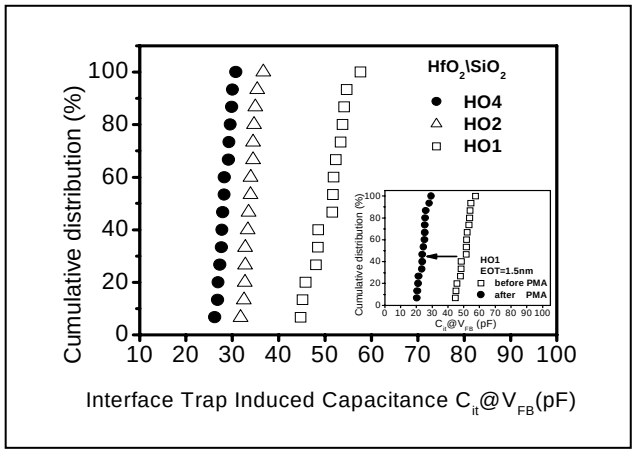
圖十

圖十一為 EOT=1.8 nm 元件之 I-V 崩潰特性圖，可看出崩潰電場達 12 MV/cm 以上。



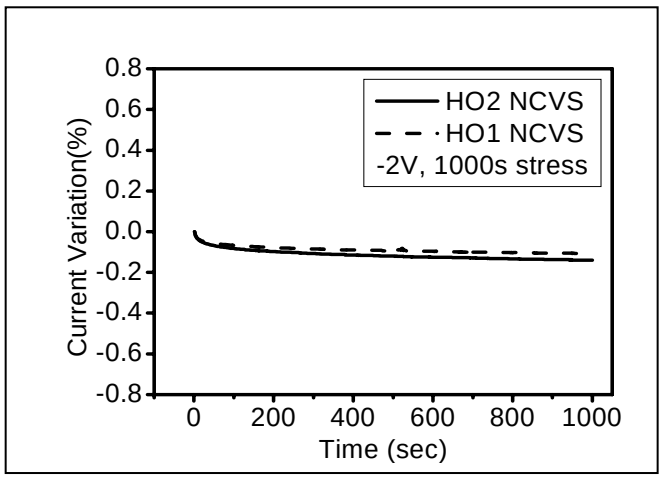
圖十一

圖十二為於平能帶處之界面陷阱密度值統計分布，可看出退火處理溫度愈高(HO4)其 D_{it} 值較小，而金屬後之溫處理可進一步再減少 D_{it}。

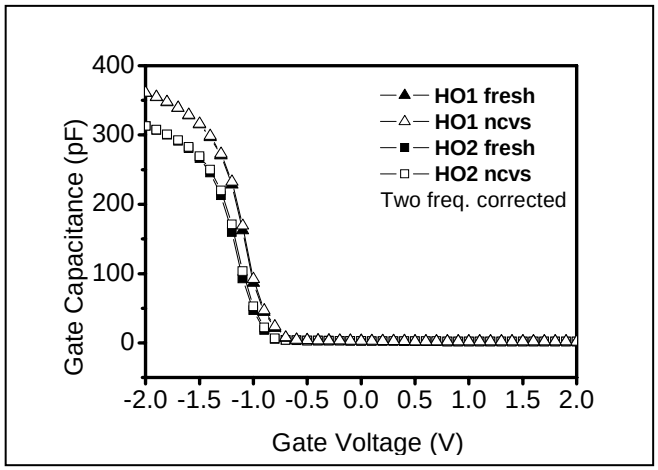


圖十二

圖十三為元件於 -2V 下 1000 sec 之電流變化特性，略呈現電子抓陷行為，但 C-V 特性變化甚小，如圖十四所示。

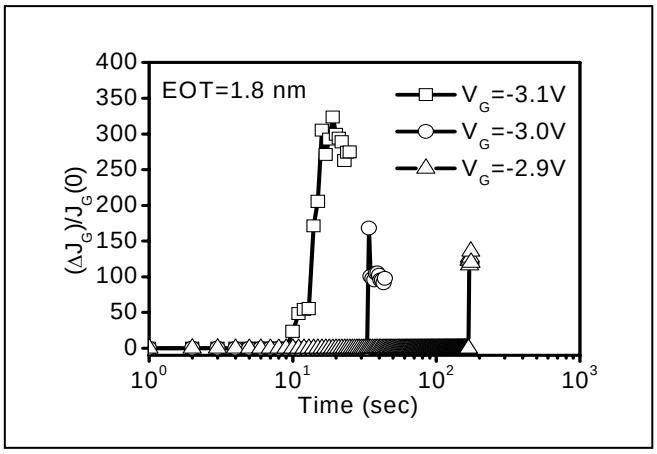


圖十三

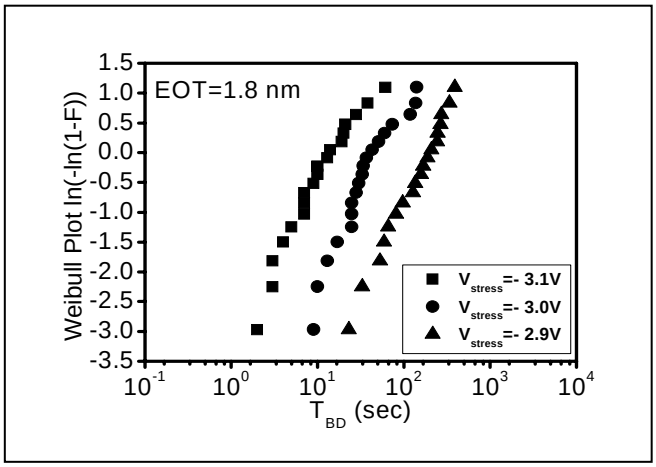


圖十四

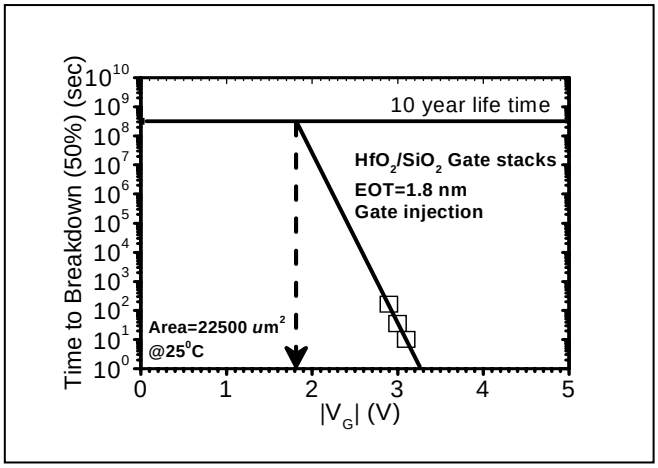
圖十五為 EOT=1.8 nm 元件於不同偏壓下之電流變化特性，可看出電壓愈大，愈早崩潰，其 t_{BD} Weibull Plot 圖如圖十六所示，而於 1.8V 下預測可達 10 年之壽命，如圖十七所示，絕緣層之可靠度表現佳。



圖十五



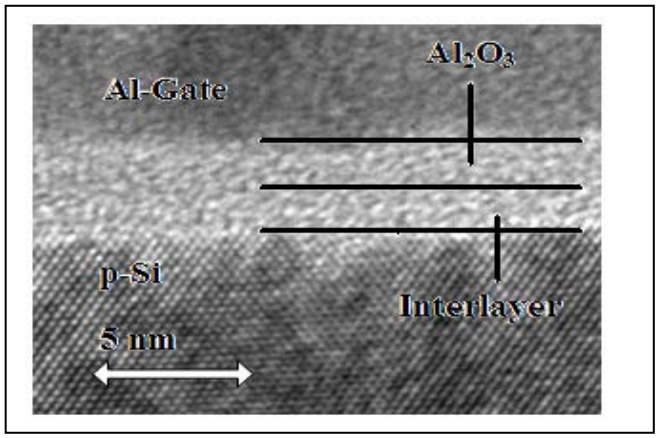
圖十六



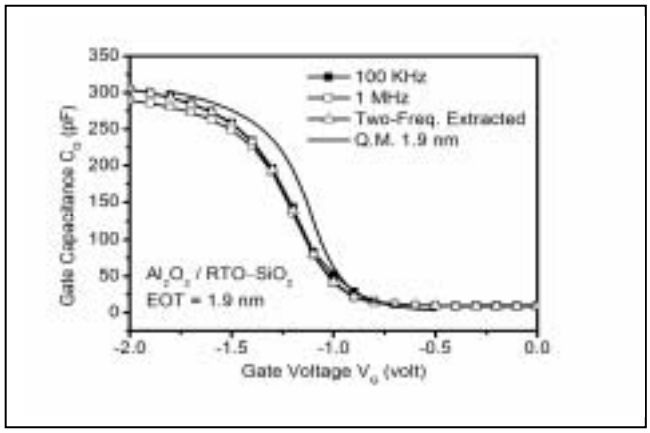
圖十七

(C). 以硝酸氧化 Al 金屬備製 Al_2O_3/SiO_2 金氧半元件結構

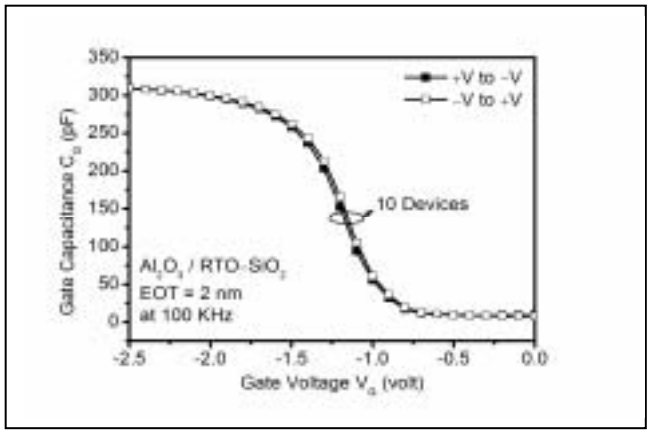
圖十八為先生長 SiO_2 再沉積 Al 後，以 HNO3 氧化成 Al_2O_3，經 650°C 之溫度處理所得的元件 TEM 圖，可看出兩層之堆疊。圖十九為 EOT=1.9 nm 元件之 C-V 圖，圖二十為其來回掃描之 C-V 圖，可看出絕緣層之界面特性良好。



圖十八

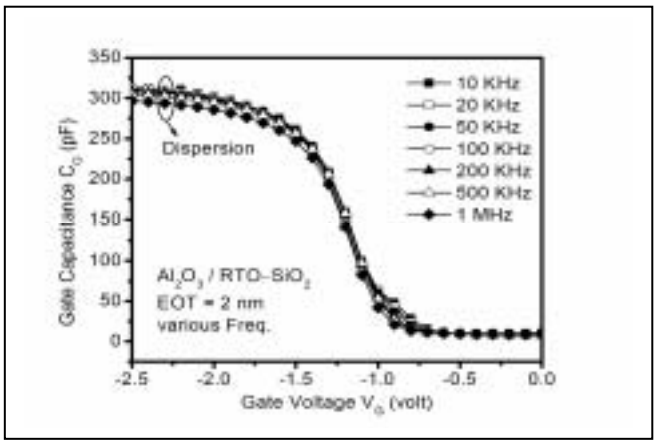


圖十九

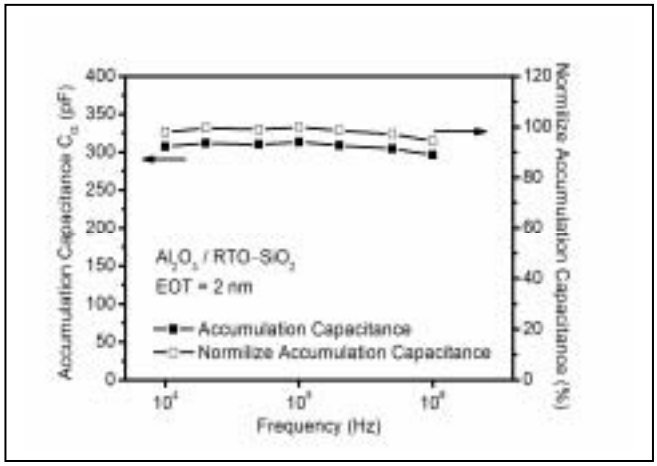


圖二十

圖二十一為於 10K~1MHz 範圍之 C-V 特性，可看出頻率變化影響甚小，如圖二十二所示，同時可看出 C-V 之遲滯現象可忽略，

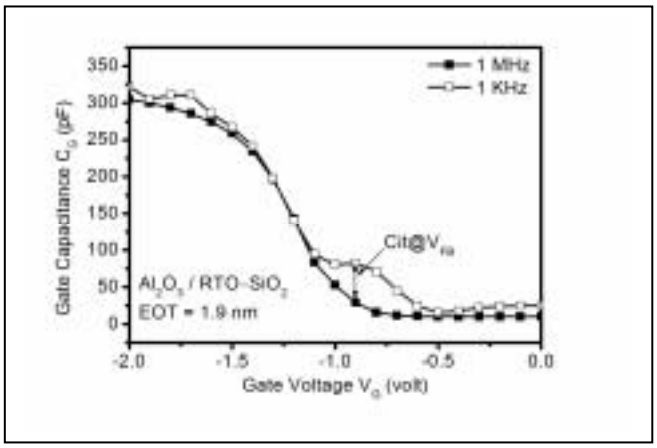


圖二十一



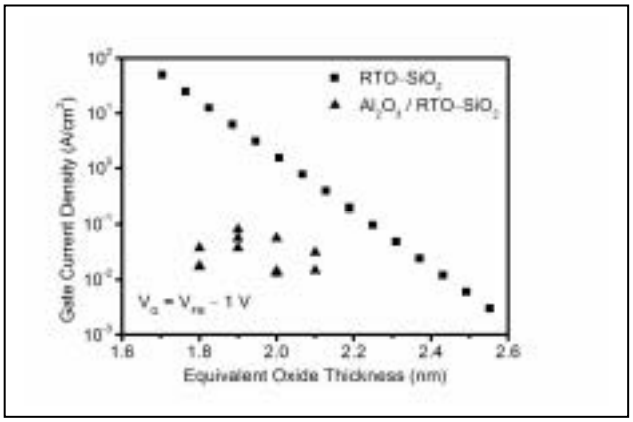
圖二十二

圖二十三為 EOT=1.9 nm 元件於 1MHz 與 1KHz 之 C-V 特性，於平能帶處利用電容所擷取之界面陷阱密度 D_{it} 約為 1.25×10^{12} $cm^{-2}ev^{-1}$。



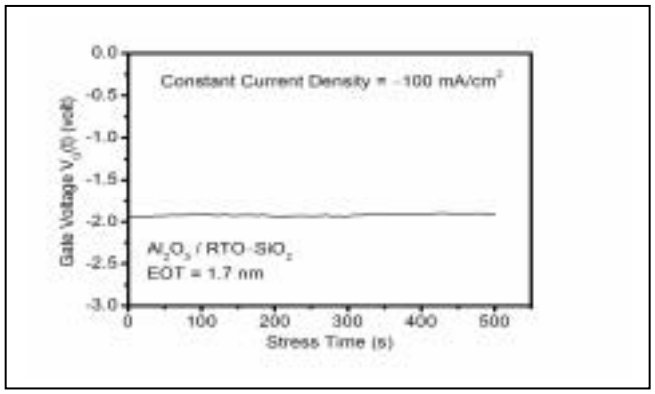
圖二十三

圖二十四為 $V_G=V_{FB}$-1V 下電流與 EOT 之關係圖，可看出高介電常數絕緣層特性呈現，比 RTO-SiO_2 之電流為小。

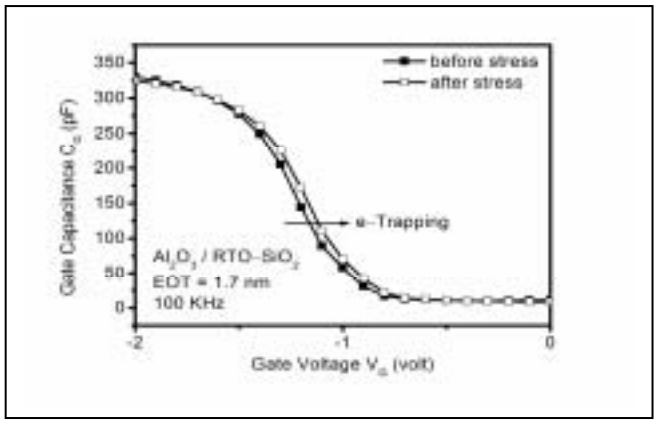


圖二十四

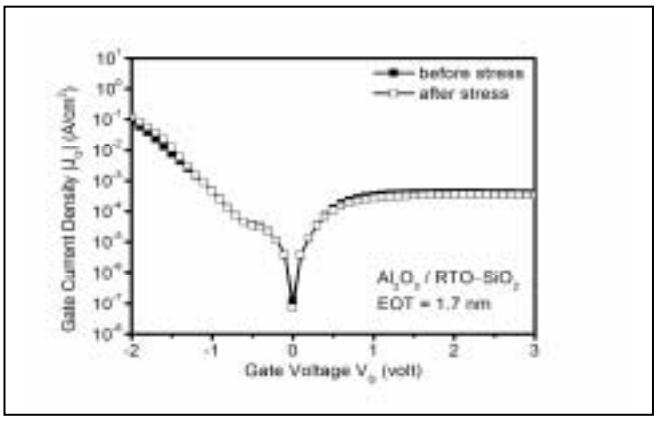
圖二十五為 EOT=1.7 nm 元件於 100 mA/cm^2 定電流下之電壓變化情形，由圖二十六之 C-V 特性可看出經 100mA/cm^2 定電流 500 sec 施壓後，平能帶電壓移為 46 mV 之電子抓陷，施壓前後之元件電流特性變化不大，如圖二十七所示，本技術為低成本發展潛力大之高介電常數絕緣層製程。



圖二十五



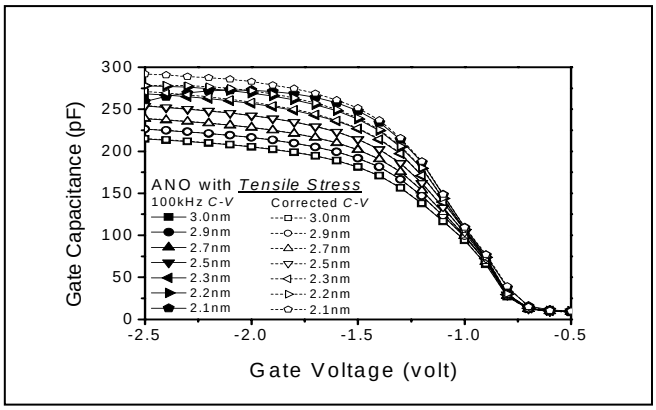
圖二十六



圖二十七

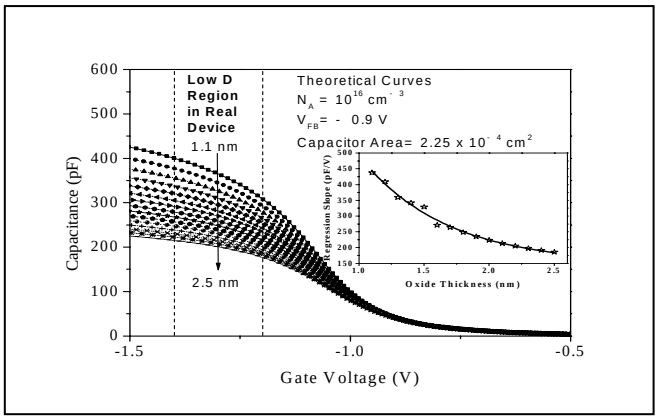
(D). 利用低功率散逸因素區域之電容特性擷取超薄氧化層厚度技術研發

圖二十八為超薄氧化層 MOS 元件於不同氧化層厚度下之 C-V 特性，可看出在較薄時於聚集區之漏電嚴重，會影響 C-V 之準確性，要從該區擷取厚度需另外修正處理。



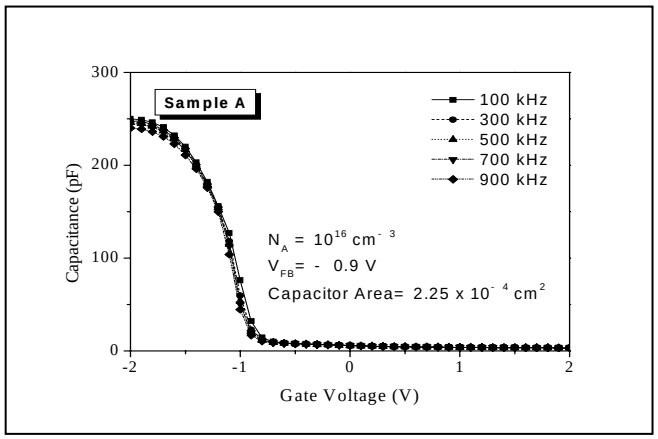
圖二十八

圖二十九為理論之不同厚度 C-V 特性，在所標示之區域內，觀察到電容值對電壓之斜率會隨厚度而敏感變化，該區域為可能之最低功率散逸區。

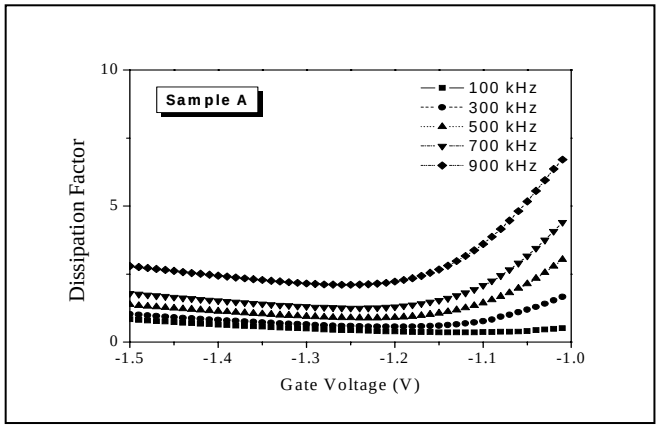


圖二十九

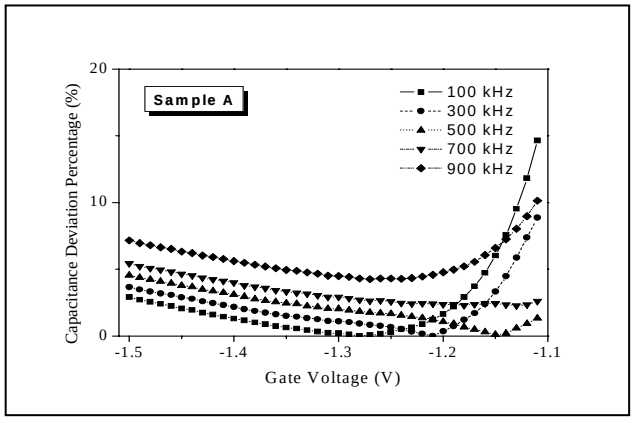
圖三十為一厚度為 2.0 nm 之元件 C-V 特性，其厚度可用傳統之雙頻率修正法得知。利用上述原理，測量其 D 值分布如圖三十一所示，發現在-1.1V 至-1.4V 範圍之 D 值出現較低值，經由理論電容值與實驗電容值之比較，可得到圖三十二之分布圖，明顯看出在-1.1V 至-1.4V 範圍之實驗電容值接近理論電容值。



圖三十

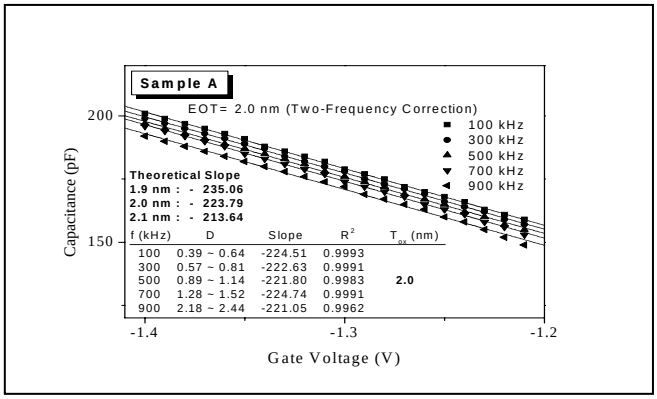


圖三十一



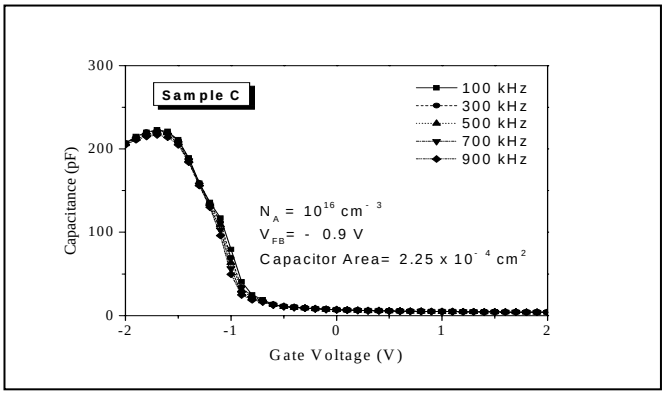
圖三十二

圖三十三為在-1.1V 至-1.4V 範圍之電容分布放大圖，可得知其斜率約為-221~-224 pF/V，與圖二十九之內插理論對照後可得 2.0 nm 之厚度，該值與採用傳統雙頻率修正法得到的值一樣，表示本方法之可信度佳。

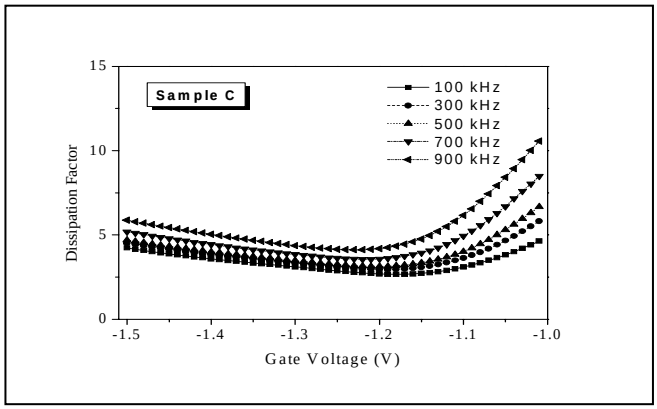


圖三十三

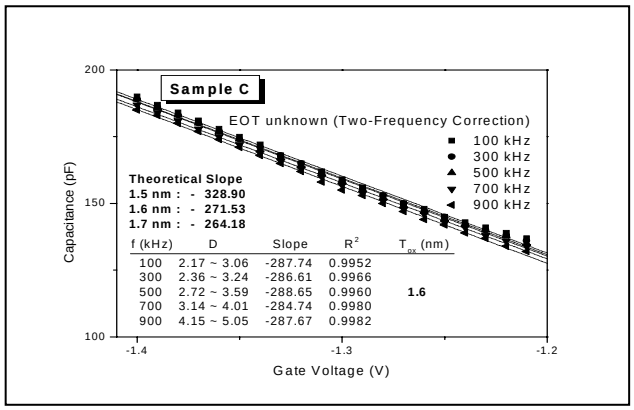
圖三十四為一厚度更薄之元件，因為漏流嚴重，C-V 曲線變形嚴重，此元件無法採用傳統之雙頻率修正法得到正確厚度。接著採用本研究提出之方法，先量取 D 值分布如圖三十五所示，然後在最低 D 值區-1.2V 至-1.4V 範圍分析其斜率，再與圖二十九之內插理論圖分析比較，可快速判斷出其厚度為 1.6 nm，相當實用。



圖三十四



圖三十五



圖三十六

四、總結與討論

在第三年度之研究中，發現了將 SiC 直接置於純水中陽極氧化處理，即可快速得到氧化層，經高溫短時間退火後，証實氧化層品質佳，與傳統高溫製程之品質相當。對於高介電常數絕緣層製程，利用本單位提出之 HNO_3 氧化金屬法，可得到品質甚佳之 HfO_2/SiO_2 及 Al_2O_3/SiO_2 堆疊結構，成本低且特性佳，具參考性。在超薄氧化層厚度量測技術開發上，提出利用低功率散逸因素區之電容值來取斜率，可快速得知厚度，相關理論及適用範圍具研究空間，值得注意。整體而言，本計畫之執行已產出多樣的技術及學術論文，對現今業界及學術界提供參考，所培養之碩博士生對國家相信有其貢獻。相關重要之研究仍持續進行中，而成果也會陸續整理發表，主持人在執行國科會研究計畫由 2004 年至今所產出之研究成果表列如下，僅此提供參考。

五、主持人近三年半(2004~至今)之研究成果：

(A) Refereed Paper

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7. Y.P. Lin and J.G.Hwu, 2004, **"**Suboxide Characteristics in Ultrathin Oxides Grown under Novel Oxidation Processes", *Journal of Vacuum Science and Technology A*, Nov/Dec, PP.2265-2272.
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11. C.H.Chang, T.M. Wang, and J.G.Hwu*, 2006, "Quality Improvement and Electrical characteristics of High-k Films after Receiving Direct Superimposed with Alternative Current Anodic Oxidation (DAC-ANO) Compensation", *Electrochemical Society Transactions - Physics and Technology of High-k Gate Dielectric III*, Volume 1, Issue 5, PP. 465-475. (EI)
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13. C.J.Hung and J.G.Hwu*, 2006, "Enhancement in Ultra-thin Oxide Growth by Thermal Induced Tensile Stress", *IEEE Transactions on Device and Material Reliability*, Vol.6, No.1, PP.28-32. (SCI/EI)
14. S.W.Huang and J.G.Hwu*, 2006, "Lateral Nonuniformity of Effective Oxide Charges in MOS Capacitors with Al_2O_3 Gate Dielectrics", *IEEE Transactions on Electron Devices*, Vol.53, No.7, July, PP.1608-1614. (SCI/EI)
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China, Vol. B & C, PP.112-113.

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可供推廣之研發成果資料表(一)

■ 可申請專利　■ 可技術移轉　日期：96 年 7 月 31 日

國科會補助計畫	計畫名稱：矽金氧半超薄閘極絕緣層製程研發及新型元件應用(3/3) 計畫主持人：胡 振 國 計畫編號：NSC95-2221-E-002-375　學門領域：微電子
技術/創作名稱	於碳化矽基板上形成絕緣層之方法、碳化矽電晶體及其製造方法
發明人/創作人	胡振國 莊凱傑
技術說明	中文： 提出之陽極氧化生長處理，可使 SiC 基板上快速生長得到絕緣層，因實施容易，速度快，甚具應用性。
	英文： Novel technology of using anodization in D.I. water was proposed to oxidize the SiC substrate. Oxides are rapidly grown on SiC within few minutes. It is of practice for the preparation of insulators on SiC.
可利用之產業及可開發之產品	1. 先進高功率 SiC 元件閘極氧化層
技術特點	1. 低成本 2. 氧化層可經本研究方法快速生長得到 3. 具低熱預算開發潛力 4. 低溫處理不易引起雜質重分布
推廣及運用的價值	1. 現今高品質閘極氧化層之選定仍以高溫熱生長 SiO_2 為主，若能引用本低溫短時間製程，可取得先機，商機無限。 2. 研發成本低，相對風險低，值得投入開發。

出席國際學術會議心得報告

計畫編號	**NSC95-2221-E-002-375**
計畫名稱	**矽金氧半超薄閘極絕緣層製程研發及新型元件應用(3/3)**
出國人員姓名 服務機關及職稱	*張嘉華 台灣大學電子工程研究所 博士班學生 **莊凱傑 台灣大學電子工程研究所 博士班學生
會議時間地點	2007.9.18~2007.9.21 日本茨城縣築波國際會議中心
會議名稱	2007 International Conference on Solid State Devices and Materials (2007 SSDM)
發表論文題目	*Low Temperature Ultra-thin Hafnium Oxide Dielectrics by Sputtering of Hf Metal on Tilted Substrate Followed by Nitric Acid Oxidation then Anodization Compensation in D. I. Water **Silicon Oxide Gate Dielectric on N-type 4H-SiC Prepared by Low Thermal Budget Anodization Method

一、參加會議經過

2007 年國際固態元件與材料會議(International Conference On Solid State Devices and Materials，SSDM 2007)，是由日本應用物理學協會 (Japan Society of Applied Physics) 發起且由IEEE電子元件協會 (IEEE Electron Devices Society) 共同贊助主辦之一年一次之國際性會議，為固態元件材料領域相當重要之大型國際會議。在今年2007年9月18~21日於日本築波國際會議中心舉行，自1969首次舉辦至今，已有38年的歷史。本次研討會的第一天(9/18)為短期課程(short course)，主題為探討莫爾定律達到極限後，電子元件如何繼續演進，及高速CMOS技術的發展。第二天開始為各主題的論文發表以及海報張貼，本次會議共分13 個主題發表，會議共分為十一間會議室(Room A ~ Room K),依不同的主題分類,可選取與個人研究領域相關的主題參與會議。

1.學生張嘉華於本次會議中發表的排程如下

2007/09/20

Room 202 (B) Area 8 Advanced Material Synthesis and Crystal Growth Technology

2.學生莊凱傑於本次會議中發表的排程如下

2007/09/20

Room 303 (G) Area 6 Compound Semiconductor Circuits, Electron Devices and Device Physics

會議發表時間為12分鐘口頭報告，三分鐘由聽眾或會議主持人提問。學生在本次會議發表後，均有國際學者提問及給予建議，受惠良多。

二、與會心得

2007 International Conference on Solid State Devices and Materials (SSDM) 是每年都會在日本舉辦的會議，主要的方向為固態物理元件及材料，藉著會議期間的口頭報告及海報展示相互的討論，可得知目前世界上研究發展的趨勢，同時令學生印象深刻的是國外學者對做學問的態度，在台下詰問發表者時看似挑剔，在發表結束時卻又遞上名片表現出對此研究的高度興趣，並且願意用更多的資源來幫助你，這對研究者著實是一大鼓勵。各界的批評與考驗，確實的讓參與者了解自己論文的內容，充滿自信的言語，這些對我做學問的態度幫助很多，更希望能將他們的研究方法與精神帶回。很榮幸能參加這次的會議，讓我增廣見聞許多。以下為學生張嘉華及莊凱傑參與本次會議的照片紀錄。

三、建議

感謝國科會及學校的補助使得學生們能有機會可以到國外參加大型國際會議，並發表我們的研究成果，與國外學者交流。藉由本次到日本的機會，學生能有機會見到日本的研究型城市-筑波市。筑波市為日本對研究學園城市的特殊規劃，藉由此研究機關的建設，使得日本在研究計劃的開發以及民間研究機關等的招攬有極大的貢獻，筑波市並有一重要的交通運輸建設(筑波特快:Tsukuba Express)，可快速連接東京都與筑波間的交通(東京秋葉原-筑波市:45 minutes)，可加快大城市與科技城的交流。此一經驗可以提供我國做一重要的參考，希望藉此可以提供國內發展科技城市之經驗，有效的整合學術界與產業界，期望加速我國科技的進步。

四 攜回資料

1. 會議光碟片，光碟片中收錄所有與會者之研究論文
2. 會議紙本論文集。
3. 本次會議議程紙本資訊。