The Improved Stability of Deuterated Amorphous Silicon Thin Film Transistor

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Abstract

In order to reduce the bias-induced degradation in hydrogenated amorphous silicon thin film transistor (a-Si:H TFT), a deuterated amorphous silicon layer prepared by deuterium plasma treatment is used as the active layer. It is demonstrated that the stability, i.e., the shifts of threshold voltage and subthreshold swing, of deuterated amorphous silicon thin film transistor can be indeed improved as compared to the hydrogenated ones. This result is consistent with the improvement of the light-induced degradation in deuterated amorphous silicon film and this improvement can be explained by the efficient coupling between Si-D wagging mode and amorphous silicon phonon mode.

I. Introduction

Hydrogenated amorphous silicon thin film transistor (a-Si:H TFT) has wide used in many different areas [1], and the most important application is the active-matrix liquid crystal display (AMLCD) However, the instability of a-Si:H TFTs is the long-lasting problem constraining its usability. This instability comes from two sources: one is the charge trapping inside the insulating layer, i.e., silicon nitride a-SiN_x:H [2]; the other is the creation of metastable defects, i.e., silicon dangling bonds, in the a-Si:H which increase the interface states at the a-Si:H/insulator interface. Therefore, it seem quite straight forward to improve the TFT stability in two ways: first, optimizing the silicon nitride quality in order to reduce the trapped charge effect; second, improving the a-Si:H structure to reduce the creation rate of Si metastable defects under bias. The creation of metastable defect in a-Si:H was known for a long time. In 1977, it was first observed that the extended illumination of a-Si:H with visible light produced a decrease in photoconductivity (the Staebler-Wronski effect) [3]. This degradation becomes one of the most important topics in the studies of a-Si:H material and it is found the degradation is due to the increase of the metastable defects in the films. It is also found that the metastable defects can be created by the charge injection (forward bias) or temperature stress [4, 5]. Therefore, if we can find a method to reduce the degradation of the a-Si:H under illumination, the degradation of a-Si:H TFT under bias may also be slowed down.

In 1995, the hot electron degradation in Si metal oxide semiconductor transistor (MOSFET) has been found to be greatly reduced by passivating the Si/SiO_2 interface with deuterium instead of hydrogen [6]. In 1997, Sugiyama *et al.* [7] have demonstrated that an a-Si:D solar cell is more stable than an a-Si:H cell under normal operation and our group has also demonstrated that an a-Si:D film is more stable than an a-Si:H film under illumination and proposes a possible model to explain this improvement [8]. Since the creation mechanism of metastable states in the channel region of a-Si:H or a-Si:D TFTs by the hot electrons is similar to the creation of metastable states in the a-Si:H(D) films by illumination. It is expected that the a-Si:D TFT may also exhibit the lower creation rate of metastable states in the channel and the device degradation could be improved. In this paper, it is demonstrated that the degradation of a-Si:D TFT is indeed improved as compared to the hydrogenated ones.

II Experiments

Figure 1 displays the fabrication processes of the amorphous silicon TFTs. The substrate used is Corning 7059 glass. First, the 80 nm Cr was evaporated on the glass substrate and the 50 nm thick n^+ a-Si:H was deposited on the Cr as shown in Fig. 1(a). After deposition, the n^+ a-Si:H was etching by reactive ion etching (RIE) and Cr metal was patterned by wet etching to form the contact pad of the TFTs as shown in Fig. 1(b). Before removing the photoresist (PR) on the n^+ a-Si:H, a liquid phase deposited silicon dioxide (LPD-SiO_2) was grown to planarize the surface [9]. The preparation procedures of LPD-SiO_2 solution are described elsewhere [9]. The samples were immersed in the growth solution to grow the SiO_2 until the step between n^+ a-Si:H and glass substrate is filled up as shown in Fig. 1(c). A 100 nm a-Si:H was deposited after removing the PR as shown in Fig. 1(d). This a-Si:H is used as the active layer in the TFTs. Then the D_2 or H_2 plasma treatment processes were used to treat the a-Si:H

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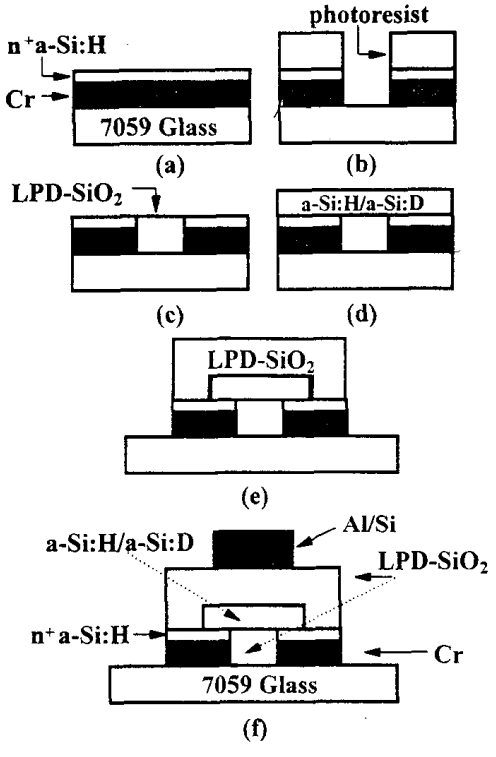

Figure 1 The flow chart of the TFT fabrication processes.

layers. The procedures of plasma treatment processes are as follows: the a-Si:H films were annealed at 550°C in N_2 environment for 5 minutes to expel all the hydrogen atoms out of the films. Then the annealed films were treated separately by H_2 and D_2 plasma until their electrical properties (dark and photoconductivities) were recovered. The plasma treatment conditions are followings: substrate temperature 300°C, chamber pressure 6 torr, gas flow rate 3 sccm, power density 0.1 W/cm^2 and the treatment time 3 hours. Three different active layers were prepared , i. e., the as-deposited a-Si:H, plasma treated (PT) a-Si:H and plasma treated (PT) a-Si:D. Then the active layers were mesa etching by RIE as shown in Fig. 1(e) to reduce the gate leakage current from the gate electrode to the source/drain electrodes. The etching condition are: CF_4 36.5 sccm, O_2 4 sccm, pressure 30 mtorr and the power density 0.4 W/cm^2. After etching, a 200 nm LPD SiO_2 was deposited at 50°C and the gate electrode (Al with 1% Si) was vacuum evaporated and patterned. The final TFT device structure was shown in Fig. 1(f). The current-voltage characteristics of the three types of TFTs were measured, their on/off current ratio, threshold voltage, subthreshold swing, *etc.*, were extracted. Then the TFTs were stressed by varying the gate (V_{gs}) and drain (V_{ds}) bias from 0 to 40 V. The stress time was varied from 500 to 10000 seconds. After stress, the changes of threshold voltage and subthreshold swing of the TFTs were recorded and compared to find out the most stable devices.

III. Results and Discussion

The drain current (I_d) versus drain voltage (V_{ds}) characteristics of as-deposited a-Si:H, PT a-Si:H and PT a-Si:D TFTs are shown in Figs. 2 (a), (b) and (c), respectively. Apparently the a-Si:D TFT exhibits the

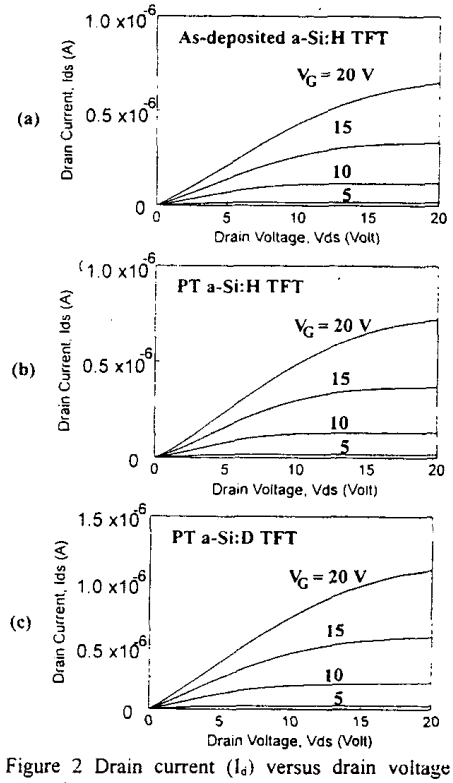

Figure 2 Drain current (I_d) versus drain voltage (V_{ds}) characteristics of (a) as-deposited a-Si:H, (b) PT a-Si:H and (c) PT a-Si:D TFTs before bias stress.

highest drain current at the same gate and drain biases. The relation between square root of I_d and V_{ds} of the same TFT biased in the saturation region ($V_{gs} = V_{ds}$) are shown in Fig. 3 (a). The field effect mobility evaluated from the slope are about 0.13, 0.14 and 0.20 cm^2/V-sec for the as-deposited a-Si:H, PT a-Si:H and PT a-Si:D TFTs, respectively. These are the typical value for TFT with SiO_2 as the gate insulator. The threshold voltage obtained from the intercept of V_{ds} axis is about 5.2, 4.3 and 3.8 V for the as-deposited a-Si:H, PT a-Si:H and PT a-Si:D TFTs, respectively. Because the LPD-SiO_2 is

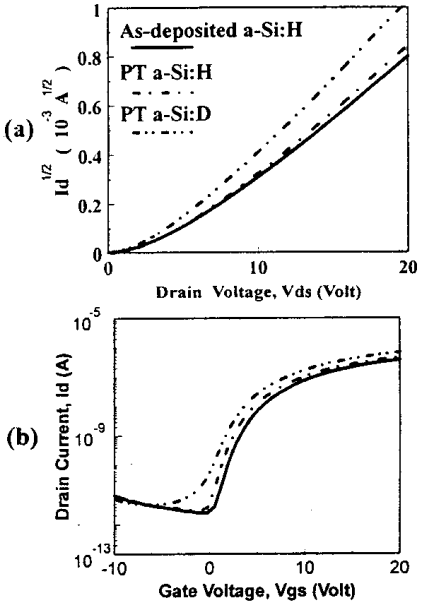

Figure 3 (a) Relation between square root of I_d and gate bias (V_{gs}) and (b) transfer curves of as-deposited a-Si:H, PT a-Si:H and PT a-Si:D TFTs with $V_{ds} = V_{gs}$.

grown near the room temperature (50°C), the defect state density inside the LPD-SiO_2 is larger than that in SiO_2 grown at high temperature. The threshold voltages of three TFTs are thus expected to be slightly higher than the value of normal TFT. Figure 3 (b) shows the transfer curve of above three TFTs with V_{ds} = 10 V, respectively. The on/off current ratio are about 5 order of magnitude and the subthreshold swing are about 1.5 V/decade for the three TFTs. These device parameters demonstrate that they are good quality TFTs with SiO_2 as the gate insulator.

Next, the stabilities of a-Si:H and a-Si:D TFTs were tested under V_{gs} = V_{ds} = 20 V. The stress time varies from t = 500 to 10000 seconds in seven steps. During the bias stress, threshold voltage shift (ΔV_T) and the subthreshold swing shift (ΔS) are extracted from the experiment data.

First, Figs. 4 (a) and (b) replot the threshold voltage and subthreshold swing shift of the as-deposited a-Si:H, PT a-Si:H and PT a-Si:D TFTs after V_{gs} = V_{ds} =20 V

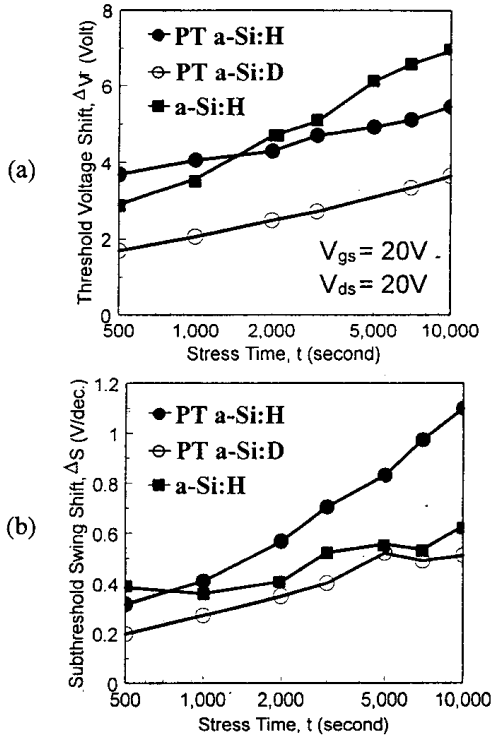

Figure 4 The (a) threshold voltage and (b) subthreshold swing shifts of the as-deposited a-Si:H (■), plasma treated (PT) a-Si:H (●) and a-Si:D (○) TFTs. The stress condition is V_{gs} = 20 V, V_{ds} = 20 V and the stress time varies from t = 500 to 10000 seconds

stress for 500 to 10000 seconds. After 10000 second stress, the threshold voltage shift of the as-deposited

a-Si:H, PT a-Si:H and PT a-Si:D TFTs are 6.94, 5.45 and 3.65 V, respectively. The shift of a-Si:D TFT is the lowest. For the subthreshold swing, the shifts of the as-deposited a-Si:H, PT a-Si:H and PT a-Si:D TFTs are 0.629, 1.10 and 0.512 V/decade. Again, the a-Si:D TFT has the lowest shift.

In a-Si:H(D) TFT, the sources of the threshold voltage shift are the charges trapped inside the gate insulator and the interface states created by increasing the metastable states in the a-Si:H(D) layer [10]. Form experimental results described in above sections, it is found that the a-Si:D TFT has the lowest threshold voltage shift under five different stress conditions. Because the gate insulator (LPD-SiO_2) of three TFTs are the same, their fabrication procedures are also the same. The improved stability of a-Si:D TFT is indeed due to the lower metastable states created in the a-Si:D active layer. After the same stress time (10000 seconds), the a-Si:D TFT also shows the smallest shift in subthreshold swing among three different samples. The shift of subthreshold swing is related to the density of defect states at the insulator /a-Si:H(D) interface by bias stress [18,19]. Therefore, the experimental data indicates that the a-Si:D film is the most stable one under bias stress like the case under light exposure.

V. Conclusions

A good quality a-Si:D TFT using plasma treatment method is demonstrated. The threshold voltage is 3.8 V, the field effect mobility at the saturation region is 0.16 cm^2/V-sec, the on/off current ratio is about 5 order of magnitude and the subthreshold swing is 1.5 V/decade. From the measurement of different stress conditions, it is found that the PT a-Si:D TFT is the most stable one as compared to the as-deposited and PT a-Si:H TFTs. The stability of amorphous silicon TFT can indeed be improved by using deuterium atoms to replace hydrogen atoms. This is consistent with the conclusions of the light-induced degradation in our previous paper [8].

References

1. M. Kinugawa, *Thin Film Transistor Technologies*, p. 145 (1992).
2. M. J. Powell, *IEEE Tran. Electron Devices*, **36**, 2753, (1989).
3. D. L. Staebler and C. R. Wronski, *Appl. Phys. Lett.*, **31**, 291 (1977).
4. M. Stutzmann, W. B. Jackson and C. C. Tsai, *Phys. Rev. B*, **32**, 23 (1985).
5. R. A. Street, *Appl. Phys. Lett.*, **59**, 1084 (1991).
6. J. W. Lyding , K. Hess and I. C. Kiziyalli, *Appl. Phys. Lett.*, **68**, 2526 (1996)
7. S. Sugiyama, Y. Yang and S. Guha, *Appl. Phys. Lett.*, **70**, 378 (1997).
8. J. H. Wei, M. S. Sun and S. C. Lee, *Appl. Phys. Lett.*, **71**, 1498 (1997).
9. J. S. Chou and S. C. Lee, *Appl. Phys. Lett.*, **64**, 1971 (1994).
10. C. van Berkel and M. J. Powell, *Appl. Phys. Lett.*, **51**, 1094 (1987).