行政院國家科學委員會專題研究計畫 成果報告

前瞻智慧型天線系統之關鍵元組件研製
研究成果報告(精簡版)

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計 畫 主 持 人：江簡富

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報 告 附 件 ：出席國際會議研究心得報告及發表論文

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中 華 民 國 96 年 12 月 11 日

行政院國家科學委員會補助專題研究計畫成果報告

前瞻智慧型天線系統之關鍵元組件研製

計畫類別：■ 個別型計畫　　□ 整合型計畫

計畫編號：NSC 95-2221-E-002 -085 -

執行期間：九十五年八月一日至九十六年七月三十一日

計畫主持人：江簡富 教授

共同主持人：

計畫參與人員：張子軒、李宜音、陳純熙、鄧平援、李偉暘、杜博仁、楊善詠、麥肇倫

成果報告類型(依經費核定清單規定繳交)：□精簡報告　■完整報告

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□赴國外出差或研習心得報告一份

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■出席國際學術會議心得報告及發表之論文各一份

□國際合作研究計畫國外研究報告書一份

處理方式：除產學合作研究計畫、提升產業技術及人才培育研究計畫、列管計畫及下列情形者外，得立即公開查詢

■涉及專利或其他智慧財產權，□一年□二年後可公開查詢

執行單位：國立台灣大學電信研究所

中　華　民　國　九　十　六　年　十　月　三　十　日

中文摘要

關鍵詞：介電質共振天線、單極天線、低雜訊放大器、超寬頻、切換電感振盪器、充電時間、液晶螢幕顯示器、驅動電路、場序式。

本計畫研究成果分為六項子題，分別呈現在六篇期刊論文及六件專利申請中，該六項子題分別為：

子題一、寬頻介電質共振-單極天線

子題二、多頻之分離式介電質共振器天線

子題三、低電壓低功率24 GHz CMOS低雜訊放大器

子題四、適用於超寬頻的雙頻切換電感振盪器

子題五、延長充電時間並可精確充電之液晶螢幕驅動電路

子題六、場序式顯示器之設計

英文摘要

Key words: dielectric resonator antenna, monopole antenna, low-noise amplifier, ultra-wideband, switched-inductor oscillator, charging time, liquid crystal display, driver, field sequential color.

The outcome of this project is divided into six subjects, respectively presented in six journal papers and six patents. These six subjects are

Subject 1: Broadband dielectric resonator antenna with metal coating

Subject 2: Dualband split dielectric resonator antenna

Subject 3: A K-band CMOS low-noise amplifier with low dc power consumption

Subject 4: Dual-band VCO with switched inductors for UWB applications

Subject 5: Active and adaptive charging method on data lines for delay compensation

Subject 6: Design constraints on FSC LCD

可供推廣之研發成果資料表

■ 可申請專利　■ 可技術移轉　日期：96 年 10 月 30 日

國科會補助計畫	計畫名稱：前瞻智慧型天線系統之關鍵元組件研製 計畫主持人：江簡富 教授 計畫編號：NSC 95-2221-E-002 -085 – 學門領域：電信學門
技術/創作名稱	寬頻介電質共振-單極天線
發明人/創作人	張子軒、江簡富
技術說明	中文： 本發明結合介電質共振天線(DRA)與單極天線(monopole)達到 49%寬頻效果。不僅體積小、構造簡單、製作容易，且利用共面波導(CPW)饋入，易與其他平面電路整合。在頻帶內的輻射場型皆為全方位性。
	英文： In this invention, DR antenna is integrated with monopole antenna to achieve a broadband of 49% bandwidth. This proposed DR-monopole antenna has many advantages such as small volume, simple structure and ease of fabrication. The antenna is fed by coplanar waveguide, which can be easily integrated with other planar circuits. The radiation pattern is omnidirectional over the bandwidth.
可利用之產業及可開發之產品	WLAN 802.11a 網路相關產品。
技術特點	新穎性：本發明結合介電質共振天線與單極天線，具有良好的線性極化、場型為全方向性、體積小且可達到 49%的頻寬。結構簡單容易實作、利用共面波導結構饋入，易於和其他平面元件整合。 進步性：在 WLAN 802.11a 的應用中，接入點(access point)和個人電腦收發機(transceiver)的相對位置會隨著使用者移動而改變，為了使用上的方便，天線場型必須為全方向性。本發明不僅天線體積小，製作簡單、成本低廉，具有全方向性場型的優點，符合 WLAN 802.11a 無線網路應用。
推廣及運用的價值	產業上利用性：電腦無線網路日益普及，傳輸速度快，廣為大眾所接受。本發明將單極天線與介電質共振天線的頻帶相連結，並設計共面波導饋入系統整合兩天線以達到 49%的寬頻。

可供推廣之研發成果資料表

■ 可申請專利　■ 可技術移轉　日期：96 年 10 月 30 日

國科會補助計畫	計畫名稱：前瞻智慧型天線系統之關鍵元組件研製 計畫主持人：江簡富 教授 計畫編號：NSC 95-2221-E-002 -085 – 學門領域：電信學門
技術/創作名稱	多頻之分離式介電質共振器天線
發明人/創作人	張子軒、江簡富
技術說明	中文：本發明在一矩形介電質共振器中嵌入一狹縫與四個凹口，獲得雙頻的特性，並增加頻寬。該狹縫將本體從中分成兩個相同之部份，每一部份各嵌入兩個凹口，利用微帶線當作訊號線，透過耦合槽縫饋入天線。本發明易與其他平面電路整合，並減少其他元件對天線的干擾。
	英文：In this invention, the resonant frequencies of a DR antenna is tuned by embedded a split and four notches, and the bandwidth is increase. The split separates the dielectric resonator into two identical parts, with two notches in each part. A microstrip line is used to feed this antenna via a coupling aperture. This invention is easy to integrate with other planar circuits, and can minimize interference from other components.
可利用之產業及可開發之產品	WiMAX、WLAN 802.11a 網路相關產品。
技術特點	新穎性：本發明係在介質共振器天線中嵌入凹口與狹縫，調整 TE^{y}_{111}、TE^{y}_{112}、TE^{y}_{113} 之共振頻率，以移動頻帶至所需的應用。在狹縫與凹口處的電場會被增強，使能量能更有效率地輻射，降低天線品質因子，增加頻寬。利用微帶線透過槽縫耦合至天線，易於和其他平面元件整合。 進步性：本發明具有寬波束的垂直極化輻射場型，可用於 WiMAX 與 WLAN 無線網路應用。
推廣及運用的價值	產業上利用性：無線網路日益普及，傳輸速度快，廣為大眾所接受。本發明係一多頻介電質共振器天線，該天線的頻寬涵蓋 3.375-3.93 GHz 與 5.08-5.415 GHz，滿足 WiMAX 與 WLAN 之規格，在水平面上，具由寬波束、垂直極化的輻射場型。

可供推廣之研發成果資料表

■ 可申請專利　■ 可技術移轉　日期：96 年 10 月 30 日

國科會補助計畫	計畫名稱：前瞻智慧型天線系統之關鍵元組件研製 計畫主持人：江簡富 教授 計畫編號：NSC 95-2221-E-002 -085 – 學門領域：電信學門
技術/創作名稱	低電壓低功率 24 GHz CMOS 低雜訊放大器
發明人/創作人	鄧平援、江簡富
技術說明	中文：本發明利用 TSMC 0.18 μm CMOS 製程設計一個應用於 24 GHz 短距離雷達感測器系統的低雜訊放大器。主要架構為三級的共源放大器串接，並包含前端輸入級匹配網路、中間級匹配電路以及輸出匹配電路。本發明的功率消耗僅 8.3 mW (1 V supply)，power gain 為 13.5 dB，noise figure 為 4.7 dB，input/output return loss > 10 dB，晶片面積為 0.64 mm x 0.48 mm。 英文：This invention presents a 24 GHz LNA for short-range radar system using TSMC 0.18 um CMOS process. The architecture is a cascade of three stages of common-source amplifiers, accompanied by input, inter-stage, and output matching networks. This invention consumes 8.3 mW under 1 V supply, its power gain is 13.5 dB, noise figure is 4.7 dB, return loss is less then – 10 dB, the chip size is 0.64 mm x 0.48 mm.
可利用之產業及可開發之產品	毫米波低雜訊放大器、短距離雷達感測系統。
技術特點	本發明的特點為：用適當的剪裁技巧來選取電晶體尺寸，使用較小的尺寸來達到阻抗匹配，因此降低功率消耗。本發明的被動元件(如電感)均為 on-chip 的繞線平面式電感，電容為 TSMC 所提供的 MIM 電容。
推廣及運用的價值	產業上利用性：毫米波雷達系統將是汽車防撞系統的重要技術，如何接收並放大訊號，且不額外增加雜訊是一個重要的研究主題。一般熟知的射頻電路多需要特殊製程，如 GaAs HEMT、SiGe HBT，不僅價格昂貴，且無法與數位電路結合，製作 SOC 並不實際。本發明採用低價格的 CMOS 製程，符合產業發展趨勢。

可供推廣之研發成果資料表

■ 可申請專利　■ 可技術移轉　日期：96 年 10 月 30 日

國科會補助計畫	計畫名稱：前瞻智慧型天線系統之關鍵元組件研製 計畫主持人：江簡富 教授 計畫編號：NSC 95-2221-E-002 -085 – 學門領域：電信學門
技術/創作名稱	適用於超寬頻的雙頻切換電感振盪器
發明人/創作人	李偉暘、江簡富
技術說明	中文：本發明使用切換電感當開關切換兩個不同的頻帶，與一般用切換電容當開關不同。不僅構造簡單、相位雜訊低、消耗功率與現有設計互有高低，且能切換兩個頻帶來取代使用兩個 VCO 架構，降低了晶片的面積與成本。
	英文：In this invention, a VCO is implemented with switched inductors to achieve dual-band operation. Compared with VCO using switched capacitors, this proposed VCO has advantages such as simple structure, low power consumption, low phase noise, and is capable of switching two frequency bands to replace two separate VCOs. Hence, its chip size is small and the cost is reduced.
可利用之產業 及 可開發之產品	UWB 無線網路相關產品。
技術特點	新穎性：本發明使用切換電感開關切換兩個不同的頻帶，與一般用切換電容當開關不同，若以電容開關要達到能切換較寬的兩個頻帶，必須加裝較多的切換電容開關，而開關越多所產生的雜訊就越多，而導致相位雜訊過高。 進步性：在 UWB 的應用中，為了使用 OFDM 的傳輸方式，需要產生不同的 LO 訊號，而本發明的 VCO 相位雜訊較低，且能產生雙頻的 LO 訊號，符合 UWB 無線網路應用。
推廣及運用的價值	產業上利用性：本發明利用切換電感來切換兩個頻帶，取代使用兩個 VCO 架構，降低了晶片的面積與生產成本。

可供推廣之研發成果資料表

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國科會補助計畫	計畫名稱：前瞻智慧型天線系統之關鍵元組件研製 計畫主持人：江簡富 教授 計畫編號：NSC 95-2221-E-002 -085 – 學門領域：電信學門
技術/創作名稱	延長充電時間並可精確充電之液晶螢幕驅動電路
發明人/創作人	陳純熙、江簡富
技術說明	中文：大尺寸及高解析度的液晶顯示器是顯示器的發展趨勢，其最需解決的是充電時間不足的問題。本發明利用兩排畫素之間的差值、資料線上的時間常數計算出快速充電所需的電壓。此外，因本發明將三條資料線同時開啟，可減少兩條資料線的延遲時間，大幅提高資料驅動電路可用的充電時間。與傳統的資料驅動電路相比能夠達到快速充電的目的。另外，本發明亦較其他預充電的方法精確。 英文：A fast charging method for large-size or high-resolution liquid crystal display is proposed by comparing data of adjacent rows. The proposed method bundles three rows in one set, and the charging period allocated for these three rows are rearranged to charge all three rows more precisely than conventional methods.
可利用之產業及可開發之產品	液晶顯示器驅動電路相關產品。
技術特點	新穎性：以相鄰畫素的資料以及資料線上的時間常數產生微幅調整所需的電壓，以達到減少充電時間的目的。 進步性：本發明利用重新分配充電時間的方法，在三條掃瞄線為一組之內重新分配各掃瞄線所需的時間延遲，可以大幅提高充電的準確性。
推廣及運用的價值	產業上利用性：適用於大尺寸的液晶螢幕之資料及掃瞄驅動電路。

可供推廣之研發成果資料表

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國科會補助計畫	計畫名稱：前瞻智慧型天線系統之關鍵元組件研製 計畫主持人：江簡富 教授 計畫編號：NSC 95-2221-E-002 -085 – 學門領域：電信學門
技術/創作名稱	場序式顯示器之設計
發明人/創作人	李宜音、江簡富
技術說明	中文：本發明提出場序式顯示器之畫素電路設計法則，滿足充電、電位保持、電容耦合及信號延遲四個限制。利用此方法，可將場序式面板畫素耗電控制為濾光片式面板畫素耗電之 1/6，場序式面板儲存電容所需面積僅為濾光片式面板儲存電容之 30%，場序式面板之開孔率為濾光片式之 1.7-2 倍。
	英文：This invention proposes a methodology to design pixels for field sequential color LCDs, satisfying four constraints on charging, holding, asymmetric kickback and delay. Compared with color filter LCDs, the power consumption can be reduced to 1/6, the storage capacitor can be reduced to 30 %, the aperture ratio can be increased to 1.7-2 folds.
可利用之產業及可開發之產品	液晶顯示器相關產品。
技術特點	本發明以簡易之方法進行場序式顯示器之設計，較傳統的設計能節省約 67%的功率，適合應用在省電式低功率液晶面板。 本發明提出場序式顯示器在充電、電位保持、電容耦合及信號延遲四個限制。
推廣及運用的價值	產業上利用性：本發明可利用同樣解析度同樣尺寸濾光片式顯示器之設計參數，快速換算出場序式顯示器之設計參數。

Broadband Dielectric Resonator Antenna With Metal Coating

Tze-Hsuan Chang, *Student Member, IEEE*, and Jean-Fu Kiang, *Member, IEEE*

***Abstract*—A broadband dielectric resonator (DR) antenna is proposed, which consists of a rectangular DR coated with metal on three sides and placed on a ground plane. The structure is analyzed by modelling the dielectric-air interface as perfect magnetic conductor (PMC). A coplanar waveguide (CPW) with terminating slots is used to feed the antenna. Measurement results exhibit a wide bandwidth of about 47% over which the E_θ pattern on the horizontal plane is nearly omnidirectional. The 10-dB bandwidth of this broadband DR monopole covers 4.2–6.8 GHz. Hence, it can be used for WLAN 802.11a applications.**

***Index Terms*—Dielectric resonator (DR) antenna, monopole antenna.**

I. Introduction

THE prevalence of wireless communication demands broadband antennas which can be embedded within a handset to provide versatile applications. Since it is difficult to obtain wide impedance bandwidth with single resonant antenna, multiple antennas with different operating frequencies have been integrated to satisfy the bandwidth requirement [1], [2].

High-permittivity dielectric material has been used in microwave circuits such as filters or oscillators [3]. In order to facilitate the design of dielectric resonator, a heuristic approach that models the dielectric-air interface as a perfect magnetic wall was proposed to predict the resonant frequencies of cylindrical resonators in 1965 [4]. Since 1983, dielectric resonators have been designed as antenna elements by exciting different modes of DR using conventional feeding mechanisms [5].

A DR antenna exhibits a broader bandwidth if its Q factor is lower. In [6], a notched rectangular DR antenna with a low Q factor is proposed. By lifting a DR above the ground plane, its Q factor can be effectively reduced [7]. The bandwidth of DR can also be increased by modifying its geometry. For example, a truncated tetrahedral DR with its narrow base attached to the ground reaches an impedance bandwidth of 40% [8]. A split conical DR with split side attached to the ground can reach a bandwidth of 50% [9].

High-permittivity material can be used to reduce the size of DR at the expense of bandwidth reduction. However, DRs with larger aspect ratio has been used to reduce the Q factor and hence obtain a wider impedance bandwidth [10], [11].

Multiple DRs with close resonant frequencies can exhibit broadband characteristics by coupling their resonant modes. For example, two cylindrical DRs can be stacked to couple their $\mathrm{HEM}_{11\delta}$ modes [1]. In [2], two rectangular DRs with different sizes are placed at proximity, leaving a slot to couple their TE^{y}_{111} modes.

The bandwidth of DR antenna can also be extended by attaching additional parasitic elements to incur another resonance. In [12], two metal strips are attached to the top of a DR to incur additional resonance close to that of the DR. The inductance of the metal strip and the capacitance between the strip and the ground plane form an LC tank which can be coupled to the DR resonant mode to exhibit a wider bandwidth.

The impedance bandwidth of DR antennas can be further increased by modifying their feeding structures. In [13], a coupling slot is proposed to excite the DR. The resonant modes of slot and DR are coupled to increase the antenna bandwidth.

In [14], a patch resonant mode and a dielectric resonant mode are coupled to increase the DR antenna bandwidth. The signal is fed from the microstrip feed line, through the slot on the ground plane and the slot on the patch, to the DR. In [15], a DR is attached to a circular slot and an eccentric ring slot to achieve a broad bandwidth. A grounded metal plate placed in a plane of symmetry of the electric field distribution can reduce the DR size by half without perturbing the original field distribution. In [16], a rectangular DR integrated with an inverted L-plate antenna is proposed. The DR not only serves as a radiator but also serves as a feeding element for the L-plate.

Typical bandwidth of a rectangular DR antenna is about 6–10%, which can be increased to more than 10% by using lower-permittivity dielectric at the cost of increasing the DR size. Stacking DRs of different sizes or using parasitic DRs can further increase the impedance bandwidth to more than 20% [1], [2]. The former incurs a higher antenna profile, while the latter occupies larger space. Stacking DRs of different permittivities can achieve well coupling to microstrip line and a wider bandwidth of 40% simultaneously. However, the antenna complexity increases. Conical or truncated conical DR can provide more than 50% of impedance bandwidth, but the radiation pattern varies over the band due to the presence of higher-order modes [9].

In this work, a broadband dielectric resonator antenna with a nearly-omnidirectional radiation pattern is proposed. The dielectric resonator is partially coated with metal on its surface, which can be modeled as a cavity having perfect electric conductor (PEC) and perfect magnetic conductor (PMC) walls on

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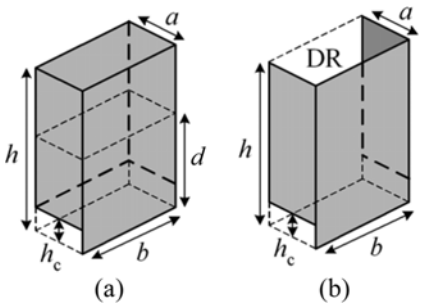

Fig. 1. DR with metal coating on the bottom and on the other: (a) five sides and (b) three sides, gap of height h_c is open near the bottom, metal coating is marked by gray shade.

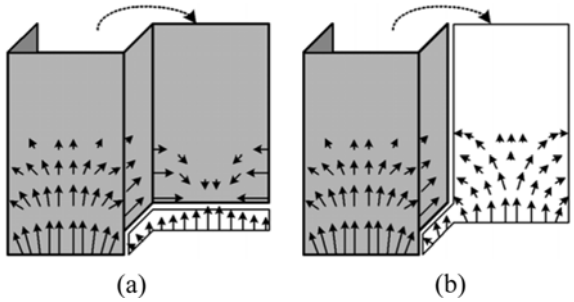

Fig. 2. Current distribution on metal coating (gray surface), and electric field distribution on DR surface (white surface), corresponding to the DR in Figs. 1(a) and (b), respectively.

different portions of the surface. The resonant modes of the DR are investigated. The electric field and the current distributions of these modes are carefully studied to understand their relation to the radiation patterns. The metal coating is also fed as a monopole. The input impedance can be matched by adjusting the DR position and the slot length, and broad bandwidth is achieved by coupling the resonant modes of the metal-coated DR and the monopole.

II. Resonant Modes of Coated DR

Fig. 1(a) shows a rectangular dielectric resonator partially coated with metal, and a small gap of height h_c is open near the bottom of the dielectric resonator. Since the permittivity of the dielectric is much higher than that of the air, the dielectric-air interface can be approximated as a PMC boundary, and the metal coating is treated as a PEC boundary. Hence, the structure is a cavity with PEC and PMC on different portions of the surface, filled with high-permittivity dielectric.

The current and the electric field distributions of the fundamental mode are plotted in Fig. 2(a). The fields and the currents concentrate near the bottom of the dielectric. The electric field across the gap is mainly parallel to the PMC surface. The current flows vertically from the bottom, changes direction on the metal coating, and ends on the opposite side.

The effects of varying parameters are summarized in Table I. It is observed that the resonant frequency is significantly affected by the DR dimensions a and b, and is less affected by the metal height h, since the fields concentrate near the bottom. The effect of decreasing the DR height d while keeping h constant has also been considered. The height d has significant effect on the resonant frequency only when d is comparable to h_c.

TABLE I
Effect of Structure Dimensions on the Resonant Frequency (f_r)

h (mm)	6	8	10	12	14	
f_r (GHz)	6.5	6.49	6.5	6.47	6.49	
b (mm)	3	3.5	4	4.5	5	
f_r (GHz)	7.13	6.83	6.41	6.15	5.79	
a (mm)	1.5	1.7	1.9	2.1	2.3	2.5
f_r (GHz)	7.59	7.13	6.67	6.27	5.87	5.53
d (mm)	1	2	3	4	8	12
f_r (GHz)	8.09	6.7	6.54	6.52	6.46	6.47
h_c (mm)	0.2	0.5	0.8	1.4	1.7	2
f_r (GHz)	5.68	6.09	6.37	6.59	6.75	6.91

Default parameter (mm): $a = 2$, $b = 4$, $d = 12$, $h = 12$, $h_c = 1$, DR is coated on five sides and grounded as in Fig. 1(a).

(a)

$h = d$ (mm)	10	11	12	13	14	
f_r (GHz)	6.05	6.02	6.08	6.04	6.07	
b (mm)	5	5.5	6	6.5	7	
f_r (GHz)	6.07	6.05	6.07	6.05	5.99	
a (mm)	2.5	2.7	2.9	3.1	3.3	3.5
f_r (GHz)	7.14	6.6	6.17	5.84	5.49	5.19
h_c (mm)	0.2	0.5	0.8	1.4	1.7	2
f_r (GHz)	5.68	6.09	6.37	6.59	6.75	6.91

Default parameters (mm): $a = 3$, $b = 6$, $d = h = 12$, $h_c = 1$, DR is coated on three sides and grounded as in Fig. 1(b).

(b)

Fig. 2(a) shows that the current of the fundamental mode on the back coating has strong horizontal component, which generates electric field with horizontal polarization on the xy-plane. Hence, the back coating is removed to reduce the horizontal current, as shown in Fig. 1(b). Fig. 2(b) shows the current and the electric field distributions on the metal coating and the DR surface, respectively. The current distribution is similar to that in Fig. 2(a). The electric field starts from the bottom vertically, gradually decreases and bends to terminate at the metal coating. The effects of varying parameters are also summarized in Table I. Compared to that in Fig. 2(a), the width b now has little effect on the resonant frequency.

III. Monopole Mode of Metal Coating

Place the DR with metal coating as shown in Fig. 1(b) on a ground plane as shown in Fig. 4(a). The metal coating is connected to coplanar waveguide (CPW) signal line to form a monopole antenna, and its resonant frequency is increased as its height is decreased. Fig. 3 shows that the current flows mainly vertically, having a maximum near the ground plane. The current gradually decreases and vanishes at the top. The electric field starts from the ground plane, flows vertically inside the DR, bends and terminates at the coating. Both the current and the electric field have dominant vertical component, which generates strong vertical polarization on the xy-plane. Since the coating width is comparable to its height, the current has a small amount of horizontal component which generates the horizontal polarization on the xy plane.

IV. Antenna Properties

Fig. 4(a) shows the configuration of the proposed DR antenna. The DR with three-side metal coating shown in Fig. 1(b)

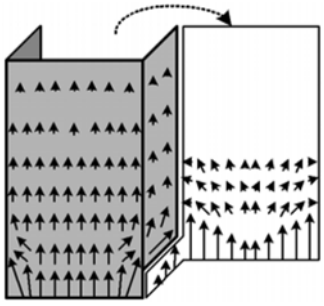

Fig. 3. Current and electric field distributions of the monopole mode on metal coating (gray surface) and DR surface (white surface), respectively.

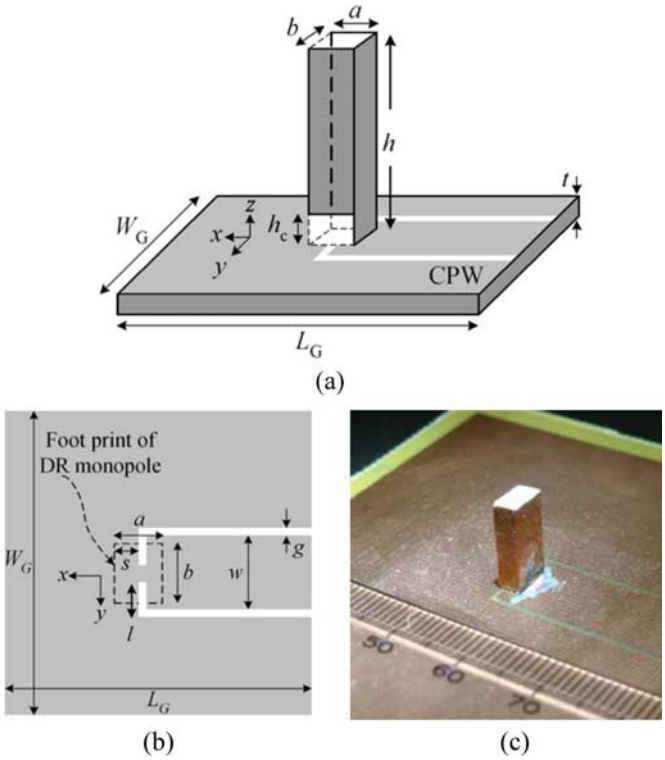

Fig. 4. (a) Configuration of DR-monopole antenna with feeding structure, (b) layout of feeding structure, and (c) photograph.

is placed on the ground plane, the metal coating is connected to the signal line of the CPW to excite the monopole mode, and a pair of open-circuited slots at the end of the CPW are used to excite the DR mode.

Fig. 4(b) shows the layout of the feeding structure, and Fig. 4(c) shows the photograph of the DR-monopole antenna. The DR is placed over the terminating slots of the CPW, and the length of the terminating slots is l. The size of ground plane is $L_G \times W_G$, and the thickness of the substrate is t. The width w and the gap g of the CPW are adjusted to obtain the characteristic impedance of 50 Ω.

By tuning the monopole height and the dimensions of DR, the resonant frequencies of the monopole and the fundamental mode of DR can be moved close to each other. By changing the lengths of the terminating slots l and the offset between the DR and the terminating slots s, good impedance matching can be

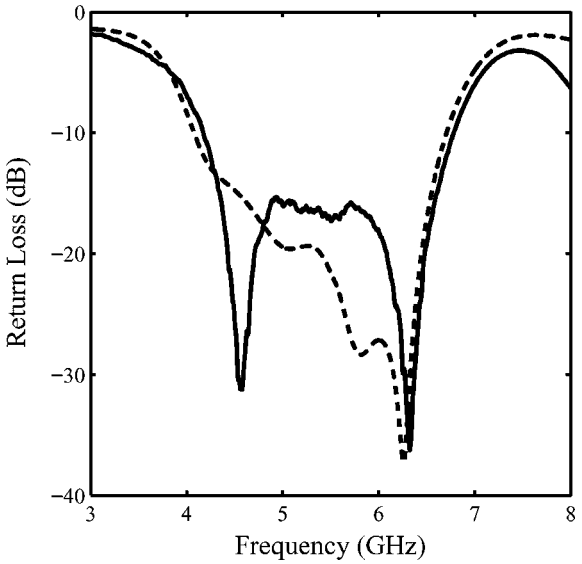

Fig. 5. Return loss of DR-monopole, $a = 3.3$ mm, $b = 5.6$ mm, $h = 12$ mm, $h_c = 0.5$ mm, $g = 0.5$ mm, $w = 10$ mm, $s = 0$ mm, $t = 0.6$ mm, $l = 5.25$ mm, $W_G = L_G = 70$ mm, —: measurement, – – –: simulation.

achieved. The broad impedance bandwidth is achieved by coupling the resonant bands of the monopole and the fundamental mode of DR with metal coating. Fig. 5 shows the return loss of the DR-monopole antenna, the measurement and the simulation results match reasonably well at the band edges. The 10-dB bandwidth is about 47.3% (4.2–6.8 GHz), which is wide enough to cover the IEEE 802.11a applications. Two nulls occurs at 4.56 GHz and 6.32 GHz, which are close to the resonant frequencies of the monopole and the fundamental mode of DR, respectively.

Fig. 6 shows the radiation patterns generated by the DR-monopole with coating on three sides and five sides, respectively. For frequency associated with the monopole mode, the DR-monopole with three-side coating has a more omnidirectional E_θ pattern on the xy-plane than that with five-side coating. The E_ϕ component with three-side coating is lower than that with five-side coating at $\phi = 75°$. For frequency associated with the fundamental mode of DR, the DR-monopole with three-side coating also has a more omnidirectional E_θ pattern on the xy-plane that with five-side coating. Hence, the DR with three-side coating is preferred.

Figs. 7 and 8 show the measurement and simulation radiation patterns at $f = 4.56$ GHz and $f = 6.32$ GHz, respectively. At $f = 4.56$ GHz, the E_θ pattern on the xy-plane is nearly omnidirectional, with the gain of about 1.2 dBi. The horizontal current exists on the side metal coating as shown in Fig. 3 and incurs E_ϕ component with multiple lobes. Hence, the E_ϕ component is only a few dB lower than the E_θ component in some directions. The E_θ pattern on the yz-plane is symmetric, and the maximum gain of 3.2 dBi occurs at $\theta = 44.6°$. The E_θ pattern on the xz-plane is asymmetric, and the maximum gain of 5.2 dBi occurs at $\theta = 33°$.

At $f = 6.32$ GHz, the horizontal current on the side coating as shown in Fig. 2(b) incurs E_ϕ components on the xy-plane with multiple lobes. The E_θ component on the xy-plane is

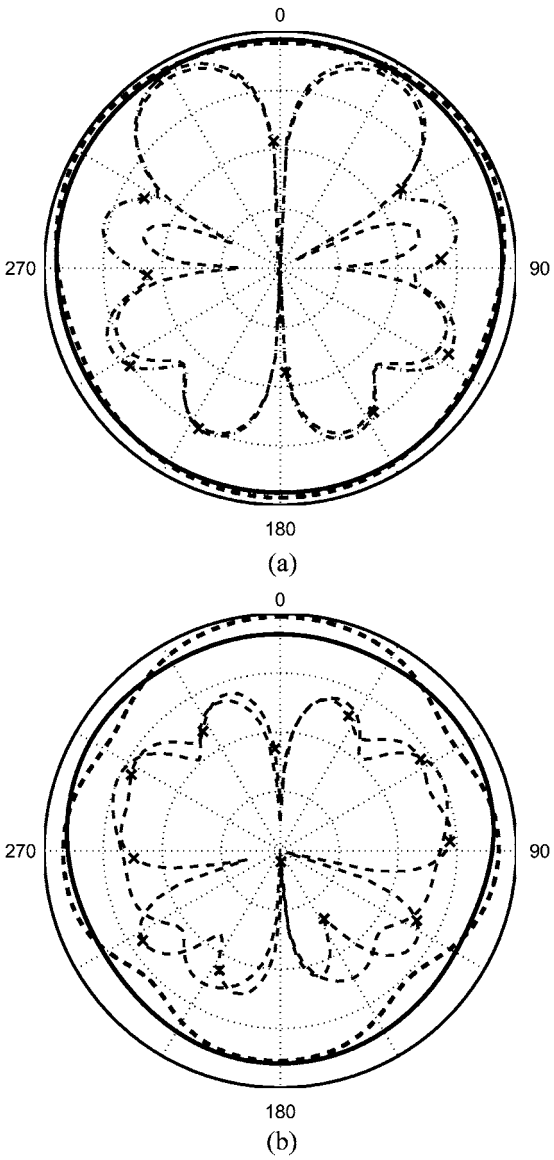

Fig. 6. Comparison of radiation patterns on xy-plane between DR with coating on three sides and five sides: (a) monople mode and (b) fundamental mode of DR, —: E_θ of DR with coating on three sides, - - -: E_θ of DR with coating on five sides, -·-: E_ϕ of DR with coating on three sides, -×-: E_ϕ of DR with coating on five sides, 10-dB per division on radials.

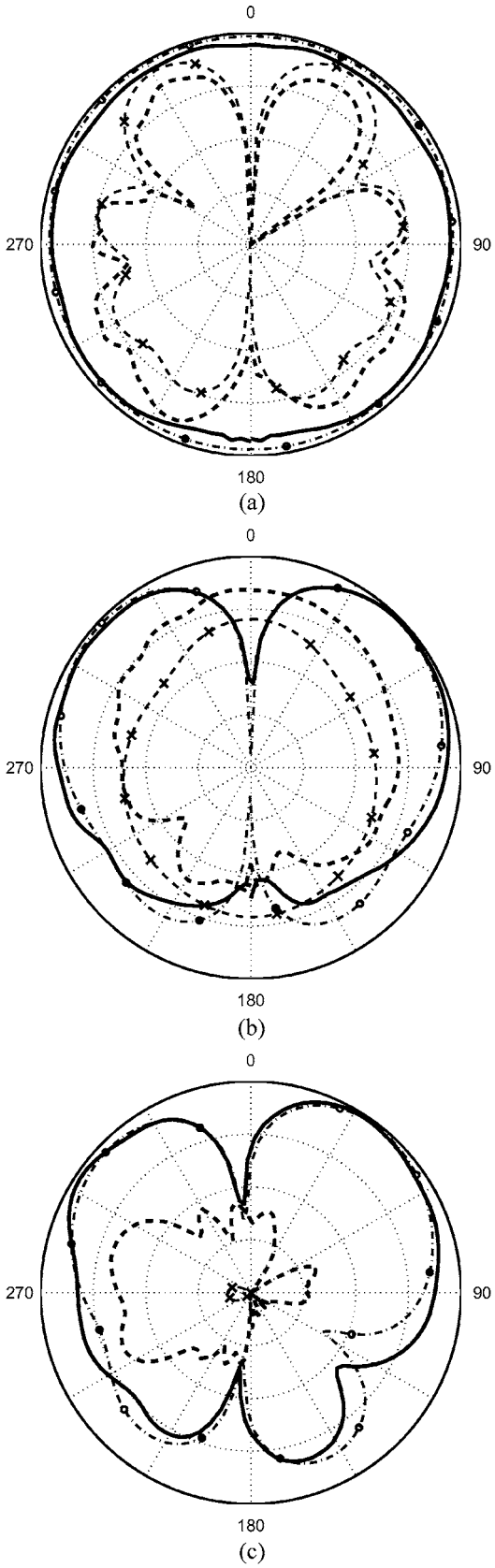

Fig. 7. Radiation patterns at $f = 4.56$ GHz, (a) xy-plane, (b) yz-plane, (c) xz-plane, —: measured E_θ, - - -: measured E_ϕ, -o·: simulated E_θ, · × ·: simulated E_ϕ, 10-dB per division on radials, all parameters are the same as in Fig. 5.

nearly omnidirectional with gain of 1.9 dBi. The E_θ pattern on the yz-plane is symmetric and has a maximum gain of 3.0 dBi at $\theta = 53°$, while that on the xz-plane is asymmetric with the maximum gain of 5.7 dBi at $\theta = 50°$.

The maximum of E_θ component on the xz- and the yz-planes is tilted from $\theta = 90°$ due to the finite size of ground plane. Hence, the antenna gain of vertical polarization is less than 2 dBi on the xy-plane. For WLAN applications, for example, this DR antenna can be placed on a desk with the z-axis pointing to zenith, providing a nearly omnidirectional radiation pattern with vertical polarization on the horizontal plane (xy-plane).

Fig. 9(a) shows the effect of antenna height h on the resonant frequency. When $h = 10$ mm, the resonant modes of the monopole and the DR are strongly coupled. As h is increased to 11 mm, the coupled band is split into two resonant bands. When h is further increased, the first resonant frequency gradually decreases, and a third null appears between the two nulls associ-

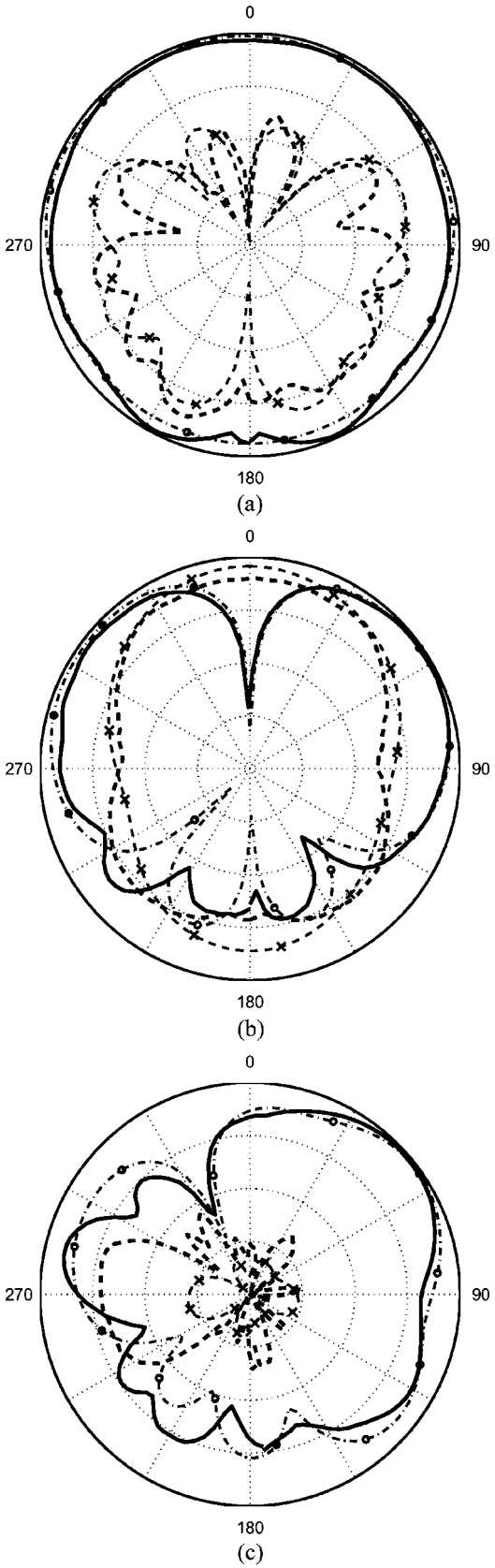

Fig. 8. Radiation patterns at $f = 6.32$ GHz, (a) xy-plane, (b) yz-plane, (c) xz-plane, —: measured E_θ, − − −: measured E_ϕ, −o·: simulated E_θ, · × ·: simulated E_ϕ, 10-dB per division on radials, all parameters are the same as in Fig. 5.

ated with the monopole mode and the DR mode, respectively. Fig. 10 shows the current distribution and the electric field distribution at $f = 5.5$ GHz, associated with the curve shown in Fig. 9(a) with $h = 13$ mm. The current distribution is similar to that of the DR mode near the bottom and similar to that of the monopole mode around the upper portion.

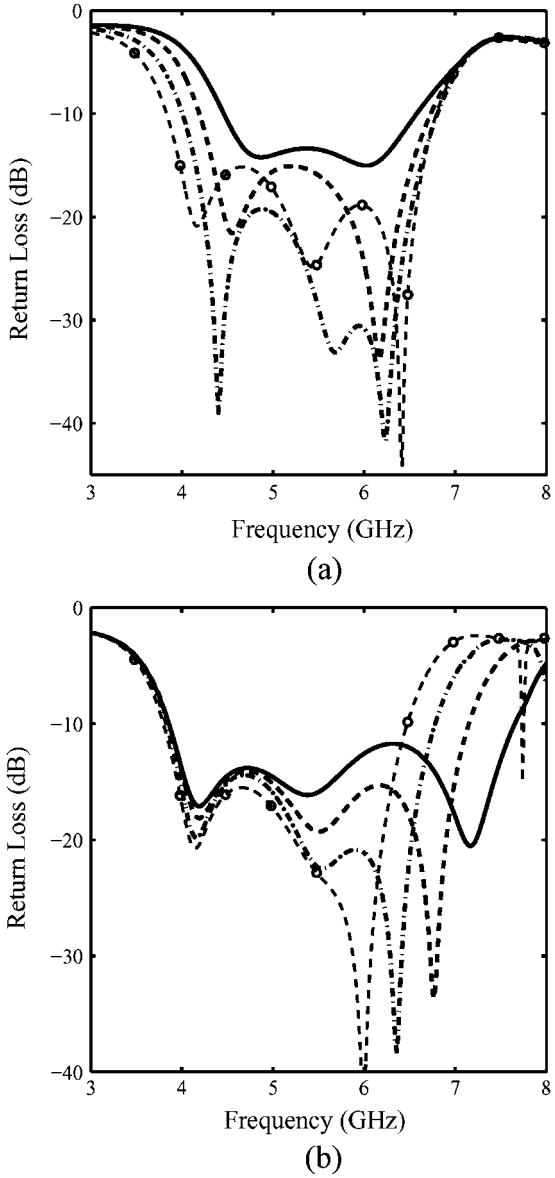

Fig. 9. Effects of antenna height h and dielectric constant on resonant frequency, $a = 3$ mm, $b = 6$ mm, $h_c = 1$ mm, $l = 5.35$ mm, $s = 0.2$ mm, $g = 0.5$ mm, $w = 10$ mm, $W_G = L_G = 70$ mm, $t = 0.6$ mm, (a) $\epsilon_r = 20$, —: $h = 10$ mm, − − −: $h = 11$ mm, −·−: $h = 12$ mm, −o−: $h = 13$ mm, (b) $h = 12$ mm, —: $\epsilon_r = 16$, − − −: $\epsilon_r = 18$, −·−: $\epsilon_r = 20$, −o−: $\epsilon_r = 22$.

Fig. 9(b) shows the effect of the DR permittivity on the resonant frequency. As the dielectric constant is increased, the wavelength in the cavity is reduced, rendering a lower resonant frequency. Note that the first resonant frequency is hardly affected by the dielectric constant.

V. Conclusion

In this paper, a broadband CPW-fed DR-monopole is proposed. The resonant bands of monopole and dielectric resonator are coupled to render a wide bandwidth of 47%. The bandwidth can be adjusted by tuning the resonant frequencies of the DR

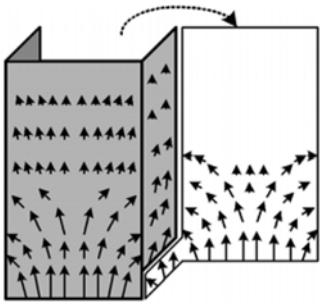

Fig. 10. Current distribution on metal coating (gray surface), and electric field distribution on DR surface (white surface) at $f = 5.5$ GHz, parameters are the same as in Fig. 9(a) with $h = 13$ mm.

and the monopole separately. The E_θ component is nearly omnidirectional on the horizontal plane over the band. The size of the DR-monopole is $12\,\mathrm{mm} \times 3.3\,\mathrm{mm} \times 5.6\,\mathrm{mm}$, and the bandwidth is wide enough to cover the IEEE 802.11a applications.

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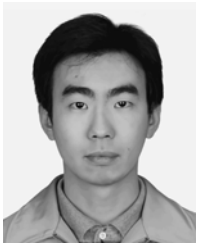

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Dualband Split Dielectric Resonator Antenna

Tze-Hsuan Chang, *Student Member, IEEE*, and Jean-Fu Kiang, *Member, IEEE*

***Abstract*—A dualband dielectric resonator antenna (DRA) is designed by splitting a rectilinear dielectric resonator (DR) and carving notches off the DR. It is observed that notches engraved at different positions affect different modes. Removal of dielectric material from where the electric field is strong incurs a significant increase in resonant frequency. The abrupt change of normal electric field across the discontinuities reduces the Q-factor and increases the impedance bandwidth. Both the TE^{y}_{111} and TE^{y}_{113} modes incur broadside radiation patterns on the xy-plane. The proposed DRA can cover both the worldwide interoperability for microwave access (WiMAX, 3.4–3.7-GHz) and the wireless local area network (WLAN, 5.15–5.35-GHz) bands.**

***Index Terms*—Dielectric resonator (DR).**

I. Introduction

DIELECTRIC resonators made of low-loss and high-permittivity material have been used to implement antennas [1]. They have higher radiation efficiency than printed antennas at higher frequency due to the absence of ohmic loss and surface wave, in addition to compact size, light weight, and low cost.

Many efforts have been devoted to developing multiband or wideband dielectric resonator antennas (DRAs) [2]–[15]. For example, make the feeding aperture radiate like a slot antenna to incur another band [2]–[4] and induce parasitic effects with attached metal strips [5]–[7].

In [8], specific higher order modes with the electric field distribution on the top surface of the dielectric resonator (DR) similar to that of the fundamental mode are intentionally excited. In [9] and [10], higher order modes of truncated conical or tetrahedral DR are excited to obtain wide impedance bandwidth.

DRs of different sizes have been placed vertically to form a stacked DRA, or at close proximity, to form a multielement DRA to attain wideband or dualband features [12]–[15].

In this paper, a dualband DR antenna is proposed by splitting a rectilinear DR evenly. The electric field over the gap in between is significantly enhanced, hence reducing the Q-factor. Two notches are also engraved in each piece to tune the resonant frequencies and increase the impedance bandwidth as well. The effect of the gap and notches on the resonant frequencies are carefully studied and the resonant bands associated with the TE^{y}_{111} and TE^{y}_{113} modes can be adjusted to cover the worldwide interoperability for microwave access (WiMAX, 3.4–3.7-GHz) and the wireless local area network (WLAN, 5.15–5.35-GHz) bands.

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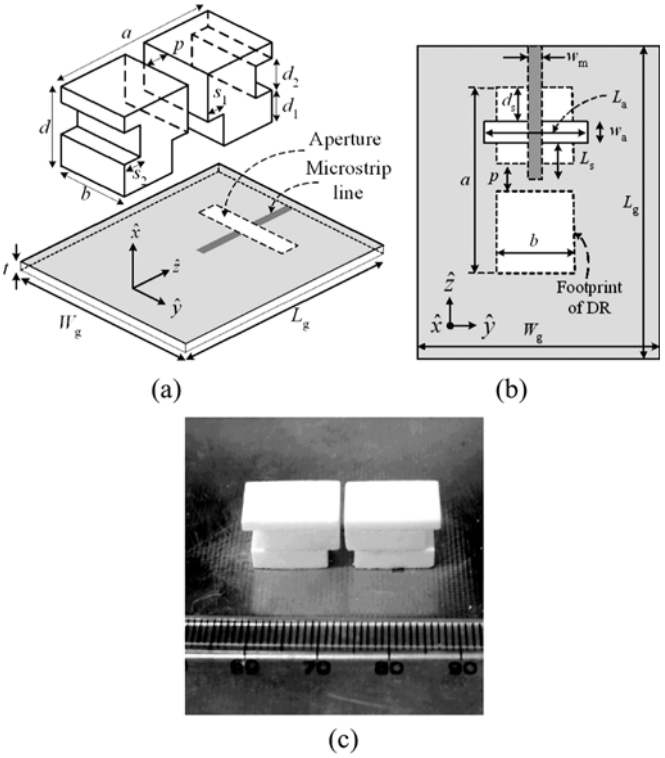

Fig. 1. Configuration of split DRA. (a) Panoramic view. (b) Top view. (c) Photograph.

II. Antenna Configuration

Fig. 1 shows the configuration of the DRA, which is composed of two identical rectangular DRs of dimension $a \times b \times d$, separated by a gap p. Each DR is engraved with two notches at its bottom and side edge, with dimensions $s_1 \times b \times d_1$ and $s_2 \times b \times d_2$, respectively. The DRs are placed on a ground plane of size $W_g \times L_g$ on an FR4 substrate of thickness t and permittivity 4.4. A microstrip line is used to feed the DRs through an aperture of size $L_a \times W_a$. The microstrip line is extended over the aperture by L_s. The offset between the aperture and the DR is d_s.

The resonant frequency is mainly determined by the DR dimensions a, b, d and permittivity $\epsilon_0\epsilon_r$. The carved notches change the electric field distribution in the original DRs, hence the resonant frequencies. Since the gap is perpendicular to the electric field of the TE^{y}_{111} mode of the otherwise intact DR, the electric field is enhanced within the gap. Thus, the resonant frequency of the TE^{y}_{111} mode and the input impedance are significantly affected. The input impedance can be fine tuned by adjusting the DR offset d_s, the length of the extended microstrip line, and the aperture length L_a.

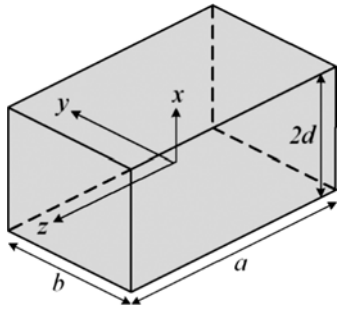

Fig. 2. Single block of dielectric resonator.

III. Prediction of Resonant Frequency Shift

The electric field $\bar{E}_0$ and the magnetic field $\bar{H}_0$ in a dielectric resonator taking the space V satisfy the Maxwell's equations

$$-\nabla \times \bar{E}_0 = j\omega_0 \mu \bar{H}_0 \tag{1}$$

$$\nabla \times \bar{H}_0 = j\omega_0 \epsilon \bar{E}_0 \tag{2}$$

where ω_0 is the resonant frequency. When the shape of dielectric resonator is modified by engraving gap, tunnel, or notch, the dielectric constant in the space V becomes a function of location $\epsilon'(\bar{r})$ and the field distributions and the resonant frequency become $\bar{E}, \bar{H}$ and ω, respectively, satisfying the Maxwell's equations as well. Applying the reaction operation between the original field and the perturbed field [16], the resonant frequency of the modified DR can be expressed as

$$\omega = \frac{\tilde{W}_m + \tilde{W}_{eb}}{\tilde{W}_m + \tilde{W}_{ea}}\omega_0 - \frac{j \iint_S (\bar{H} \times \bar{E}_0^* + \bar{H}_0^* \times \bar{E}) \cdot d\bar{s}}{\tilde{W}_m + \tilde{W}_{ea}} \tag{3}$$

where

$$\tilde{W}_m = \iiint_V \mu \bar{H}_0^* \cdot \bar{H} dv$$

$$\tilde{W}_{ea} = \iiint_V \epsilon(\bar{r}) \bar{E} \cdot \bar{E}_0^* dv$$

$$\tilde{W}_{eb} = \iiint_V \epsilon \bar{E}_0^* \cdot \bar{E} dv$$

which indicates that the resonant frequency is affected by the reaction between the field distributions of the original and the modified DR structures. It also implies that the resonant frequency can be more accurately predicted if the perturbed field can be approximated with reasonable accuracy. For example, if a small gap is carved off a DR, the electric field normal to the air-dielectric interface will be significantly enhanced, which can be observed by simulation.

IV. Rectangular Dielectric Resonator With Shape Modifications

A DR of dimension $d \times b \times a$ on an infinite ground plane can be viewed as a single block of rectangular dielectric with height $2d$ in free space, as shown in Fig. 2. Since the permittivity of DR is much higher than that of the air, the air-dielectric interface can be approximated as a perfect magnetic conductor (PMC) wall in a first-order analysis [17], and the modes can be categorized into transverse electric (TE) and transverse magnetic (TM) modes [18]. It is shown that the PMC approximation gives more accurate results with the TM modes than with the TE modes [17]. The dielectric waveguide model (DWM) is proposed to render more accurate prediction, in which the DR is treated as a portion of a dielectric waveguide truncated in the propagation direction [19]–[21]. The PMC approximation is imposed on the guide surfaces and total reflection is assumed in the propagation direction. By this way, the fields of the TE^y_{11m} modes with odd m can be derived as

$$\begin{aligned}
E_{0x} &= -k_z A \cos(k_x x)\cos(k_y y)\sin(k_z z)\\
E_{0y} &= 0\\
E_{0z} &= k_x A \sin(k_x x)\cos(k_y y)\cos(k_z z)\\
H_{0x} &= \frac{k_x k_y}{j\omega\mu} A \sin(k_x x)\sin(k_y y)\cos(k_z z)\\
H_{0y} &= \frac{k_x^2 + k_z^2}{j\omega\mu} A \cos(k_x x)\cos(k_y y)\cos(k_z z)\\
H_{0z} &= \frac{k_z k_y}{j\omega\mu} A \cos(k_x x)\sin(k_y y)\sin(k_z z)
\end{aligned} \tag{4}$$

where A is an arbitrary constant, $k_x = \pi/2d, k_z = m\pi/a$, and k_y is determined from [22]

$$\frac{k_y b}{2} = \tan^{-1}\left(\frac{\sqrt{k_x^2 + k_z^2}}{k_y}\right). \tag{5}$$

The resonant frequency can thus be calculated as

$$f_r = \frac{c}{\sqrt{\epsilon_r}}\sqrt{k_x^2 + k_y^2 + k_z^2}. \tag{6}$$

The field expressions of the TE^y_{11n} modes with even n can be derived as

$$\begin{aligned}
E_{0x} &= -k_z B \cos(k_x x)\cos(k_y y)\cos(k_z z)\\
E_{0y} &= 0\\
E_{0z} &= k_x B \sin(k_x x)\cos(k_y y)\sin(k_z z)\\
H_{0x} &= \frac{k_x k_y}{j\omega\mu} B \sin(k_x x)\sin(k_y y)\sin(k_z z)\\
H_{0y} &= \frac{k_x^2 + k_z^2}{j\omega\mu} B \cos(k_x x)\cos(k_y y)\sin(k_z z)\\
H_{0z} &= -\frac{k_z k_y}{j\omega\mu} B \cos(k_x x)\sin(k_y y)\cos(k_z z)
\end{aligned} \tag{7}$$

where B is an arbitrary constant, $k_x = \pi/2d, k_z = n\pi/a$, k_y and the resonant frequency can be determined from (5) and (6), respectively.

Fig. 3 illustrates the electric field distributions of the first three modes indexed by the third suffix, which indicates the number of variations of the electric field in the DR. The E_z component along the z-axis has an odd number of variations for the odd modes and has an even number of variations for the even modes. The E_x component is antisymmetric with respect to the x-axis for the odd modes and is symmetric for the even modes.

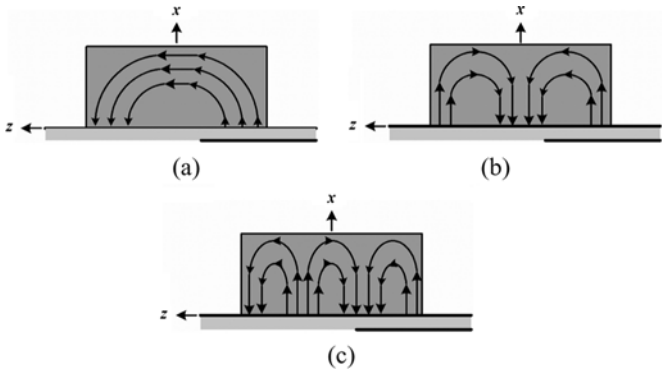

Fig. 3. Electric field distribution of (a) TE^{y}_{111} mode, (b) TE^{y}_{112} mode, and (c)TE^{y}_{113} mode of a solid DR.

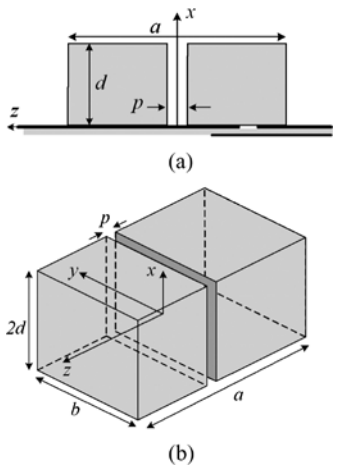

Fig. 4. (a) DRs on a ground plane with gap in between. (b) Panoramic view of the equivalent problem.

A. Field Enhancement by a Gap

Fig. 4(a) shows two rectangular DRs placed on a ground plane, separated by a gap at $z = 0$. At $z = 0, E_z$ component of the TE^{y}_{111} and TE^{y}_{113} modes reaches the maximum while that of the TE^{y}_{112} mode vanishes. The gap p is much smaller than a and the resonant modes associated with the single DR formed by filling the gap between the aforementioned two DRs are excited. The air-dielectric interface of the gap is normal to $\hat{z}$, hence the E_z component is significantly enhanced to satisfy the continuity condition on D_z.

Fig. 5 shows the effect of gap width p on the return loss. It is observed that the resonant frequency of the TE^{y}_{111} mode increases significantly, while those of the TE^{y}_{112} and TE^{y}_{113} modes are slightly affected. Note that the band associated with the TE^{y}_{111} mode merges with that of the TE^{y}_{112} mode.

By image theory, the structure in Fig. 4(a) is equivalent to that in Fig. 4(b) if the ground plane is of infinite extent. The two DRs with a separating gap can be regarded as an inhomogeneous DR with permittivity $\epsilon'(\bar{r})$. The gap width p is assumed much smaller than a, hence the field distribution inside the single inhomogeneous DR is almost the same as that without the gap, except the normal electric field E_z inside the gap is enhanced to satisfy the air-dielectric continuity condition. Thus, the fields of

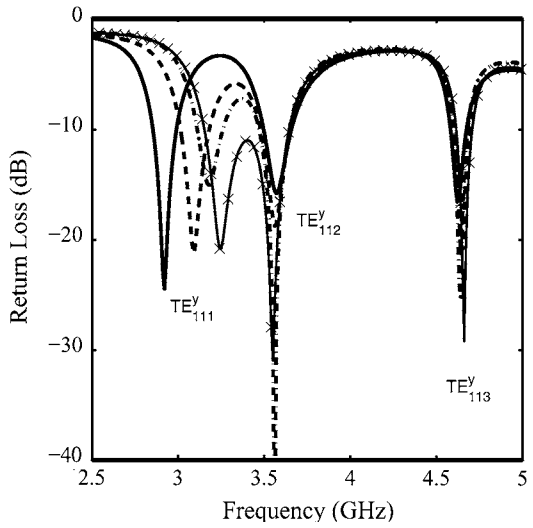

Fig. 5. Effect of gap width p on return loss, $a = 28$ mm, $b = 9$ mm, $d = 10$ mm, $\epsilon_r = 20, w_a = 2$ mm, $L_a = 10$ mm, $L_s = 8$ mm, $d_s = 7$ mm, $W_g = L_g = 70$ mm, $t = 0.6$ mm, $w_m = 1.15$ mm. (—) $p = 0$ mm. (- - -) $p = 0.2$ mm. $(- \cdot -)p = 0.4$ mm. $(- \times -)\, p = 0.5$ mm.

TABLE I
COMPARISON OF RESONANT FREQUENCY SHIFT DUE TO GAP WIDTH; FREQUENCY UNIT: GIGAHERTZ, LENGTH UNIT: MILLIMETER

$f_r(\Delta f)$	$p = 0.1$	$p = 0.2$	$p = 0.4$	$p = 0.5$
HFSS	3.03 (0.1)	3.11 (0.18)	3.25 (0.33)	3.3 (0.37)
Theory (TE^{y}_{111})	2.93 (0.1)	3.03 (0.2)	3.23 (0.41)	3.33 (0.51)
HFSS	3.65 (0.01)	3.67 (0.03)	3.65 (0.01)	3.66 (0.02)
Theory (TE_{112})	3.666 (0.014)	3.673 (0.028)	3.669 (0.056)	3.696 (0.07)
HFSS	4.64 (0.01)	4.65 (0.02)	4.66 (0.03)	4.67 (0.04)
Theory (TE^{y}_{113})	4.7 (0.02)	4.755 (0.04)	4.86 (0.05)	4.92 (0.07)

the TE^{y}_{111} and TE^{y}_{113} modes in the air gap can be approximated as

$$\begin{aligned} E_z &= m_1 k_x A \sin(k_x x)\cos(k_y y)\cos(k_z p/2) \\ E_x &= E_y \simeq 0 \\ \bar{H} &= \bar{H}_0. \end{aligned} \tag{8}$$

Note that the E_z component is enhanced by a factor m_1. For the TE^{y}_{111} mode, m_1 approaches ϵ_r as the gap width is very small. For the TE^{y}_{113} mode, it is observed that the E_z component is only slightly enhanced, incurring a small m_1 of about 2 to 3. Hence, the resonant frequency of the TE^{y}_{113} mode is slightly increased. In contrast, the fields of the TE^{y}_{112} modes in the air gap are approximately

$$\begin{aligned} E_x &= k_z B \cos(k_y y)\cos(k_x x) \\ E_z &= E_y \simeq 0 \\ \bar{H} &= \bar{H}_0. \end{aligned} \tag{9}$$

Substituting (4) and (8) with $k_z = \pi/a$ and $k_z = 3\pi/a$, respectively, into (3), the resonant frequencies of the TE^{y}_{111} and TE^{y}_{113} modes can be estimated. Substituting (7) and (9) with $k_z = 2\pi/a$ into (3), the resonant frequency of the TE^{y}_{112} mode can be estimated. The theoretical prediction and simulated results are summarized in Table I. The resonant frequency of the DR is also affected by the feeding position, resulting in a deviation between

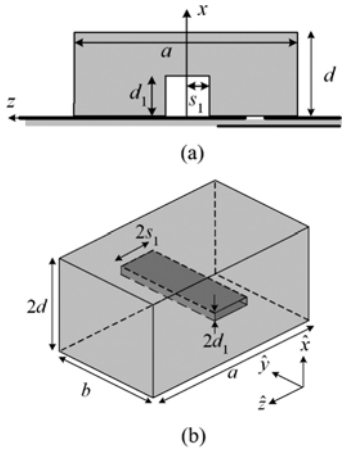

Fig. 6. (a) DR on ground plane with tunnel engraved at its bottom. (b) Equivalent problem of DR in free space with a tunnel.

simulation and prediction. Note that the increments of resonant frequency listed in the parentheses match reasonably well.

The radiation patterns can be determined from the tangential electric fields on the DR surfaces. Since the electric field distribution of the TE^y_{112} mode $E_z \propto \sin(2\pi z/a)$ has opposite directions on different portions of the DR top surface, a null in the E_θ pattern occurs in the $\hat{x}$-direction. The resonant frequencies of the TE^y_{111} and TE^y_{112} modes move closer as p is increased and the two bands are merged at $p = 0.5$ mm. However, due to the difference of radiation pattern, it is preferred to separate the band associated with the TE^y_{112} mode from that with the TE^y_{111} mode.

B. Effect of an Air Tunnel

Based on (3), the resonant frequency of the TE^y_{112} mode can be shifted away from that of the TE^y_{111} mode if an air tunnel is engraved at where the electric field of the TE^y_{112} mode is strong while that of the TE^y_{111} mode is negligible. As shown in Fig. 6(a), an air tunnel is engraved at the center bottom of the DR with the dimensions of $d_1 \times b \times 2s_1$. The effect of the tunnel half-width s_1 is shown in Fig. 7. The resonant frequency of the TE^y_{112} mode is increased as s_1 and d_1 increase, while those of the TE^y_{111} and TE^y_{113} modes are almost unaffected since their electric field at the tunnel is weak.

Fig. 6(b) shows an equivalent problem in free space by doubling the heights of the DR and the tunnel using the image theory. Since the electric field of the TE^y_{111} and the TE^y_{113} modes rotates about the $\hat{y}$-axis, the field is tangential to the air-dielectric interface of the tunnel. Hence, it is reasonable to assume that $\bar{E} \simeq \bar{E}_0$ and $\bar{H} \simeq \bar{H}_0$.

As for the TE^y_{112} mode, the tunnel is located at where the electric field reaches the maximum. The E_x component is enhanced in the tunnel and can be approximated as

$$\begin{aligned} E_x &= k_z \alpha B \cos(k_x d_1)\cos(k_y y)\cos(\beta z) \\ E_z &= E_y \simeq 0 \\ \bar{H} &= \bar{H}_0. \end{aligned} \tag{10}$$

By observing the simulated field distributions and fitting the data, we record $\alpha \simeq 10$ and $\beta \simeq 568.8$ at $d_1 = 0.5$ mm, $\alpha \simeq 1.5$ and $\beta \simeq 275$ at $d_1 = 4$ mm. Substituting (7) and (10) with $k_z = 2\pi/a$ into (3), the resonant frequency shift of the TE^y_{112} mode is predicted. The simulated and predicted results are summarized in Table II. The tunnel has stronger effect on the resonant frequency of the TE^y_{112} mode than that of the TE^y_{111} and TE^y_{113} modes. Hence, the effect of tunnel height of $d_1 = 0.5$ mm and $d_1 = 4$ mm, respectively, is investigated and listed in Table II. It is observed that the E_x is strongly enhanced by α fold as the tunnel is thin. The resonant frequency f_r of the TE^y_{112} mode is 3.646 GHz. The increments of resonant frequency listed in the parentheses match reasonably well.

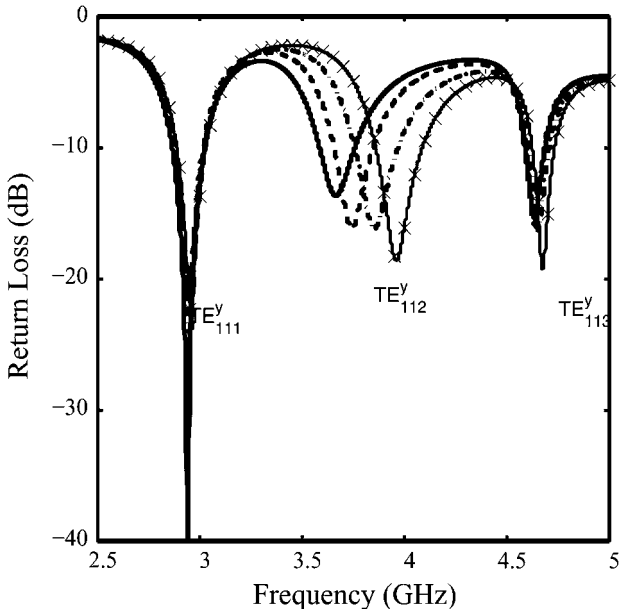

Fig. 7. Effect of s_1 on return loss, $a = 28$ mm, $b = 9$ mm, $d = 10$ mm, $p = 0$ mm, $d_1 = 4$ mm, $\epsilon_r = 20$, $w_a = 2$ mm, $L_a = 10$ mm, $L_s = 8$ mm, $d_s = 7$ mm, $W_g = L_g = 70$ mm, $t = 0.6$ mm, $w_m = 1.15$ mm. (—) $s_1 = 0.5$ mm. (- - -) $s_1 = 1$ mm. (— · —) $s_1 = 1.5$ mm. (— × —) $s_1 = 2$ mm.

TABLE II
COMPARISON OF RESONANT FREQUENCY SHIFT DUE TO TUNNEL WIDTH; LENGTH UNIT: MILLIMETER, FREQUENCY UNIT: GIGAHERTZ

$f_r(\Delta f)$	$s_1 = 0.5$	$s_1 = 1$	$s_1 = 1.5$	$s_1 = 2$
TE^y_{111}				
HFSS	2.93 (0.01)	2.94 (0.02)	2.94 (0.02)	2.95 (0.03)
Theory	2.83 (0.008)	2.844 (0.015)	2.85 (0.023)	2.86 (0.032)
$d_1 = 4$				
TE^y_{112}				
HFSS	3.6 (0.02)	3.64 (0.06)	3.67 (0.09)	3.73 (0.15)
Theory	3.68 (0.03)	3.7 (0.05)	3.72 (0.07)	3.73 (0.08)
$d_1 = 0.5$				
$\alpha = 10$				
TE^y_{112}				
HFSS	3.67 (0.07)	3.74 (0.14)	3.85 (0.25)	3.96 (0.33)
Theory	3.74 (0.08)	3.82 (0.165)	3.91 (0.246)	3.98 (0.323)
$d_1 = 4$				
$\alpha = 1.5$				
TE^y_{113}				
HFSS	4.63 (0.01)	4.63 (0.01)	4.65 (0.03)	4.67 (0.05)
Theory	4.65 (0.004)	4.66 (0.013)	4.68 (0.032)	4.71 (0.066)
$d_1 = 4$				

C. Modification by Engraving Notches

Since the E_x component of the $\mathrm{TE}^y_{111}, \mathrm{TE}^y_{112}$, and TE^y_{113} modes reaches maximum at $z = \pm a/2$, their resonant frequencies should be affected by notches near $z = \pm a/2$. Fig. 8(a)

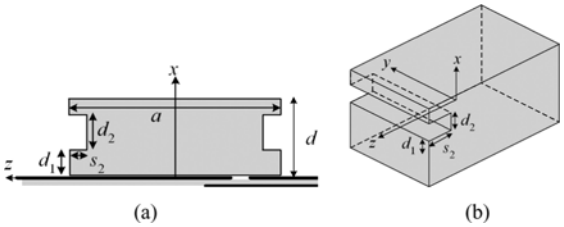

Fig. 8. (a) Grounded dielectric resonator with two notches on its edges. (b) Panoramic view of an isolated DR with one notch.

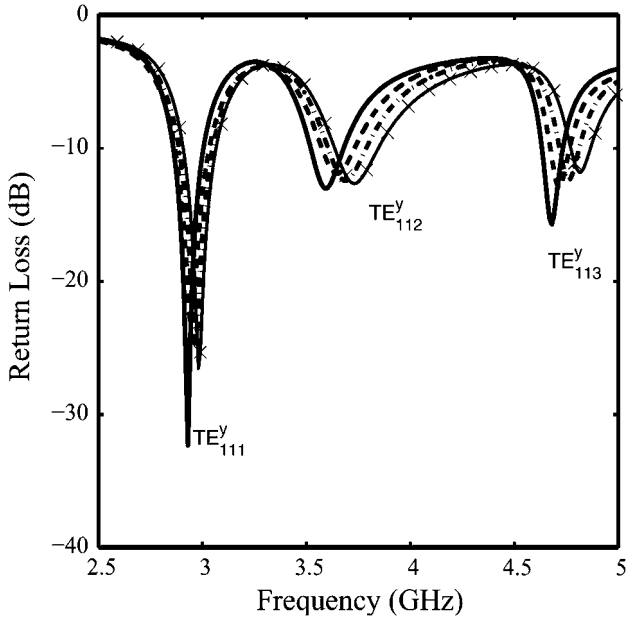

Fig. 9. Effect of s_2 on return loss, $a = 28$ mm, $b = 9$ mm, $d = 10$ mm, $\epsilon_r = 20$, $w_a = 2$ mm, $L_a = 10$ mm, $L_s = 8$ mm, $d_s = 7$ mm, $W_g = L_g = 70$ mm, $t = 0.6$ mm, $w_m = 1.15$ mm. (—) $s_2 = 0.5$ mm. (- - -) $s_2 = 1$ mm. (— · —) $s_2 = 1.5$ mm. (— × —) $s_2 = 2$ mm.

TABLE III
COMPARISON OF RESONANT FREQUENCY SHIFT DUE TO NOTCH DEPTH $m_2 = 1.5$; LENGTH UNIT: MILLIMETER, FREQUENCY UNIT: GIGAHERTZ

$f_r(\Delta f)$ (GHz)	$s_2 = 0.5$	$s_2 = 1$	$s_2 = 1.5$	$s_2 = 2$
HFSS	2.93 (0.01)	2.95 (0.04)	2.96 (0.05)	2.98 (0.07)
Theory	2.86 (0.03)	2.89 (0.06)	2.92 (0.09)	2.95 (0.12)
TE^y_{111}				
HFSS	3.59 (0.01)	3.65 (0.07)	3.69 (0.11)	3.73 (0.15)
Theory	3.71 (0.06)	3.78 (0.12)	3.84 (0.18)	3.9 (0.23)
TE^y_{112}				
HFSS	4.68 (0.04)	4.72 (0.08)	4.76 (0.12)	4.82 (0.18)
Theory	4.75(0.11)	4.85(0.21)	4.94(0.30)	5.02(0.37)
TE^y_{113}				

shows a grounded DRA with two notches engraved around its edge. The notches will distort the electric field distribution and the Q-factor of the DR will decrease, incurring a wider impedance bandwidth. Fig. 9 shows that the resonant frequencies of the three modes are increased by increasing the notch depth s_2.

By image theory, the grounded DR with two notches is equivalent to an isolated DR with four notches on its edges. First, consider only one notch of dimensions $d_2 \times b \times s_2$ engraved off a DR in free space, as shown in Fig. 8(b). The electric field within the notch is more complicated since both E_x and E_z components exist. The simulation show that the E_x component is stronger

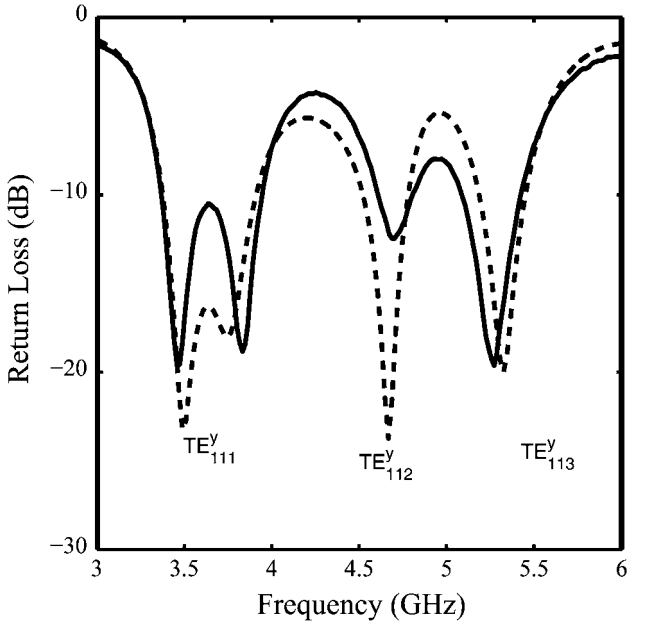

Fig. 10. Return loss, $a = 28$ mm, $b = 9$ mm, $d = 10$ mm, $p = 1$ mm, $d_1 = 4$ mm, $s_1 = 2$ mm, $d_2 = 4$ mm, $s_2 = 2$ mm, $\epsilon_r = 20$, $h = 4$ mm, $w_a = 2$ mm, $L_a = 10$ mm, $L_s = 2.5$ mm, $d_s = 4$ mm, $W_g = L_g = 70$ mm, $t = 0.6$ mm, $w_m = 1.15$ mm. (—) Measurement. (- - -) Simulation.

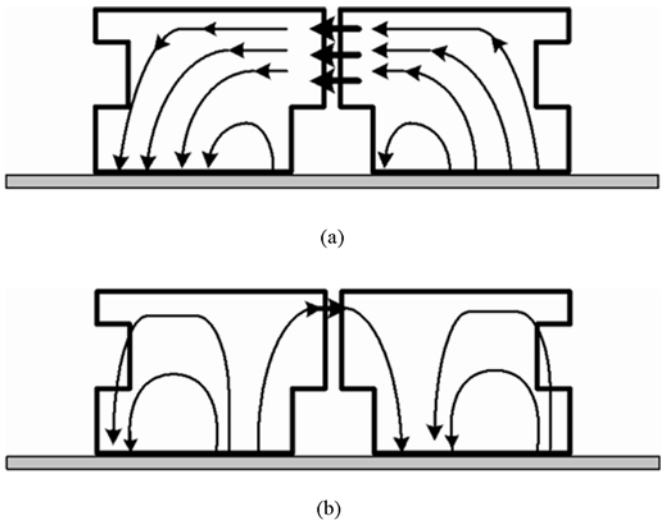

Fig. 11. Electric field distribution at (a) 3.45 and (b) 5.26 GHz.

than the E_z component. The E_x component normal to the air-dielectric interface of the notch is enhanced to satisfy the continuity condition and can be approximated as

$$E_x = -m_2 k_z A \cos(k_x d_1) \cos(k_y y) \sin(k_z z), \quad \text{for } \mathrm{TE}^y_{111} \text{ and } \mathrm{TE}^y_{113} \text{ modes} \tag{11}$$

$$E_x = m_2 k_z B \cos(k_x d_1) \cos(k_y y) \cos(k_z z), \quad \text{for } \mathrm{TE}^y_{112} \text{ modes.} \tag{12}$$

With $d_2 = 4$ mm, m_2 is about 1.5. Substituting (4) and (11) into (3), the resonant frequencies of the DR with notches are obtained. The predicted and the simulated results are summarized in Table III. The prediction for the TE^y_{113} mode is less accurate, but the increasing trend is consistent.

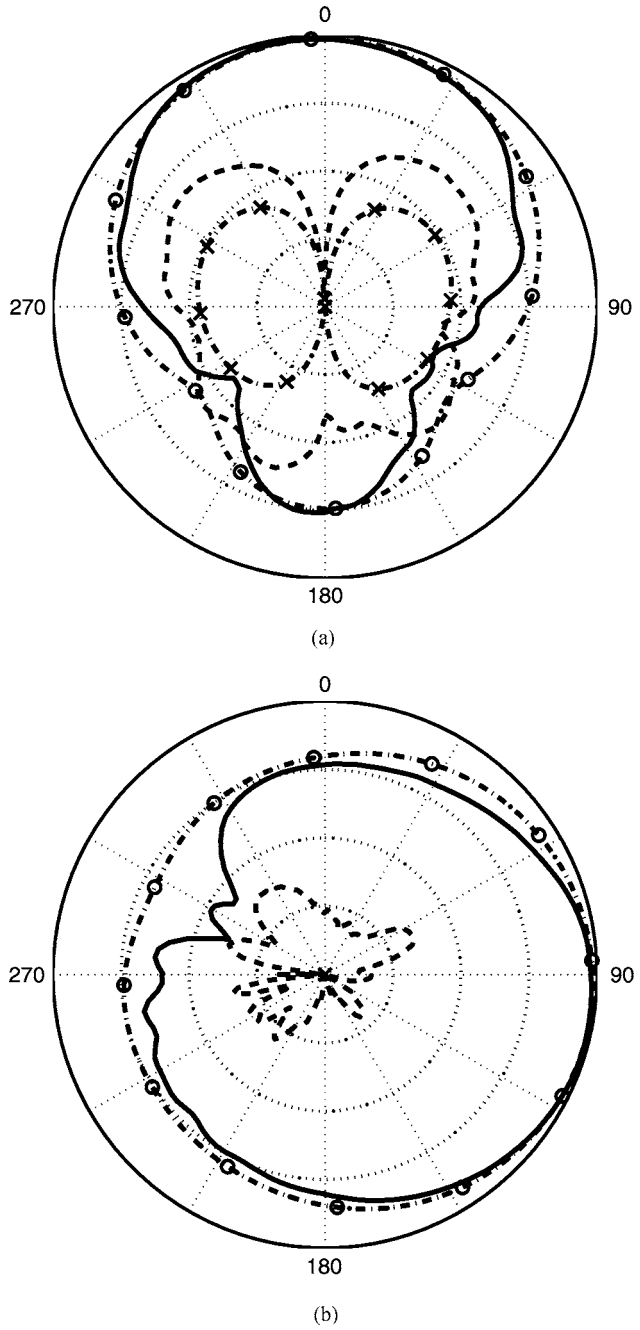

Fig. 12. Radiation patterns at $f = 3.45$ GHz: (a) xy-plane and (b) xz-plane. (—) Measured E_θ. (- - -) Measured E_ϕ ($-\circ-$) Simulated E_θ. ($-\times-$) Simulated E_ϕ, the gain at $\theta = 90°$ and $\phi = 0°$ is 5.6 dBi, 10-dB per division on radials; all parameters are the same as in Fig. 10.

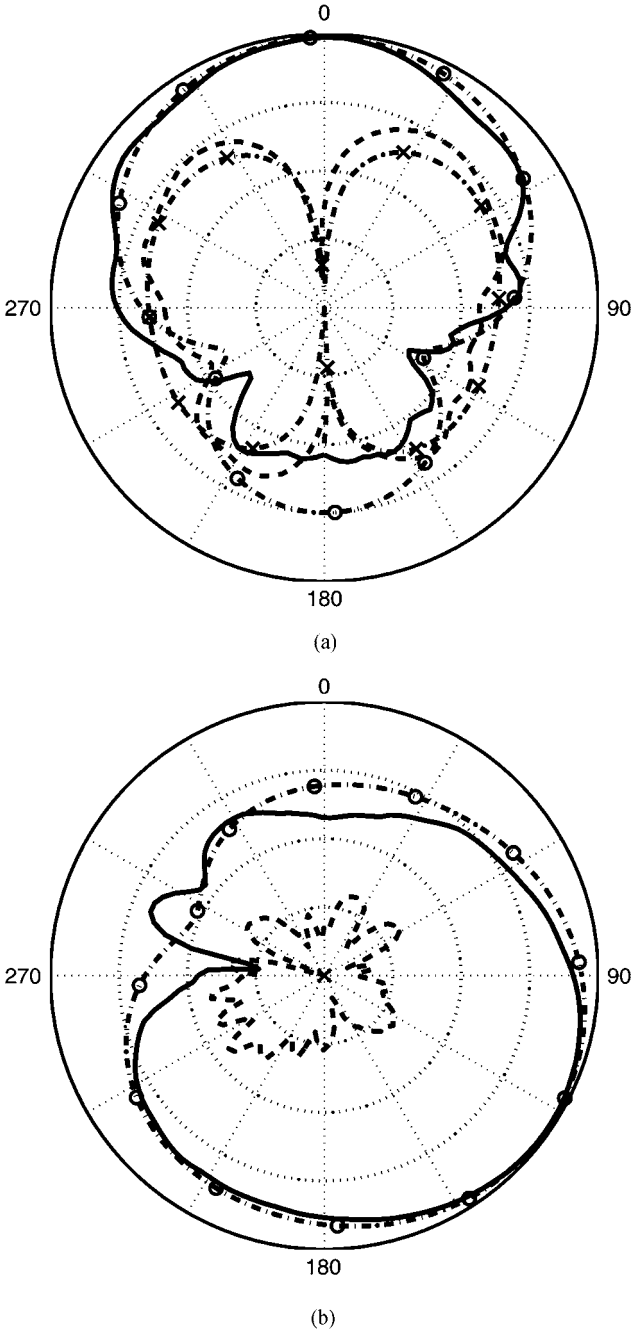

Fig. 13. Radiation patterns at $f = 3.6$ GHz: (a) xy-plane and (b) xz-plane. (—) Measured E_θ. (- - -) Measured E_ϕ. ($-\circ-$) Simulated E_θ. ($-\times-$) Simulated E_ϕ, the gain at $\theta = 90°$ and $\phi = 0°$ is 3 dBi, 10-dB per division on radials; all parameters are the same as in Fig. 10.

V. Design With Combination

The design begins with a rectangular DR of dimension 10 mm $\times$ 9 mm $\times$ 29 mm, $d_s = 7$ mm, $L_s = 8$ mm, $w_a = 2$ mm, and $L_a = 10$ mm. The resonant frequencies of the TE^y_{111}, TE^y_{112}, and TE^y_{113} modes are 2.92, 3.58, and 4.62 GHz, respectively. In order to tune the resonant frequencies of the TE^y_{111} and TE^y_{113} modes to cover the WiMax (3.4–3.7-GHz) and the WLAN (5.15–5.35-GHz) bands, the DR is modified to the shape as shown in Fig. 1(a), with $p = 1$ mm, $d_1 = d_2 = 4$ mm, and $s_1 = s_2 = 2$ mm. The resonant frequencies of the three modes are shifted to 3.58, 4.3, and 5 GHz, respectively. By adjusting the offset d_s, the extended length of microstrip line L_s, and the length of the aperture L_a, the DR can be matched to 50 Ω microstrip line feed, with the resonant frequencies slightly affected by the feeding structure. Fig. 10 shows the measured and simulated return loss. There are three bands over 3.375–3.93 GHz (15%), 4.6–4.79 GHz (4%), and 5.08–5.415 GHz (6%), associated with the TE^y_{111}, TE^y_{112}, and TE^y_{113} modes, respectively. The first band covers the WiMax (3.4–3.7 GHz) and the third band covers the WLAN (5.15–5.35 GHz).

Fig. 11 shows the electric field distributions over the first and the third bands, respectively. The third resonant band around

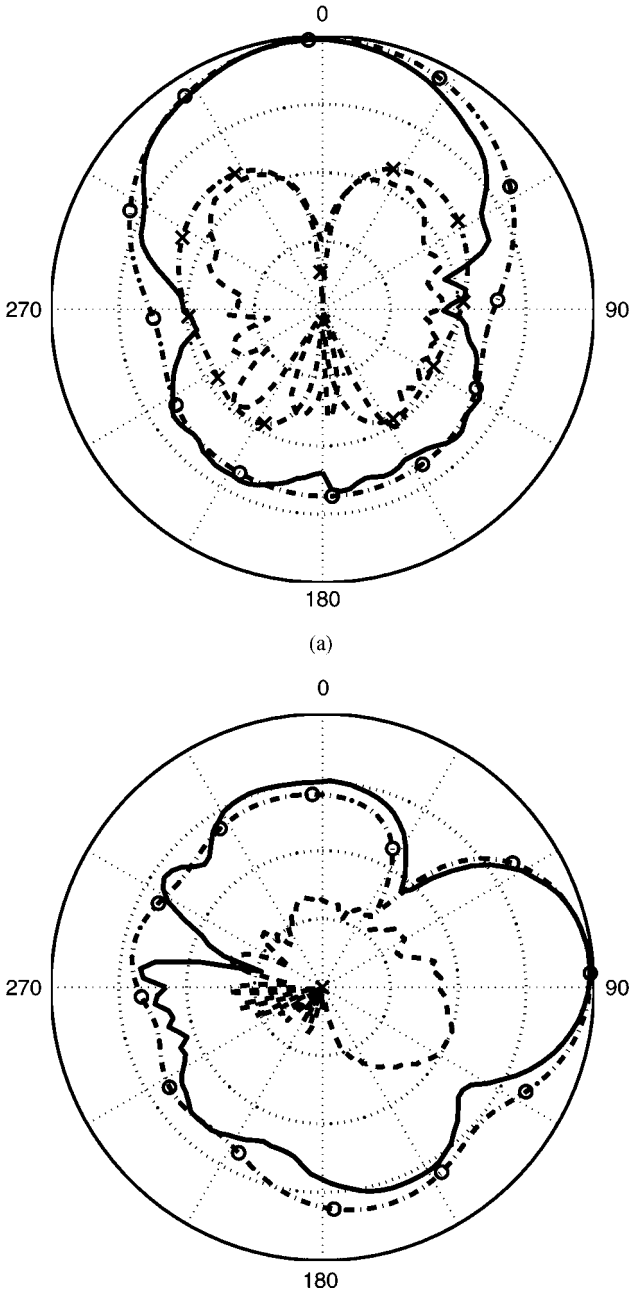

Fig. 14. Radiation pattern at 5.265 GHz: (a) xy-plane and (b) xz-plane. (—) Measured E_θ. (- - -) Measured E_ϕ. ($-\circ-$) Simulated E_θ. ($-\times-$) Simulated E_ϕ, the gain at $\theta = 90^\circ$ and $\phi = 0^\circ$ is 7.2 dBi, 10-dB per division on radials; all parameters are the same as in Fig. 10.

$f = 5.265$ GHz is associated with the TE^y_{113} mode. The split DRs can be viewed as two radiators placed closely along the $\hat{z}$-direction.

Figs. 12 and 13 show the measured and simulated radiation patterns at $f = 3.45$ GHz and $f = 3.6$ GHz, respectively. On the xy-plane, the E_θ component is stronger than the E_ϕ component by about 10 dB over $-60^\circ \leq \phi \leq 60^\circ$, the maximum gain is 5.6 dBi at $f = 3.45$ and 3 dBi at $f = 3.6$ GHz. The gain at 3.6 GHz is lower because the main beam of the E_θ pattern is slightly tilted on the xz-plane.

On the xz-plane, the E_θ component is stronger than the E_ϕ component by 10 dB over $-90^\circ \leq \theta \leq 90^\circ$ and the maximum gain is 6.5 dBi at $f = 3.45$ GHz and 6 dBi at $f = 3.6$ GHz. The front-to-back ratio is about 10 dB.

Fig. 14 shows the measured and simulated radiation patterns at $f = 5.265$ GHz. On the xy-plane, the E_θ component is stronger than the E_ϕ component by about 10 dB over $-75^\circ \leq \phi \leq 75^\circ$, and the front-to-back ratio is about 12 dB. The antenna gain is 7.22 dBi, which is higher than that at $f = 3.45$ and 3.6 GHz because the beam of the E_θ pattern on the xz-plane is narrower and is slightly tilted to $\theta = 85^\circ$. The gain at the beam direction is 8.4 dBi.

The efficiency is about 94% for the TE^y_{111} and TE^y_{113} modes. The insertion loss of the feeding microstrip is about 0.5 dB due to the substrate loss. For WiMax or WLAN applications, this DRA can be mounted on a vertical wall with the $\hat{z}$-axis pointing to zenith, providing a broadside, vertically polarized radiation pattern in front of the wall ($\hat{x}$-direction).

VI. Conclusion

A dualband DRA is proposed, which is composed of two notched DRs separated by a narrow air gap. The effects of gap and notches on the resonant frequency shift are carefully studied. Two bands are attained in 3.375–3.93 GHz (15%) and 5.08–5.415 GHz (6%) with broadside E_θ pattern on the xy-plane; the third band in 4.6–4.79 GHz (4%) is not practical. The proposed DRA can be used in the WiMAX (3.4–3.7 GHz) and WLAN (5.15–5.35 GHz) bands.

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A K-Band CMOS Low-Noise Amplifier with Low DC Power Consumption

Ping-Yuan Deng, *Student Member, IEEE* and Jean-Fu Kiang, *Member, IEEE*

***Abstract*— A K-band low-noise amplifier (LNA) is designed and fabricated in a standard 0.18 μm CMOS technology. A design method of CMOS LNA is used to render the optimum source resistance ($R_{\rm opt}$) close to 50 Ω and $Z_{\rm in} = Z_{\rm opt}^*$ by using small devices and small bias currents. This LNA chip achieves a peak gain of 13.5 dB and a noise figure of 4.7 dB at 24 GHz. The supply voltage and supply current are 1 V and 8.3 mA, respectively. The input and output return loss are lower than -10 dB. The input referred 1-dB compression ($P_{\rm 1dB}$) is -7 dBm. The chip size is 0.64 mm $\times$ 0.48 mm.**

***Index Terms*— CMOS, K-band, low-noise amplifier (LNA), microwave monolithic integrated circuit (MMIC).**

I. Introduction

AT frequencies above 20 GHz, GaAs-based HEMT and HBT processes dominate most of the applications in the past. With the rapid advance of CMOS technologies, it is becoming plausible to implement RF systems operating at 20 GHz and higher using CMOS technologies. RF and baseband circuits realized in CMOS are expected to reduce the cost of systems such as FMCW (24 GHz ISM band) [2], ultra-wideband (UWB, 22-29 GHz) short-range radars [3], and local multipoint distribution systems (LMDS). Low-noise amplifier is a key module for any RF system. CMOS LNAs have been designed for frequencies above 20 GHz [4]-[6]. LNAs with low noise figures (NFs) are usually achieved at the expense of high dc power consumption.

In this paper, we present a design method of CMOS low-noise amplifiers to achieve simultaneous noise matching and power matching by tailoring the device size. It is found that $R_{\rm opt}$ close to 50 Ω and $Z_{\rm in} = Z_{\rm opt}^*$ can be obtained by using small devices and small currents. This design also achieves acceptable power gain, low noise figure and low power consumption. Circuit design considerations of LNA will be presented in Section II. Simulation and measurement results will be discussed in Section III, followed by the conclusions.

II. Circuit Design

A. General Considerations

Fig. 1 shows the two-port network of a microwave amplifier. The transducer power gain G_T and available power gain G_A can be derived as [1]

$$G_T = \frac{1-|\Gamma_S|^2}{|1-S_{11}\Gamma_S|^2}\,|S_{21}|^2\,\frac{1-|\Gamma_L|^2}{|1-\Gamma_{\rm out}\Gamma_L|^2}$$

$$G_A = \frac{1-|\Gamma_S|^2}{|1-S_{11}\Gamma_S|^2}\,|S_{21}|^2\,\frac{1}{1-|\Gamma_{\rm out}|^2}$$

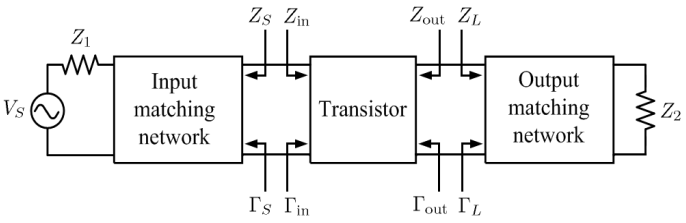


Fig. 1. Two-port network of a microwave amplifier.

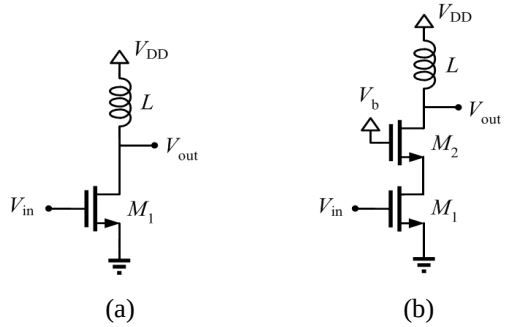


Fig. 2. LNA topology, (a) common-source amplifier, (b) cascode amplifier.

The transducer gain G_T is affected by the input and output matching networks. In the LNA design, the input matching network transforms Z_1 to $Z_{\rm opt}$ ($\Gamma_S = \Gamma_{\rm opt}$) to achieve minimum noise figure $\rm NF_{min}$. If the load reflection coefficient Γ_L is adjusted to transfer maximum power to the load ($\Gamma_L = \Gamma_{\rm out}^*$), then $G_T = G_A$. In practice, input matching in the LNA design usually involves trade-offs among power gain, noise figure, and VSWRs .

Many LNA topologies have been proposed in the literatures [5], [7]. The most frequently used LNA topology is the common-source (CS) and cascode configurations as shown in Fig. 2. The CS-stage can exhibit minimum noise figure with a proper input matching, and it can work at low supply voltage below 1 V. The cascode amplifier has higher power gain and reduced Miller effect, but it can not work at low supply voltage. Compared to a common-source amplifier, the cascode amplifier has a poorer noise performance especially when the operation frequency is close to $f_{\rm T}$. Hence, the CS-stage is chosen in this work.

B. Noise Matching with Power Matching

Fig. 3 (a) shows a common-source amplifier with source inductor $L_{\rm s1}$ as a feedback. Fig. 3 (b) shows the small-

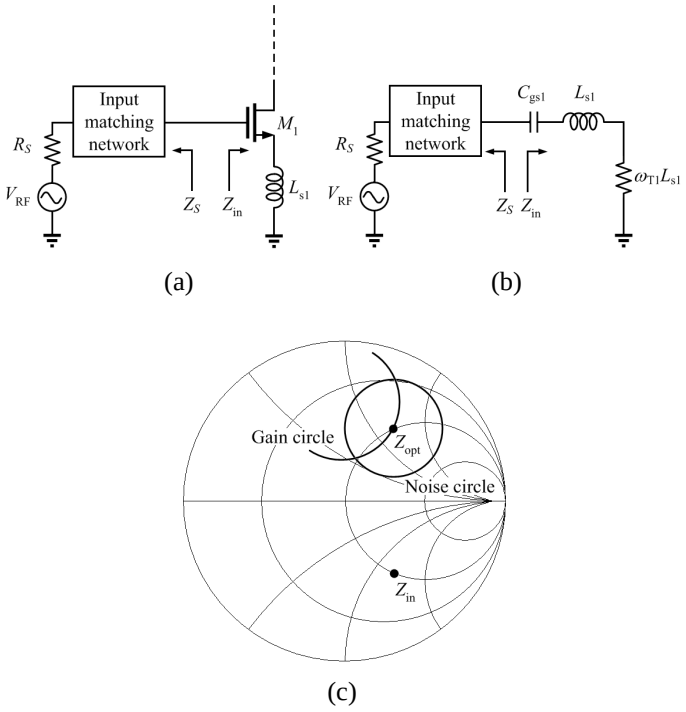


Fig. 3. (a) Schematic of the source inductive degeneration amplifier, (b) small-signal equivalent circuit of the input matching network of (a), where $\omega_{\mathrm{T1}} = g_{\mathrm{m1}}/C_{\mathrm{gs1}}$, (c) gain circle and noise circle on the Smith chart.

signal equivalent circuit of the input impedance in Fig. 3 (a). Neglecting the gate-drain capacitance, source-bulk capacitance and parasitic resistance of L_{s1}, the input impedance can be calculated as

$$Z_{\mathrm{in}} \simeq \frac{g_{m1}L_{\mathrm{s1}}}{C_{\mathrm{gs1}}} + sL_{\mathrm{s1}} + \frac{1}{sC_{\mathrm{gs1}}}$$

Thus, proper choice of g_{m1}, L_{s1}, and C_{gs1} will yield an input impedance $Z_{\mathrm{in}} = R_{\mathrm{in}} - jX$, where $R_{\mathrm{in}} = g_{m1}L_{\mathrm{s1}}/C_{\mathrm{gs1}} = 50$ Ω and $X = 1/\omega C_{\mathrm{gs1}} - \omega L_{\mathrm{s1}}$. In practice, the last two terms may not resonate at the frequency of interest. By selecting appropriate L_{s1}, the input impedance will be moved close to the constant 50 Ω circle in the Smith chart, thereby simplifying the input matching network [7]. Another advantage of this technique is that the gain circles around the maximum gain and the noise circles around the minimum noise figure become closer as shown in Fig. 3 (c) [8], [9].

The equivalent transconductance can be expressed as

$$g'_{m1} = \frac{g_{m1}}{1 + j\omega L_{\mathrm{s1}}(g_{m1} + j\omega C_{\mathrm{gs1}})}$$

where C_{gs1} is the gate-to-source capacitance, and g_{m1} is the transconductance without inductive source degeneration. The inductive source degeneration will make the transistor more resistive and increase the linearity of M_1, at the cost of decreasing its equivalent transconductance.

In the LNA design, the source impedance is chosen as $Z_S = Z_{\mathrm{opt}}$ for noise matching to reach $\mathrm{NF}_{\mathrm{min}}$. The input impedance is chosen as $Z_{\mathrm{in}} = Z_S^*$ to achieve power matching. By tailoring the device size of M_1 and the value of L_{s1}, we can make R_{opt} close to 50 Ω and $Z_{\mathrm{in}} = Z_{\mathrm{opt}}^*$ with a small bias current, thus

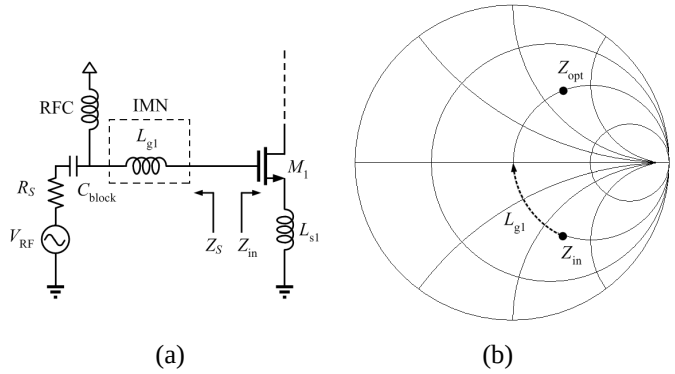


Fig. 4. (a) Schematic of source inductor feedback amplifier with series inductor, (b) effect of adding L_{g1}.

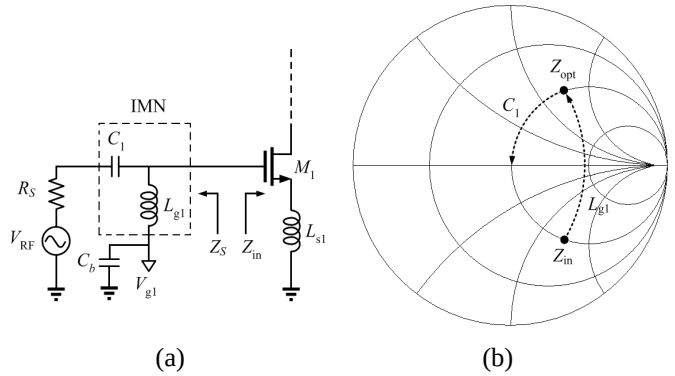


Fig. 5. (a) Schematic of source inductor feedback amplifier with shunt inductor and series capacitor, (b) effect of adding L_{g1} and C_1.

the dc power consumption can be reduced. In other words, if the conditions

$$\mathrm{Re}\,(Z_S) = \mathrm{Re}\,(Z_{\mathrm{opt}}) = 50\ \Omega$$
$$Z_{\mathrm{in}} = Z_S^* = Z_{\mathrm{opt}}^*$$

are met, then the goals of high gain, low noise figure, reasonable VSWRs, and low power consumption can be achieved simultaneously. Because Z_{in} is frequency independent, thus simultaneous noise and power matching can be achieved in a specific frequency band.

C. Input Matching Network

Fig. 4 (a) shows the schematic of the source inductor feedback amplifier with the gate inductor L_{g1} for input impedance matching [9]. To achieve noise matching, Z_S = Z_{opt}, and power matching, $Z_{\mathrm{in}} = Z_S^* = Z_{\mathrm{opt}}^* = R_{\mathrm{opt}} - jX$, an additional gate inductor L_{g1} is used to resonate with $-jX$ at the intended frequency, as shown in Fig. 4 (b). However, the inductance L_{g1} is about 0.5$\sim$1 nH at 24 GHz, and the noise performance of L_{g1} is sensitive to its parasitic resistance. Additional bias network such as a large shunt resistor (or RFC) and large dc-block capacitors are required. Consequently, an alternative input matching network is required at this frequency range.

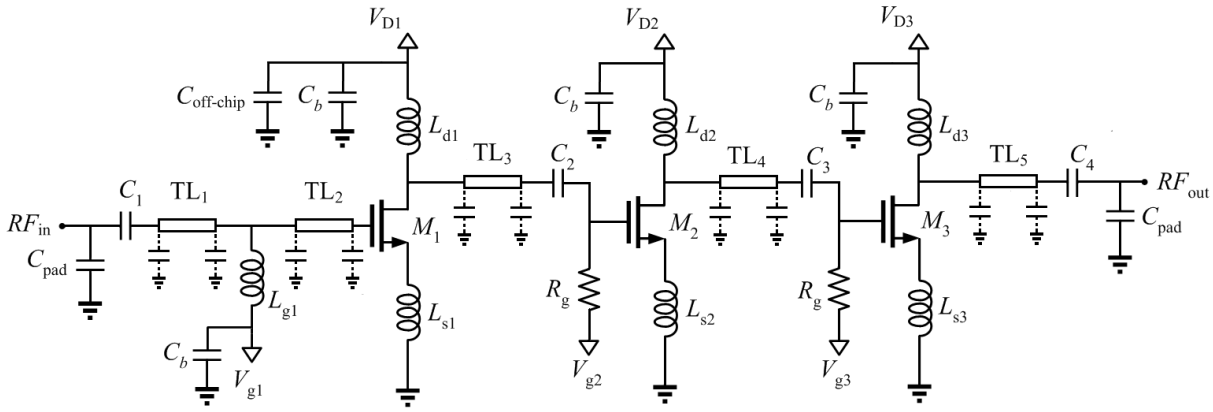


Fig. 6. Schematic of K-band LNA.

Fig. 5 (a) shows the proposed schematic of source inductor feedback amplifier with shunt inductor and series capacitor for input impedance matching. Proper device size of M_1 is chosen to tune the source impedance into $Z_{\rm S} = Z_{\rm opt} = R_{\rm opt} + jX = 50 + jX$. At conjugate matching ($Z_{\rm in} = Z^*_{\rm opt}$) as shown in Fig. 5 (b), a shunt inductor $L_{\rm g1}$ will change the negative reactance to a positive reactance jX on the same constant-conductance circle on the Smith chart, the series capacitance C_1 is then used to resonate with jX. The combination of $L_{\rm g1}$ and C_1 transfers R_S to $Z_{\rm opt}$, $L_{\rm g1}$ and C_1 also act as part of the bias network and dc block, respectively.

By using this approach, the required value of $L_{\rm g1}$ is about 0.2∼0.3 nH, which can be practically implemented in Si-based technology at frequency above 20 GHz. A bypass capacitor C_b is added to stabilize the supply voltage $V_{\rm g1}$ and to isolate the noise to it. Thus, no additional bias networks such as large shunt resistors and large dc-block capacitors are required, which leads to a smaller chip size and lower noise figure.

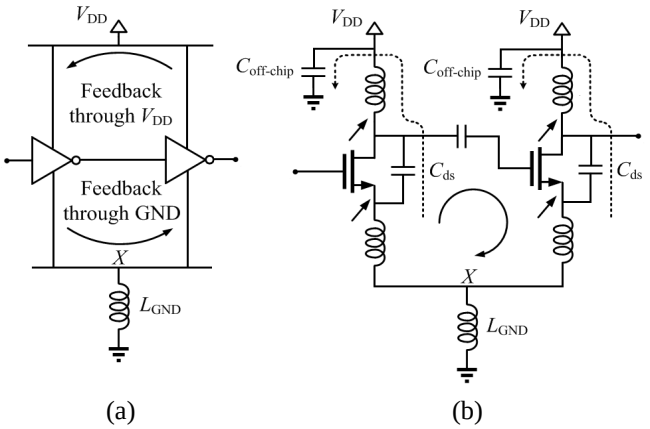


Fig. 7. Stability concern: (a) Feedback through supply loop or nonideal ground, (b) large bypass capacitors are used to quench the oscillation at low frequency.

D. Design of 24 GHz LNA

Since a single transistor does not generate enough gain at high frequencies, the three-stage cascaded common-source structure is proposed as shown in Fig. 6. In the first stage, proper choice of g_{m1} and $C_{\rm gs1}$ of M_1 and $L_{\rm s1}$ are used to shift the input impedance for noise matching. In order to reduce the power consumption, the device size of M_1 should be as samll as possible to reduce the bias current. In this work, M_1 is designed to have 11 fingers with the total gate width of 33 μm, and is biased at 1 V with drain current of 3 mA. Under these conditions, the input impedance $Z_{\rm in}$ is conjugate to $Z_{\rm opt}$. Thus, minimum noise figure, high power gain, low bias current and good input impedance matching (VSWR≃1) are achieved simultaneously.

The shunt inductor $L_{\rm g1}$ and series capacitor C_1 are used to conjugate match the input impedance. Higher gain of the first stage will suppress the noise contribution of the subsequent stage, leading to a better noise performance. In this work, we choose $L_{\rm g1} = 0.28$ nH and $C_1 = 112.3$ fF.

Common-source amplifiers with inductive degeneration are used as the second and the third stages to increase the overall

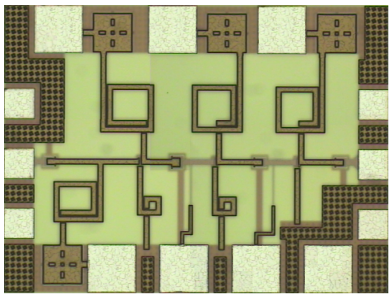


Fig. 8. Die micrograph of the 24 GHz LNA, the chip size is 0.64 mm × 0.48 mm.

gain. The inductors L_{s2} and L_{s3} are connected to the source directly to improve the stability of the circuit. Since increasing the inductance will reduce the amplifier gain, the magnitude of inductance is restricted.

The inter-stage matching network is a high-pass filter consisting of $L_{d1}$and C_2 to achieve conjugate matching between the drain of M_1 and the gate of M_2. Similarly, L_{d2} and C_3 are used to match between the drain of M_2 and the gate of M_3. The output matching network consists of L_{d3} and C_4 to provide conjugate matching with Z_{out}, and C_4 also acts as a dc block. The parasitic capacitance C_{pad} due to the input and output RF pads is included as part of the matching network. The value of C_{pad} depends on the pad size and the metal layers. In this work, The RF pads are implemented with top metal and bottom ground-shielding metal, the value of C_{pad} is about 30 fF. The on-chip bypass capacitors C_b with a value of 4 pF is implemented using the MIM feature.

E. Stability Concern

An LNA design that is nominally stable may oscillate at some unexpectedly high or low frequency due to manufacturing tolerances. The LNA may become unstable due to the feedback through V_{DD} or the feedback between two stages via nonideal ground node X are shown in Fig. 7 (a). To solve the first problem, the voltage supply is separated into V_{D1}, V_{D2} and V_{D3}. However, the amplifier may still become unstable due to the nonideal ground at X. If the start-up conditions are met, low-frequency oscillation will occur at any node in the circuit via C_{ds} as shown in Fig. 7 (b). To overcome possible low-frequency oscillation, off-chip capacitors $C_{off\text{-}chip}$ of 100 nF are shunt at the drain bias networks to bypass these low-frequency signals.

F. Layout Issues

Compared with GaAs substrate, the silicon substrate with low-resistivity will cause severe loss to RF circuits. To operate above 20 GHz, low-loss inductors with small inductance and high self-resonance frequency (SRF) are required. No ground plane is interposed between the inductor and the substrate to avoid reduction in the SRF due to increased parasitic capacitance. In order to reduce the unwanted coupling effects, adjacent inductors are separated by at least 50 μm. Transmission lines L_1-L_5 in Fig. 6 are added for layout consideration. To minimize the resistive loss, the transmission lines L_1-L_5 as well as inductors are placed on the topmost metal layer with 2.34 μm metal thickness.

Moreover, wide transmission line is preferred to reduce the resistive loss. Since wide line increases the parasitic capacitance between the inductor and the substrate, hence the inductors are optimized by trade-off between the resistive and substrate losses using the field simulator Momentum [11].

III. Results and Discussions

The 24 GHz LNA is implemented in the 0.18 μm CMOS technology. Fig. 8 shows the die micrograph of the LNA with an area of 0.64 mm $\times$ 0.48 mm, including pads. The input port and output port of the LNA chip are measured on-wafer using high-frequency probes. The dc supply and ground pads are wire-bonded to the testing board. The S parameters between the input and output ports are measured using an HP 8510 network analyzer. The noise figure is measured using an Agilent N8975A noise-figure meter with a 346C-K01 noise source. Figs. 9 and 10 show the gain and noise figure, respectively. The power gain reaches a maximum of 13.5 dB at 24 GHz with 3-dB bandwidth from 21 to 26 GHz. The noise figure reaches a minimum of 4.7 dB at 24 GHz. The input and output return losses are lower than -10 dB around 24 GHz as shown in Figs. 11 and 12, respectively. The dc power consumption is 8.3 mW at 1 V supply.

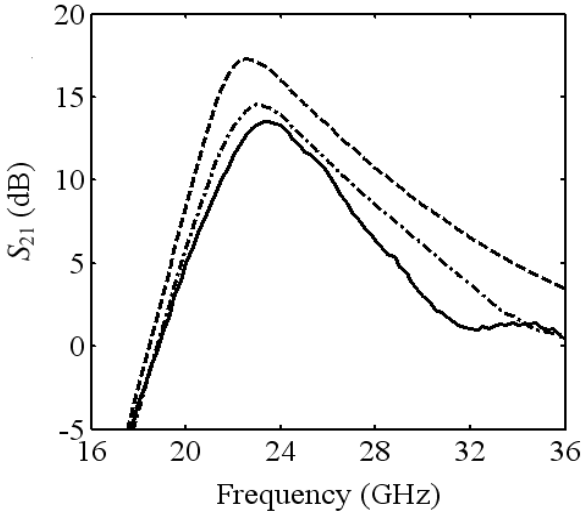


Fig. 9. Power gain of 24 GHz LNA, —: measured S_{21}, - - -: simulated S_{21}, -·-: simulated S_{21} including parasitic capacitances.

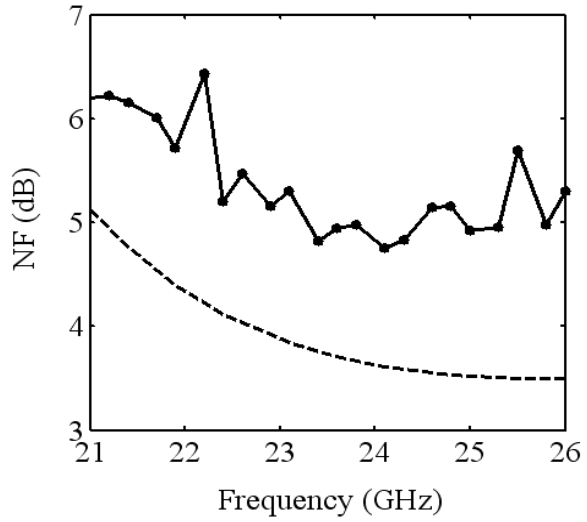


Fig. 10. Noise figure of 24 GHz LNA, –●–: measured, - - -: simulated.

Fig. 13 shows the output power versus the input power of the LNA at 24 GHz. The measured input referred 1-dB

TABLE I
PERFORMANCE OF THE PROPOSED LNA.

Parameter	[4]	[5]	[6]	[7]	[10]	This work
Technology	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	90 nm CMOS	0.18 μm CMOS	0.18 μm CMOS
Supply voltage (V)	1.8	1	1.5	1.5	2	1
Center frequency (GHz)	23.7	24	21.8	20	12-20	24
Maximum gain (dB)	12.86	13.1	15	5.8	7.5	13.5
Noise figure (dB)	5.6	3.9	6	6.4	4	4.7
S_{11}/S_{22} (dB)	$-11/-22$	$-15/-20$	$-21/$--	$-20/-20$	$-10/-10$	$-10/-15$
$P_{1\mathrm{dB}}$ (dBm)	-11.1	-12.2	--	1	--	-7
IIP_3 (dBm)	2.04	0.54	--	3	--	1.3
Circuit topology	CS+CS+CS	CS+CS	CGRF+CS+CS	CS	CS	CS+CS+CS
Power consumption (mW)	54	14	24	10	50	8.3
Chip area (mm $\times$ mm)	1.05 $\times$ 0.7	0.57 $\times$ 0.6	0.2 $\times$ 0.25	0.7 $\times$ 0.8	--	0.64 $\times$ 0.48

CGRF: common-gate resistive feedthrough

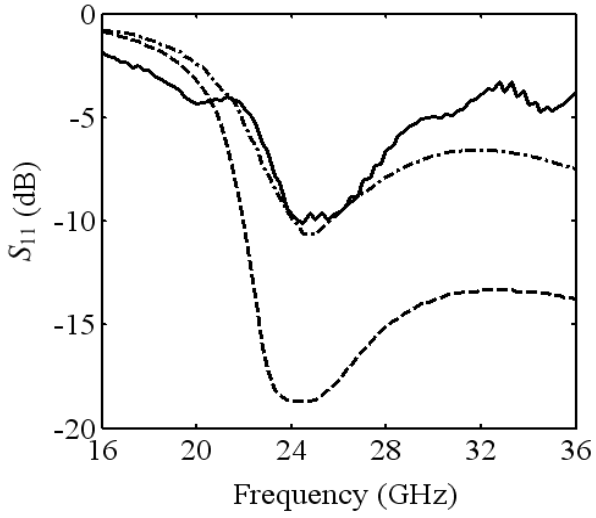


Fig. 11. Input return loss of 24 GHz LNA, —: measured S_{11}, - - -: simulated S_{11}, - · -: simulated S_{11} including parasitic capacitances.

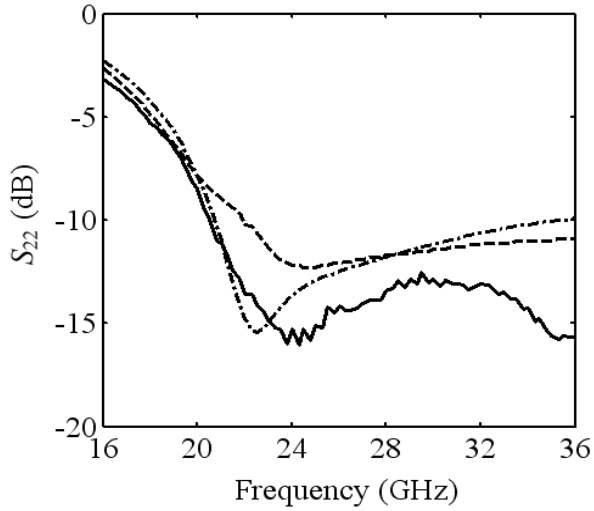


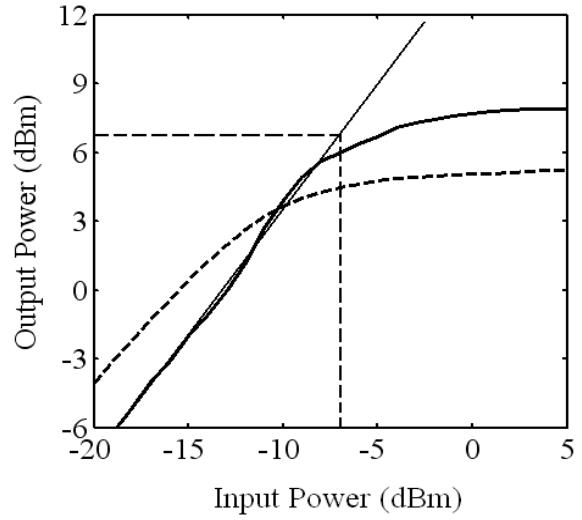
Fig. 12. Output return loss of 24 GHz LNA, —: measured S_{22}, - - -: simulated S_{22}, - · -: simulated S_{22} including parasitic capacitances.

compression ($P_{1\mathrm{dB}}$) is -7 dBm and the simulated IIP_3 is 1.3 dBm. The gate biases V_{g1}, V_{g2} and V_{g3} are tuned to 0.7, 0.75, and 0.8 V, respectively, to increase linearity.

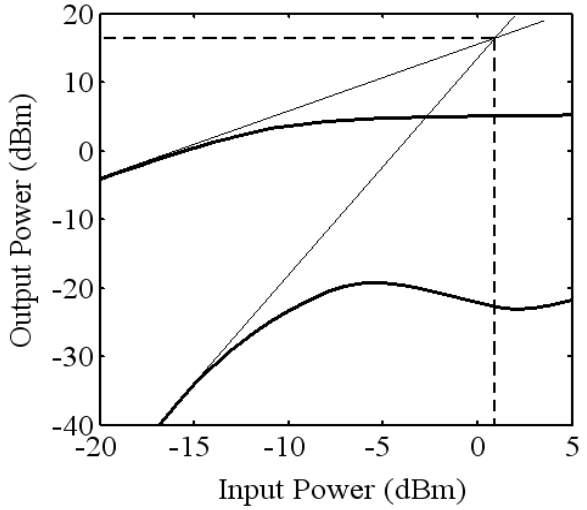
As can be observed, the measured S_{11} differs from the simulated S_{11} by a few dB, and the measured S_{21} is also lower than the simulated S_{21} by a few dB. By careful review of the layout, we suspect that the parasitic effects contributed by the silicon substrate under the transmission lines are the cause. Retrying the substrate parameters such as tanδ and permittivity in the EM simulator, we build equivalent lumped circuits for these transmission lines. As a result, several capacitors are added between the transmission lines and the ground as shown in Fig. 6. After adding these parasitic capacitances, the simulated results fit more closely to the measured results. Part of the deviation between simulation and measurement may be due to the inaccurate active device model which is deducted from the two-port S-parameter measured from 100 MHz to 20.1 GHz [12]. Finally, the performance of the proposed LNA and comparison with the literatures are listed in Table I.

IV. CONCLUSION

A 24 GHz LNA has been fabricated using a standard 0.18 μm CMOS technology. A design method of CMOS LNA is proposed to render R_{opt} close to 50 Ω and $Z_{\mathrm{in}} = Z_{\mathrm{opt}}^{*}$ by using small devices and small currents. This LNA chip achieves a maximum gain of 13.5 dB and a minimum noise figure of 4.7 dB at 24 GHz. The input and output return losses are lower than -10 dB. The supply voltage and supply current are 1 V and 8.3 mA, respectively. The input referred $P_{1\mathrm{dB}}$ and the IIP_3 are -7 dBm and 1.3 dBm, respectively. The chip size is 0.64 mm $\times$ 0.48 mm. Compared to the LNAs around 20



(a)



(b)

Fig. 13. Power amplification of 24 GHz LNA, (a) one-tone result to infer $P_{1\mathrm{dB}}$, —: measured, - - -: simulated, (b) simulated two-tone result to infer IIP_3.

GHz in 0.18 μm CMOS process found in the literatures, this LNA takes the lowest power consumption.

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Dual-band VCO with Switched Inductors for UWB Applications

Wei-Yang Lee, *Student Member, IEEE* and Jean-Fu Kiang, *Member, IEEE*

***Abstract*— A dual-band VCO is designed in a 0.18 μm CMOS process by applying the switched-inductor approach on a single PMOS cross-coupled pair VCO to enable its operation in 3,960 and 7,128 MHz bands. The VCO operates on an 1 V power supply, its phase noise at 1 MHz offset is -113.8 dBc/Hz at 3,960 MHz and -110.2 dBc/Hz at 7,128 MHz. The core VCO consumes 8.95 mW at both bands.**

***Index Terms*— CMOSFETs, phase noise, switched circuit, voltage-controlled oscillator (VCO).**

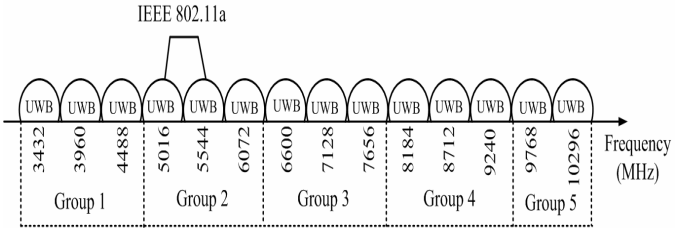

Fig. 1. Frequency allocation of MB OFDM [15].

I. Introduction

The 3.1-10.6 GHz frequency band has been allocated by the Federal Communications Committee (FCC) for the ultra-wideband (UWB) system to enable a high data-rate transmission over the air [15]. Fig.1 shows the frequency allocation of the multi-band orthogonal frequency-division multiplex (MB OFDM) approach. There are 14 bands organized into five groups, with each band covering 528 MHz. The first four groups contain three bands each, and the last group contains two bands. The operation within the first group is mandatory, and all the other groups are optional. Note that the 5-6 GHz band has also been allocated for wireless local area network (WLAN).

The voltage-controlled oscillators (VCOs) are key components of an UWB system. VCOs are widely used as CW signal generator in a phase-locked loop (PLL) based frequency synthesizer. Though multiple VCOs can be used to generate signals in multiple frequency bands, using a single multiband VCO is desirable to reduce chip area and cost [1].

In designing a VCO, there is usually a trade-off between phase noise and dc power consumption. Other factors include the center frequency of oscillation, tuning range and output power level.

By employing a PMOS cross-coupled pair with a capacitive feedback, a significant improvement in phase noise and output swing can be achieved [2]. In [3], a balanced Hartley VCO is presented, and a π-network is implemented to provide the required $180°$phase shift for the feedback signal. In [4], a Hartley differential CMOS VCO with a large-resistance element is applied to supress the even mode. In [5], a 90 GHz VCO is designed with the ring-coupled quad, and is fabricated in a 90 nm CMOS process. This ring-coupled quad takes four-stage common-source transistors to create a higher open-loop gain.

In [6] and [7], current-reuse structure like frequency multiplier is embedded in VCO to lower the power consumption. In [8], a differential Colpitts oscillator is designed to have a high gain while maintaining low phase noise due to its cyclostationary noise properties. In [9], a varactor architecture is proposed to the differential control line of a VCO to achieve large CMRR. In [10], the NMOS cross-coupled pair is used with the buffer composed of shunt inductors to increase the output power. In [11], a 40 GHz wideband VCO is implemented in a 0.18 μm CMOS technology, designed based on a non-uniform standing-wave VCO with a switched transmission-line architecture in order to achieve a wide tuning range. In [12], a complementary cross-coupled differential structure is used to achieve a higher transconductance. To avoid large process variation of load resistors, PMOS transistors are used as the loads of the buffer. In [13], a 3-D LC VCO incorporating metal-6 on-chip inductors is implemented in a 0.18 μm 1P6M CMOS technology to increase the Q factors and halve the die area. In [14], switched-inductor technique is used to designed a dual-band oscillator, but the usage of asymmetrical switched-inductor raises the phase noise.

In this paper, a daul-band voltage-controlled oscillator is proposed for the MB OFDM system. A symmetrical switched-inductance instead of a switched capacitor is used to switch the oscillator frequency. A switched inductor can replace more switched capacitors to reduce the phase noise, since the latter requires more MOS switches hence generates more phase noise.

II. Circuit Design

Fig.2 shows the architecture of the frequency synthesizer complying with MB OFDM. Two PLLs are used with the common reference clock of 33 MHz. One PLL locks the main VCO at 3,960 MHz or 7,128 MHz, and the other PLL locks the slave VCO at 528 MHz. When the frequency of the main VCO is 3,960 MHz, the single-sided band (SSB) mixer can generate 3,432 MHz and 4,488 MHz signals which are the other two bands in group 1. When the frequency of the main VCO is 7,128 MHz, the single-sided band (SSB) mixer can generate 6,600 MHz and 7,656 MHz signals in group 3. The

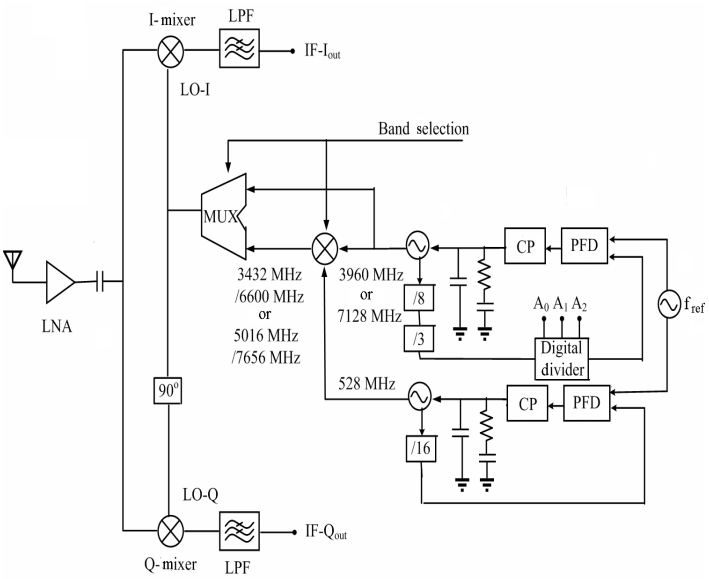

Fig. 2. Architecture of UWB receiver complying with MB OFDM.

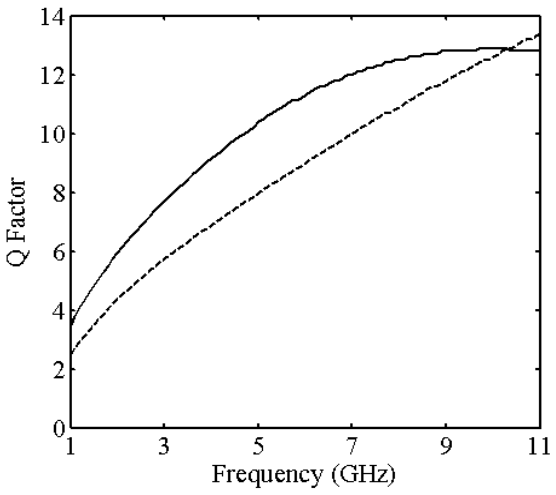

Fig. 4. Q-factor of L_1 to L_4, —: L_3, L_4, - -: L_1, L_2

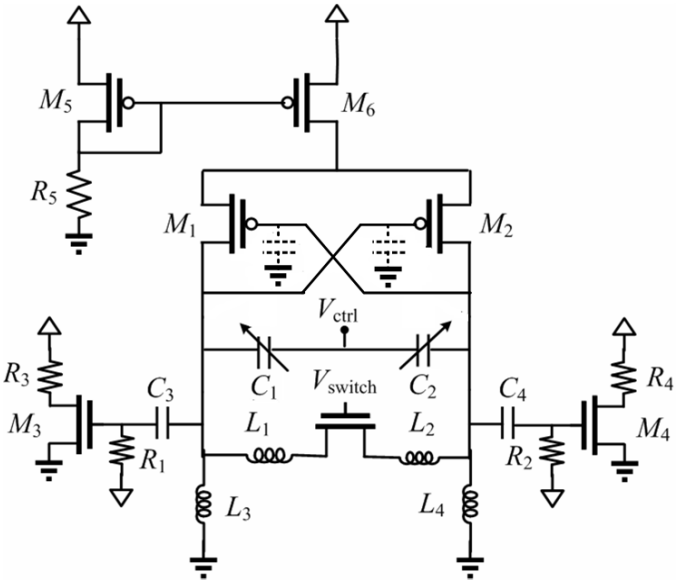

Fig. 3. Schematic of the dual-band VCO with switched inductors.

dual-band VCO has the advantages of reduced die size and cost because fewer PLLs are required.

Fig.3 shows the proposed dual-band VCO with switched inductors. The PMOS cross-coupled pair is composed of the transistors M_1 and M_2. Although the NMOS transistors have smaller size than the PMOS transistors to achieve the same g_m, the PMOS transistors provide lower $1/f$ noise and lower hot-carrier induced white noise compared to NMOS transistors.

The current mirror is composed of the transistors M_5, M_6 and the resistor R_5. The large resistance provided by M_5 maintains the Q factors of the LC-tank. The swithed-inductor approach can reduce the number of MOS switches as in conventional switched-capacitor approach, thus the former approach renders lower phase noise of the oscillator.

When the switch is off, the lower oscillator frequency is determined by C_1 and L_3 as

$$f_{o,\text{off}} = \frac{1}{2\pi\sqrt{L_3 C_1}}$$

When the switch is on, the higher oscillator frequency is determined by C_1, L_1 and L_3 as

$$f_{o,\text{on}} = \frac{1}{2\pi\sqrt{L_{\text{on}} C_1}}$$

where $L_{\text{on}} = L_3 \parallel L_1$. Note that placing a switch between the differential nodes halves the switch size compared to that the single-ended counterpart.

The inductors L_3 and L_4 need no headroom, hence the voltage swing amplitude can be increased to reduce the phase noise. The buffers are composed of the resistors R_1, R_2, R_3, R_4, and the NMOS transistors M_3, M_4. The capacitors C_3 and C_4 are used as dc block.

The phase noise of an LC-VCO can be expressed as [16]

$$\text{PN}(f_o) = \frac{2kTR_{\text{eq}}F}{V_s^2}\left(\frac{f_o}{2Q\Delta f}\right)^2\left(1+\frac{\Delta f_{1/f^3}}{\Delta f}\right) \qquad (1)$$

where f_o is the oscillator frequency, Δf is the offset frequency, Q and R_{eq} are the quality factor and equivalent resistance, respectively, of the LC tank, V_s is voltage swing amplitude, F is the excess noise factor, and $\Delta f_{1/f^3}$ is the corner frequency of the flicker-noise spectrum. The phase noise is inversely proportional to the quilty factor. Since the quilty factor of a capacitor is usually high enough in the UWB band, the quality factor of the LC-tank is thus determined by the that of the inductor.

Fig.4 shows the quality factor of the inductors used in the design. The quality factor of L_3 and L_4 is 9.08 at 3,960 MHz and 12.1 at 7,128 MHz. That of L_1 and L_2 is 6.85 at 3,960 MHz and 10.1 at 7,128 MHz.

Fig.5(a) shows the circuit model of switch at the off state, where C_{db} is the drain-to-substrate capacitance and C_{gd} is the drain-to-gate capacitance. The drain-to-substrate resistance

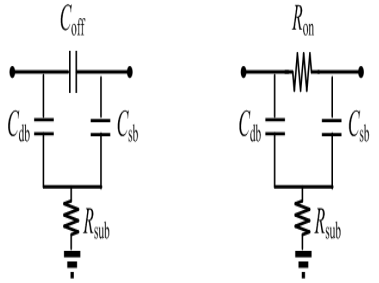

Fig. 5. Circuit model of switch (a) at off state, (b) at on state.

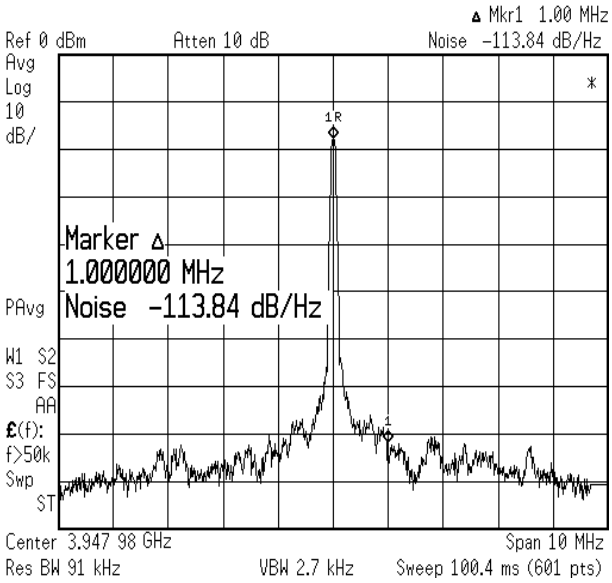

Fig. 6. Measured phase noise of the oscillator around 3,960 MHz.

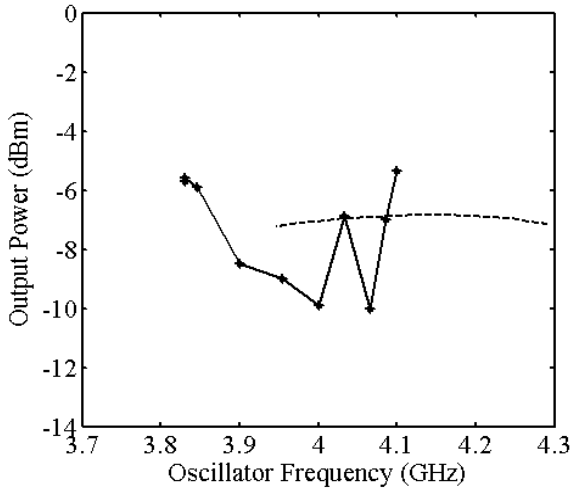

Fig. 7. Output power of the oscillator, —: measurement, - - -: simulation.

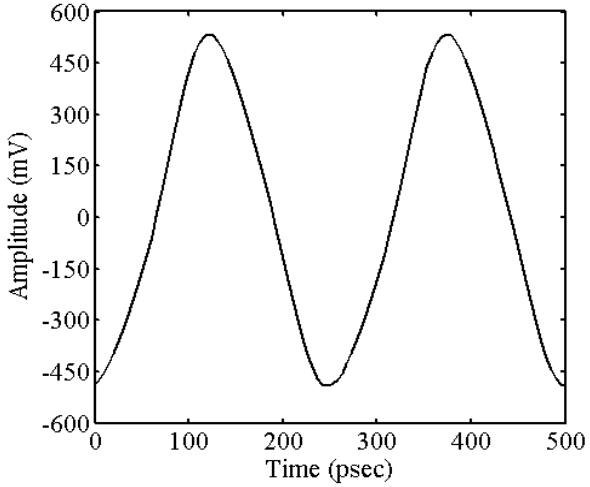

Fig. 8. Simulated output waveform of the oscillator at 3,960 MHz.

$R_{\rm sub}$ in series with $C_{\rm db}$ will reduce the Q factor of the capacitor. Fig.5(b) shows the circuit model of the switch at the on state. In order to increase tunability, $C_{\rm db}$ and $C_{\rm gd}$ should be made smaller. However, when the transistor is designed narrower, its finite on-resistance $R_{\rm on}$ will increase and boost the tank loss.

III. Results and Discussions

Fig.6 shows the measured phase noise of the oscillator at 3,960 MHz, and the phase noise at 1 MHz offset is -113.8 dBc/Hz. Fig.7 shows the output power of the oscillator, and the output power is -8.5 dBm at 3,960 MHz. Fig.8 shows the simulated output waveform of the oscillator at 3,960 MHz. Fig.9 shows the tuning range around 3,960 MHz. The dash-dot curve is the simulation result including the parasitic capacitance of layout near the gates of M_1 and M_2. The tuning range is about 8%.

Fig.10 shows the measured phase noise of the oscillator at 7,128 MHz, and the phase noise at 1 MHz offset is -110.2 dBc/Hz. Fig.11 shows the output power of the oscillator, and the output power is -7.7 dBm at 7,128 MHz by simulation. Fig.12 shows the simulated output waveform of the oscillator at 7,128 MHz. Fig.13 shows that the tuning range around 7,128 MHz is about 10.5%.

The core VCO with $V_{\rm dd} = 1$ V takes 8.95 mA of current and consumes 8.95 mW of power. The buffer with $V_{\rm dd} = 1.8$ V takes 4.47 mA of current and consumes 16.092 mW of power. The die micrograph is shown in Fig.14, and the chip size is 0.85×0.65 mm^2.

We choose the figure of merit (FOM) for VCO as defined in [1]

$$\mathrm{FOM} = \mathrm{PN}(\Delta f) - 20\log\left(\frac{f_o}{\Delta f}\right) + 10\log\left(\frac{P_{\rm dc}}{1\ \mathrm{mW}}\right) \quad (2)$$

where $\mathrm{PN}(\Delta f)$ is the phase noise at an offset Δf from the carrier frequency f_o, $P_{\rm dc}$ is the VCO power consumption in mW. The FOM of the proposed VCO is 180.6 dB at 3,960

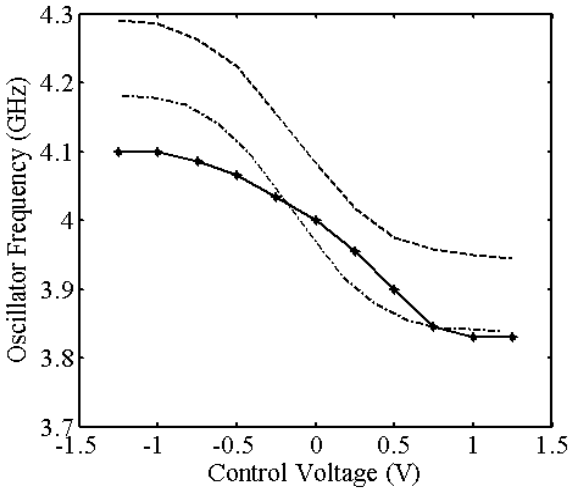

Fig. 9. Tuning range at 3,960 MHz, —-: measurement, - - -: simulation, - .- .-: simulation including parasitics.

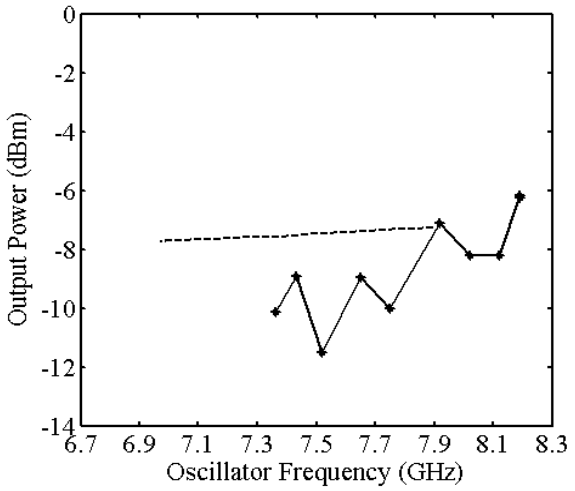

Fig. 11. Output power of the oscillator, —-: measurement, - - -: simulation.

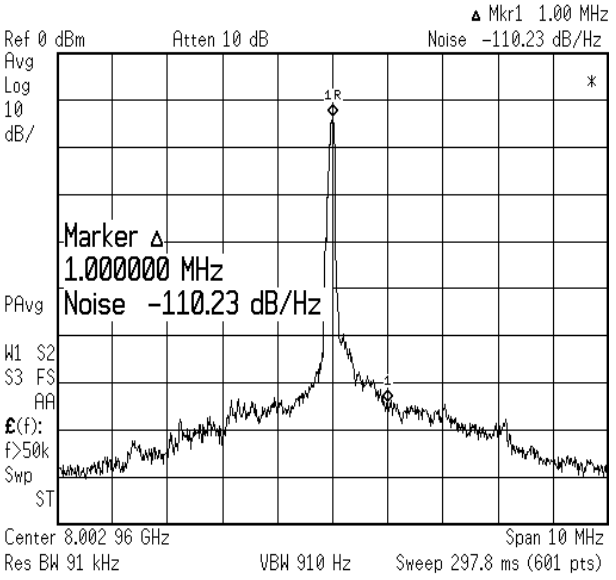

Fig. 10. Measured phase noise of the oscillator around 7,128 MHz.

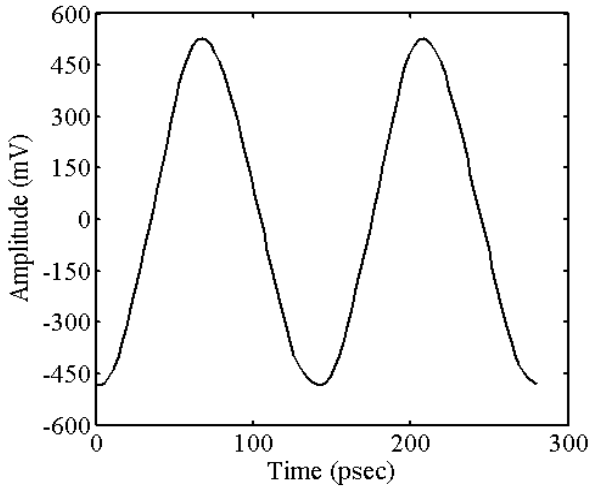

Fig. 12. Simulated output waveform of the oscillator at 7,128 MHz.

MHz and 185.2 dB at 7,128 MHz.

Finally, the performance of the proposed design will be compared with those in the literatures. The design in [1] creates less phase noise, but the proposed VCO has a smaller chip size. Compared with 32 mW in [2], the proposed VCO consumes less power. The design in [3] consumes less power of 4.2 mW, but the proposed VCO has a smaller chip size. Compared with [4], the proposed VCO can provide two frequency bands instead of one in [4]. The design in [6] consumes less power as 0.97 mW, but the proposed VCO creates less phase noise.

The design in [7] consumes less power of 0.59 mW, but the proposed VCO has a smaller chip size. The design in [8] creates less phase noise as -120 dBc/Hz at 1 MHz offset, but its power consumption is 12.6 mW, higer than the proposed VCO. The design in [10] consumes less power of 0.69 mW, but its phase noise is -97 dBc/Hz at 1 MHz offset, higher than the proposed VCO. The power consumption and phase noise in [11] are 27 mW and -99 dBc/Hz at 1 MHz offset, respectively, the proposed VCO consumes less power and creates less phase noise. The design in [12] consumes more power of 49.97 mW, but it has a smaller chip size than the proposed VCO.

In summary, the proposed dual-band VCO with switched inductors consumes less power than those in [2], [5], [8], [11], [12], [13], and has a smaller chip size than those in [1], [3], [7]. The phase noise of the proposed VCO is lower than those in [6], [9], [10], [14].

IV. Conclusion

A novel dual-band VCO with switched indutors is designed and fabricated in a 0.18 μm CMOS process. The swithed-inductor approach reduces the phase noise by reducing the

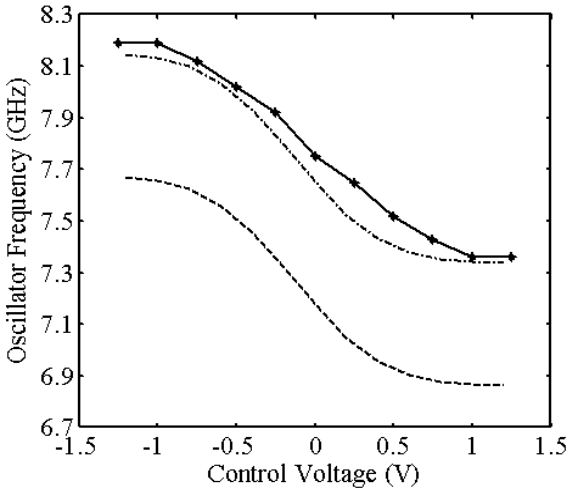

Fig. 13. Tuning range at 7,128 MHz, —-: measurement, - - -: simulation, -.- .-: simulation including parasitics.

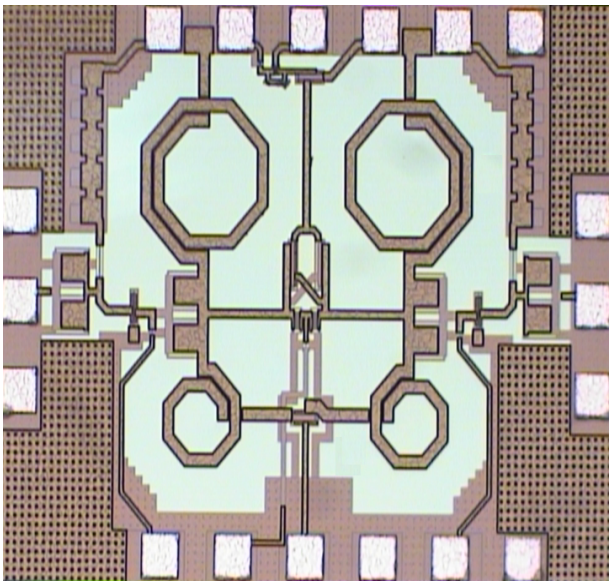

Fig. 14. Die micrograph of the proposed dual-band VCO.

number of transistors. The proposed VCO can generate two bands centered at 3,960 MHz and 7,128 MHz, respectively.

The core VCO consumes 8.95 mW, the phase noise at 1 MHz offset is -113.8 dBc/Hz at 3,960 MHz and -110.2 dBc/Hz at 7,128 MHz. The FOMs are 180.6 dB and 185.2 dB at 3,960 MHz and 7,128 MHz, respectively. The tuning ranges are 8% at 3,960 MHz, and 10.5% at 7,128 MHz. The chip size is $0.85 \times 0.65\ \mathrm{mm}^2$.

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Active and Adaptive Charging Method on Data Lines for Delay Compensation

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***Abstract*— Charging time is a critical constraint in the design of large-size or high-resolution liquid crystal display (LCD). A fast charging method is proposed to generate adaptive charging voltages by comparing the pixel values between previous and current frames. Data line segmentation is also proposed to charge different subpixels on the data line precisely, which is implemented by using operational amplifiers and resistor networks.**

***Index Terms*— LCD driver, TFT LCD, display.**

I. Introduction

High-resolution TV has more rows to charge in one frame time, thus the available charging time for each row is shorter than that for standard TV. The voltage levels on data lines change with the picture content, and such change must be completed during the allocated charging period. If the voltage levels on a data line are significantly different between two consecutive frames, precharge method is usually used to shorten the charging time.

In [1], the charging period for a data line is divided into two phases, a voltage higher than needed is applied during the precharge phase, then the data voltage is applied during the fine-tune phase. However, when the voltage levels of one pixel in two consecutive frames are close, this precharge method may over-charge this pixel. Since the precharge voltage is fixed, the fine-tune phase must be long enough if the voltage difference is large.

In [2], the charging period is divided into the precharge phase and the fine-tune phase as in [1]. Apply the voltage corresponding to the highest gray level during the precharge phase and apply the data voltage during the fine-tune phase. The higher the pixel gray level is, the longer the precharge phase takes, and vice versa. Similar to [1], when the previous gray level is significantly different from the current one, the fine-tune may not be complete in time.

In [3], a line time extension method is proposed to extend the equivalent charging time for a pixel. Two adjacent rows are pulled up at the same time. After a charging time of T_{row}, the scan line of the first row is pulled down and the data voltage is applied to the second row. This method can effectively extend the charging time. However, if the data on two adjacent rows differ too much, the fine-tune phase may not be sufficient for the second row.

In [4], a frame buffer is used to store the previous frame, and a look-up table is used to generate the over-drive voltage by comparing the previous frame and the current one. This method can charge the pixel faster but not very precisely. In [5], the charging period for a data line is divided into the precharge phase and the fine-tune phase, and a look-up table is used to generate the precharge voltage. This method has the same drawbacks as [4].

In [6], an over-drive voltage is calculated by using a VGA chip, based on the data line voltages. It has the same drawbacks as conventional over-drive method. The scan-line delay near the scan driver is shorter than that away from it, due to the resistive and capacitive loads contributed by the data lines.

In [7], the panel is split into an upper part and a lower part, with separate data driver serving each part. The signal delay on a data line can thus be reduced by half. This method requires a memory to store one frame of data before sending to the two data drivers.

In these precharging methods, the charging period is divided into a precharge phase followed by a fine-tune phase. A fixed voltage is applied in the precharge phase, and the data voltage is applied in the fine-tune phase. If a buffer is used to store the previous frame, the fine-tune phase can be executed more efficiently with the additional load of computing the voltage difference between two consecutive frames.

In this paper, we propose an active and adaptive charging method to charge the LCD panel fast by comparing the previous and the current frames of data to generate the charging voltage. A resistor network is implemented to compare the voltages sent to the operational amplifier to compensate for the data-line delay at different distances from the data driver.

II. Design Approach

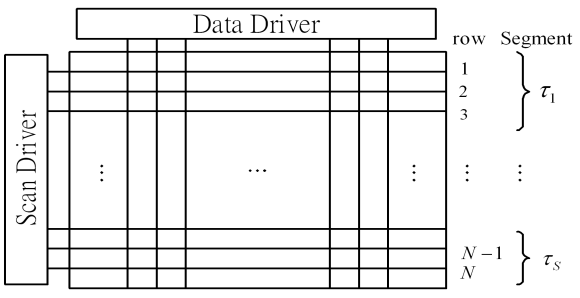

Fig. 1. Segmentation of data lines.

Without loss of generality, a 60” LCD with full HD resolution of 1,920 × 1,080 will be considered throughout this paper. To charge data lines more precisely, a data line serving 1,080 subpixels is divided into multiple segments, as shown in Fig.1.

TABLE I
PARAMETERS OF 40" FULL HD TFT-LCD [3].

Parameter	Value
resolution	1,920 × 1,080
pixel size (μm^2)	151 × 454
resistance of vertical line (kΩ)	18
capacitance of vertical line (pF)	276
resistance of horizontal line (kΩ)	5
capacitance of horizontal line (pF)	480
pixel capacitance (pF)	1.35
LCD mode	TN

Define the charging ratio as the ratio between the charged voltage and the intended voltage. For example, if the intended voltage at a pixel is 6 V and the pixel voltage reaches 5.5 V at the end of the charging period, the charging ratio will be $5.5/6 = 0.917$.

Based on the signal line model consisted of infinitesimal RC segments, the voltage waveform on a data line or a scan line can be expressed as

$$\frac{v\left(z,t\right)}{V_d} \simeq 1 - \frac{4}{\pi}\exp\left(-\frac{\pi^2 t}{4RCz^2}\right) \tag{1}$$

where R and C are the per-unit-length resistance and capacitance, respectively, along the line, V_d is the intended voltage, and $v\left(z,t\right)$ is the voltage on the line at time t and at a distance z from the source. To reach the charging ratio of 0.995, the delay time will be $T_{0.995} = 2.245RCz^2$.

In general, the delay time for the voltage at z to reach the charging ratio α is approximately

$$T_\alpha\left(z\right) = -\frac{4RCz^2}{\pi^2}\ln\frac{\pi\left(1-\alpha\right)}{4} \tag{2}$$

Since the signal line can be viewed as a cascade of infinitesimal resistive and capacitive loads, the signal line from the driver at $z = 0$ to any subpixel location z can be modeled as an equivalent RC circuit with an effective time constant $\tau_\alpha\left(z\right)$ which can be expressed in terms of $T_\alpha\left(z\right)$ as

$$\begin{aligned}\tau_\alpha\left(z\right) &= \frac{T_\alpha\left(z\right)}{-\ln(1-\alpha)} \\ &= \frac{4RCz^2}{\pi^2\ln\left(1-\alpha\right)}\ln\frac{\pi\left(1-\alpha\right)}{4}\end{aligned} \tag{3}$$

Since no data of line resistance and capacitance are available for a 60" LCD panel with full HD resolution, we assume the per-unit-length resistance and capacitance of the 60" LCD panel are the same as those of the 40" LCD panel. Table I lists the parameters of a 40" TFT-LCD with full HD resolution. The length of a scan line is $\ell = 1,920 \times 151\mu \times 3 = 86.976$ cm, hence $R = 5/0.86976 = 5.7487\mathrm{k\Omega/m}$, $C = 480/0.86976 = 551.876\mathrm{pF/m}$. The length of a data line is $\ell = 1,080 \times 454\mu = 49.032$ cm, hence $R = 18/0.49032 = 36.71\mathrm{k\Omega/m}$, $C = 276/0.49032 = 562.897\mathrm{pF/m}$.

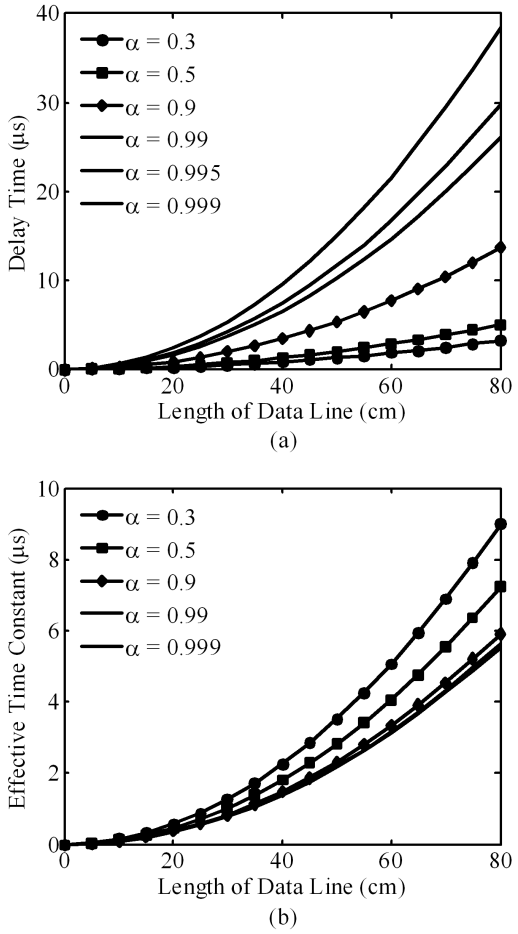

Fig. 2. (a) Delay time T_α, and (b) effective time constant τ_α, along a data line.

Figs.2(a) and 2(b) show the delay time $T_\alpha\left(z\right)$ and the effective time constants $\tau_\alpha\left(z\right)$, respectively, at different charging ratios. It is observed that $\tau_\alpha\left(z\right)$ is insensitive to α, especially when α is closed to unity. In practical applications, the value of α is chosen to be greater than 0.995 to have high fidelity. Thus, we may set $\tau_\alpha\left(z\right) = \tau\left(z\right)$.

The time allocated for displaying each row is

$$T_{\mathrm{row}} = \frac{1}{\text{frame rate}} \times \frac{1}{\text{number of rows}} \times \left(1 - \alpha_{\mathrm{sync}}\right)$$

where α_{sync} is the fraction of time reserved for horizontal sync. When the data line is being charged, the transistors on the designated row must be turned on by sending a pulse along the associated scan line. The pixels will wait for $t_{\mathrm{d,scan}}$ before the pulse arrives, where $t_{\mathrm{d,scan}}$ is the delay on scan line which can be calculated using (2). Note that $t_{\mathrm{d,scan}}$ of the farthest pixel from the scan driver must be shorter than T_{row} to have enough margin. Since the loading effect of a single pixel on a data line is negligible, the available charging time is $T_{\mathrm{charge}} = T_{\mathrm{row}}$.

The signal delay is longer for those subpixels which are farther from the data driver, and is shorter for those which

are closer to the data driver. The effective time constant for the subpixels in segment s can be approximated by a constant τ_s at certain point $z = \ell_s$ in segment s at which the voltage waveform is

$$v_s(t) = [v_s(\infty) - v_s(0+)]\left(1 - e^{-t/\tau_s}\right) + v_s(0+) \quad (4)$$

where $v_s(t)$ is the voltage at time t, $v_s(\infty)$ is the intended voltage, and $v_s(0+)$ is the initial voltage.

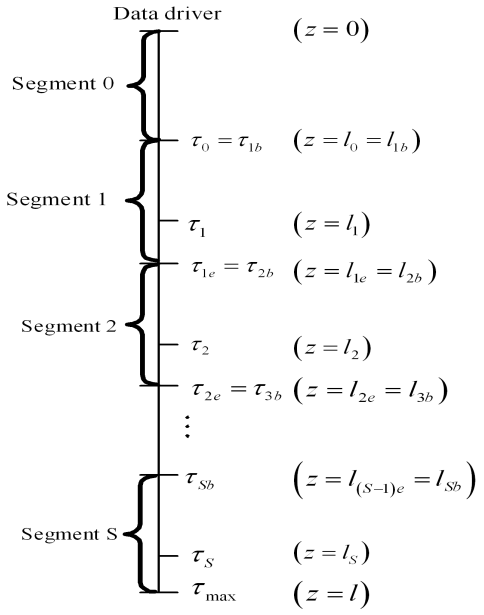

Fig. 3. Segmentation plan of a data line.

Fig. 3 shows the segmentation plan of a data line. Segment 0 ($0 \le z \le \ell_0$) is close enough to the data drive so that no active charging is required. Segment 1 ($\ell_{1b} \le z \le \ell_{1e}$) lies next to segment 0 so that $\ell_{1b} = \ell_0$. The effective time constant in segment 1 is approximated as a constant τ_1 for the ease of implementation. The value of τ_1 is chosen so that the voltage level at $t = T_{\text{charge}}$ at $z = \ell_{1b}$ is $1 - \alpha$ above the intended level. The other end point $z = \ell_{1e}$ is chosen so that its voltage level at $t = T_{\text{charge}}$ is $1 - \alpha$ below the intended level. The parameters in the next segment are then determined in the same way.

The applied voltage $v_{\text{d,amp}}$ is determined by letting $v_s(T_{\text{charge}}) = v_{\text{d,now}}$, $v_s(\infty) = v_{\text{d,amp}}$, $v_s(0+) = v_{\text{d,pre}}$ in (4) to have

$$v_{\text{d,amp}} = \frac{1}{1 - e^{-T_{\text{charge}}/\tau_s}} v_{\text{d,now}} - \frac{e^{-T_{\text{charge}}/\tau_s}}{1 - e^{-T_{\text{charge}}/\tau_s}} v_{\text{d,pre}} \quad (5)$$

where $v_{\text{d,pre}}$ and $v_{\text{d,now}}$ are the voltage levels of the previous and the current frames, respectively. The subpixel at $z = \ell_s$ reaches the charging ratio of exactly 100% at $t = T_{\text{charge}}$.

The data line from $z = 0$ to $z = \ell_0$ does not require active charging because its voltage level can exceed the specified charging ratio α at T_{charge}. To find the time constant τ_0 at $z = \ell_0$, let

$$\Delta V\left(1 - e^{-T_{\text{charge}}/\tau_0}\right) = \alpha \Delta V$$

or

$$\tau_0 = \frac{-T_{\text{charge}}}{\ln(1 - \alpha)} \quad (6)$$

where ΔV is the difference of voltage between two consecutive frames.

At the specified charging ratio α, the maximum allowable deviation of voltage level in segment s occurs at both ends, $z = \ell_{sb}$ and $z = \ell_{se}$. At $z = \ell_{sb}$, the voltage level is $(1 - \alpha)\Delta V$ too high, namely,

$$v_{\text{d,amp}}\left(1 - e^{-T_{\text{charge}}/\tau_{sb}}\right) - \Delta V = (1 - \alpha)\Delta V$$

or

$$\tau_s = \frac{-T_{\text{charge}}}{\ln\left(\dfrac{1 - \alpha + e^{-T_{\text{charge}}/\tau_{sb}}}{2 - \alpha}\right)} \quad (7)$$

At $z = \ell_{se}$, the voltage level is $(1 - \alpha)\Delta V$ too low, namely,

$$\Delta V - v_{\text{d,amp}}\left(1 - e^{-T_{\text{charge}}/\tau_{se}}\right) = (1 - \alpha)\Delta V$$

or

$$\tau_{se} = \frac{-T_{\text{charge}}}{\ln\left(1 - \alpha + \alpha e^{-T_{\text{charge}}/\tau_s}\right)} \quad (8)$$

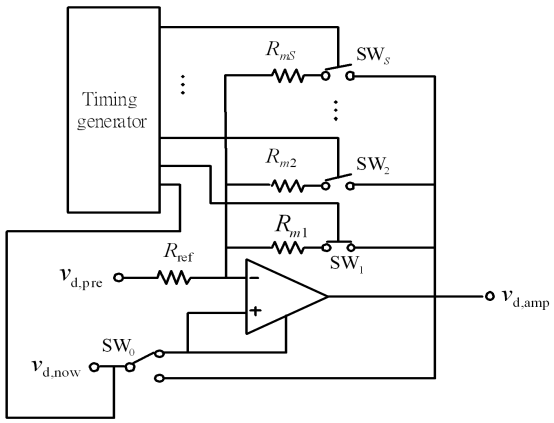

Fig. 4. Operational amplifier with resistor network and switches for data line m.

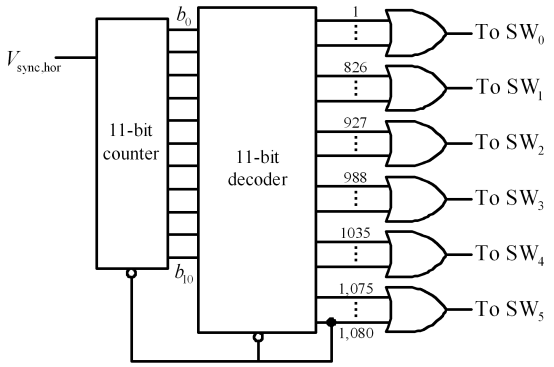

Fig. 5. Timing generator which is reset when scan line 1,080 is on, and changes switch when scan line 826, 927, 988, 1035 or 1075 is on.

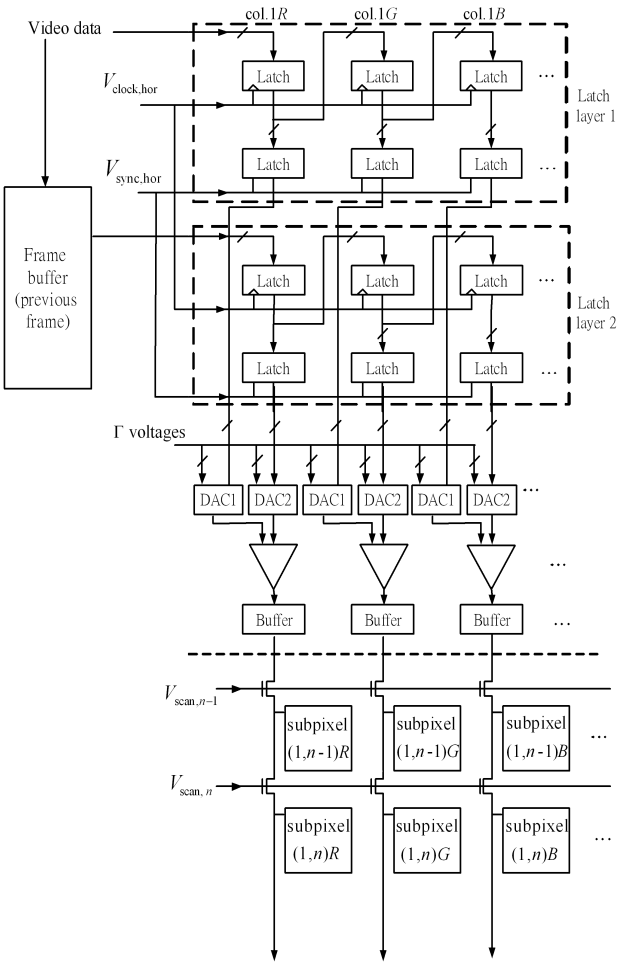

Fig. 6. Active charging circuit on data lines with frame buffer.

To determine the parameters in Fig.3, first calculate τ_0 using (6), then calculate τ_1 by setting $s = 1$ and $\tau_{1b} = \tau_0$ in (7), τ_{1e} is then obtained from (8) by setting $s = 1$, and so on. Based on (3), the distance from the data driver is related to τ as

$$z = \sqrt{\frac{\tau(z)\,\pi^2 \ln(1-\alpha)}{4RC \ln\dfrac{\pi(1-\alpha)}{4}}}$$

Fig. 4 shows the circuit of an operational amplifier to generate the voltage $v_{\mathrm{d,amp}}$. A resistor network is required to implement the S sets of coefficients in (5). When switch SW_s is closed, the output voltage on data line m becomes

$$v_{\mathrm{d,amp}} = v_{\mathrm{d,now}}\left(1 + \frac{R_{\mathrm{ref}}}{R_{ms}}\right) - v_{\mathrm{d,pre}}\frac{R_{\mathrm{ref}}}{R_{ms}} \qquad (9)$$

By comparing (9) and (5), the resistance R_{ms} can be determined as

$$\frac{R_{ms}}{R_{\mathrm{ref}}} = \frac{1 - e^{-T_{\mathrm{charge}}/\tau_s}}{e^{-T_{\mathrm{charge}}/\tau_s}} = e^{T_{\mathrm{charge}}/\tau_s} - 1 \qquad (10)$$

Fig. 5 shows the circuit of timing generator designed to change switches in the circuit of Fig. 4 to fulfill the charging ratio of 0.995 for a 60" LCD panel with full HD resolution. In this case, the pixels from rows 1 to 825 do not need active charging, thus the data voltage is sent via SW_0 to the data line. In charging the pixels from rows 826 to 926, the data voltage is sent via SW_1, and the output voltage is determined by resistance R_1 and R_{ref} as in (9), and so on.

TABLE II
PARAMETERS OF SEGMENTS AT CHARGING RATIO OF 0.995.

Segment	τ_s (μs)	R_s/R_{ref}	Subpixel
0	–	–	$1 \sim 825$
1	3.1821	99.501	$826 \sim 926$
2	3.7404	49.502	$927 \sim 987$
3	4.1658	32.836	$988 \sim 1,034$
4	4.5295	24.503	$1,035 \sim 1,074$
5	4.8566	19.504	$1,075 \sim 1,080$

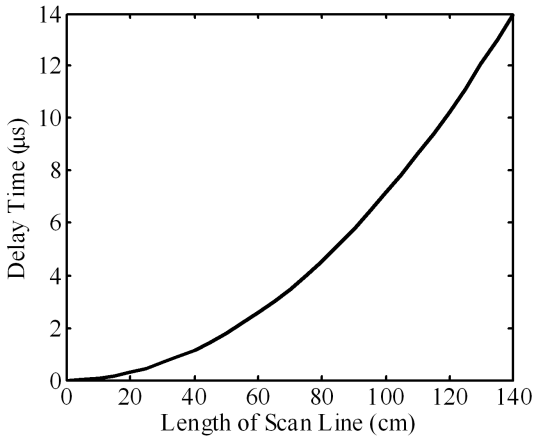

Fig. 7. Delay time on scan line with $\alpha = 0.995$.

Fig.6 shows the driver circuit with a frame buffer to charge data lines. The data in the previous frame is stored in the buffer to be compared with the data in the current frame to calculate the voltage to be sent to the data lines.

Each time a rising edge of $V_{\mathrm{sync,hor}}$ arrives, the first stage of latch layer 1 receives one subpixel data of the current frame, and the first stage of latch layer 2 receives the subpixel data of the previous frame from the frame buffer. When the next $V_{\mathrm{sync,hor}}$ arrives, the second stage of latch layer 1 will receive the first row of data of the current frame, and the second stage of the latch layer 2 will receive the first row of data of the previous frame. The data stored in these stages are then sent to DAC 1 and DAC 2, respectively, to be transformed to the voltage inputs for the operational amplifiers to determine the output voltages for all the data lines.

III. DESIGN EXAMPLES

In the standard HDTV, the frame rate is 60 Hz, thus the frame period is $1/60 = 16.67$ ms. With resolution $1,920 \times 1,080$, each row is allocated a period $T_{\mathrm{row}} = (1/60/1,080) \times 0.95 = 14.67\mu$ s, where $\alpha_{\mathrm{sync}} = 0.05$.

Fig.7 shows the delay time on the scan line with the charging ratio $\alpha = 0.995$. Based on (2), the maximum delay

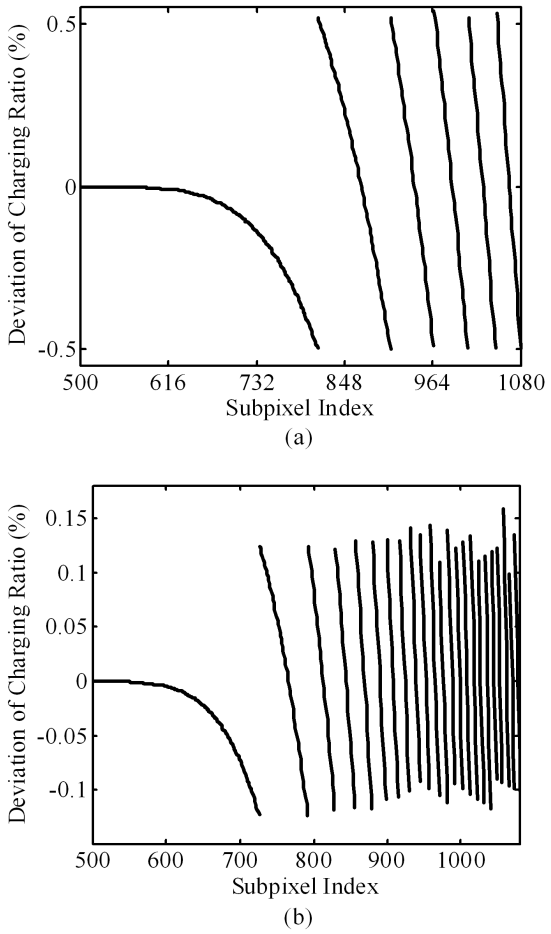

Fig. 8. Deviation of charging ratio along a data line, (a) $\alpha = 0.995$ and (b) $\alpha = 0.999$.

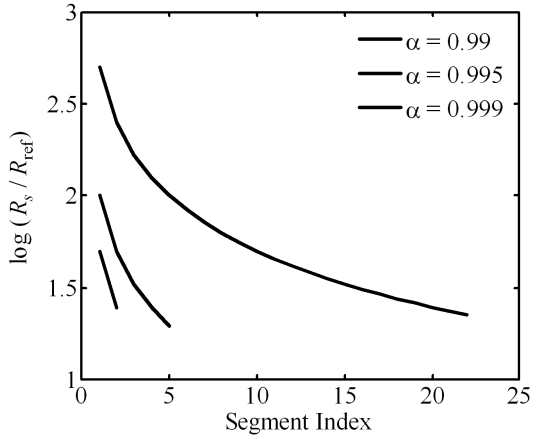

Fig. 9. Resistance of resistor network.

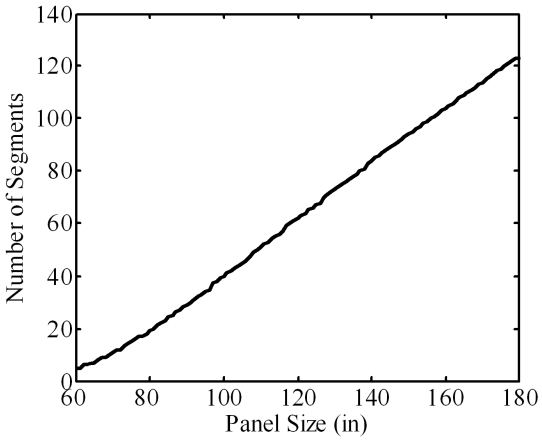

Fig. 10. Number of segments required for different panel sizes at $\alpha = 0.995$.

time on a scan line at the charging ratio of 0.995 is about 14 μs, too close to $T_{\rm row} = 14.67\mu$s. If both ends of the scan line are driven simultaneously by the scan driver, then the maximum scan-line delay of about 4.4 μs will occur at the middle of the sacn line, thus the delay time along the scan line will not prevent any pixel from being turned on early enough.

If the LCD is changed from white to black, the data voltage is changed from 0 to 6 V, rendering $\Delta V = 6$ V. By using conventional method, the voltage on the last subpixel of each data line can only reach 5.7 V at 14.67 μs, which accounts to 13 gray levels of error. On the other hand, the active charging voltage to charge a subpixel from 0 to 6 V is 6.306 V, and the voltage on the subpixel reaches 5.99 V at 14.67 μs, with the error of 0.413 gray level.

Table II lists the effective time constant and the subpixel range of each segment at the charging ratio of 0.995. Applying the segmentation plan, each data line is divided into six segments, and the resistance ratios are determined using (10). The switches are controlled by the timing generator shown in Fig.5. The counter counts from 1 to 1,080 repeatedly, triggered by $V_{\rm sync,hor}$. When the counter counts from 1 to 825, $\rm SW_0$ is closed, no active charging is exerted. When counting from 826 to 926, $\rm SW_1$ is closed, rendering $\tau_1 = 3.1821\mu$s for segment 1, and so on.

Table III lists the segmentation of subpixels along a data line at different charging ratios. At higher charging ratio, more segments are required, and the number of subpixels in each segment is reduced. The number of subpixels in a segment farther away from the driver is smaller than that in a segment closer to the driver.

Fig.8 shows the deviation of charging ratio along a data line at $\alpha = 0.995$ and $\alpha = 0.999$, which are less than 0.5% and 0.15%, respectively. LCDs are voltage-sensitive display. For voltage error greater than 5 mV, the transmittance difference could be visible. To overcome this problem, a higher value of charging ratio α is suggested. The segmentation plans associated with Figs.8(a) and 8(b) are designed based on the voltage error within 25 mV and 5 mV, respectively.

For LCD in MVA or IPS mode, the voltage swing sometimes can reach 10 V. Considering the inversion feature of LCD, the magnitude of one gray level is about 23 mV. To reduce the error to within one gray level, the charging ratio must be greater than 0.999, and 23 switches are needed for each operational amplifier.

Fig.9 shows the resistance associated with the resistor networks at different charging ratios. The range of resistance is wider at larger charging ratio.

TABLE III
SEGMENTATION OF SUBPIXELS ALONG A DATA LINE.

Segment	$\alpha = 0.99$	$\alpha = 0.995$	$\alpha = 0.999$
0	$1 \sim 882$	$1 \sim 825$	$1 \sim 726$
1	$883 \sim 1,009$	$826 \sim 926$	$727 \sim 792$
2	$1,010 \sim 1,080$	$927 \sim 987$	$793 \sim 829$
3	–	$988 \sim 1,034$	$830 \sim 856$
4	–	$1,035 \sim 1,074$	$857 \sim 879$
5	–	$1,075 \sim 1,080$	$880 \sim 898$
6	–	–	$899 \sim 915$
7	–	–	$916 \sim 930$
8	–	–	$931 \sim 944$
9	–	–	$945 \sim 957$
10	–	–	$958 \sim 970$
11	–	–	$971 \sim 981$
12	–	–	$982 \sim 992$
13	–	–	$993 \sim 1,002$
14	–	–	$1,003 \sim 1,012$
15	–	–	$1,013 \sim 1,022$
16	–	–	$1,023 \sim 1,031$
17	–	–	$1,032 \sim 1,040$
18	–	–	$1,041 \sim 1,048$
19	–	–	$1,049 \sim 1,056$
20	–	–	$1,057 \sim 1,065$
21	–	–	$1,066 \sim 1,072$
22	–	–	$1,073 \sim 1,080$

Fig.10 shows the relation between the panel size and the number of segments required to reach $\alpha = 0.995$. The number of segments increases linearly with the panel size. For example, the numbers of segments for 60", 80", and 160" panels are 6, 20, and 105, respectively. For the large one like 160" panel, two data drivers may be considered to drive the data line from opposite ends, and the total number of segments can be reduced to about 40.

IV. CONCLUSIONS

An active charging method for large-size or high-resolution LCD is proposed. In this method, the data between adjacent frames are compared, different effective time constants at different locations on a data line are considered to generate the precise active charging voltage at the given charging ratio. Compared to conventional method, this method can charge large-size panel more precisely within the charging time.

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Design Constraints on FSC LCD

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***Abstract*— Design constraints on field-sequential color (FSC) LCDs are proposed and compared with those of conventional color filter (CF) LCDs. Application of these constraints to the design of LCD screens is demonstrated.**

***Index Terms*— Liquid crystal display, thin-film transistor, power demand, TV display, HDTV.**

I. Introduction

Compared with color-filter (CF) LCDs of the same screen size, the field-sequential color (FSC) LCDs consume less power and can support a finer resolution. Under the same resolution, the pixel size of the FSC LCDs is three times that of the CF LCDs while its charging time is one third of the latter [1]. The FSC LCDs display a color image using the technique of temporal color mixture instead of the spatial color mixture, hence the response of liquid crystal molecules and circuits must be three times faster than those of the CF LCDs.

In 1989, Kaneko developed a pixel model based on an equivalent circuit [2], however, no design constraints were mentioned. In 1996, a dynamic analysis of an a-Si TFT-LCD pixel was presented by embedding an a-Si TFT model and a liquid cyrstal capacitance model in the SPICE simulator [3], but no design constraints were discussed. Tsukada proposed a theory to analyze LCD subpixels [4], [5], but no systematic design procedure was proposed. In 1998, Tsukada proposed a scaling theory to analyze the gate delay and offset voltage in TFT-LCDs with narrow bus-line width and small pixel capacitance [6].

In 2001, Zhu presented the simulation results of kickback voltage on a-Si TFT-LCDs, with the orientation of liquid crystal molecules controlled by an imposed voltage [7]. Higuchi developed poly-Si TFT-LCDs using a dual-drive technique [8]. In 2006, Tai proposed the concept of operation window based on the mechanisms of charging, holding, coupling and delay [9], which can be used to determine the pixel storage capacitance and the TFT channel width.

In this paper, an equivalent circuit of a supbixel is used to derive a set of design constraints for FSC LCDs. An operation window is thus built to analyze the difference between FSC LCDs and CF LCDs at various screen sizes. The models of pixel and signal line will be described in Section 2, the constraints on pixel design will be presented in Section 3, the pixel design for FSC LCDs will be proposed in Section 4, the assessment of different screen sizes based on these constraints will be discussed in Section 5, followed by the conclusions.

II. Models of Pixel and Signal Line

Fig. 1 shows the equivalent circuit of a pixel, where $C_{\rm LC}$ and $R_{\rm LC}$ are the capacitance and resistance, respectively, between the ITO and the common electrode of a pixel. The

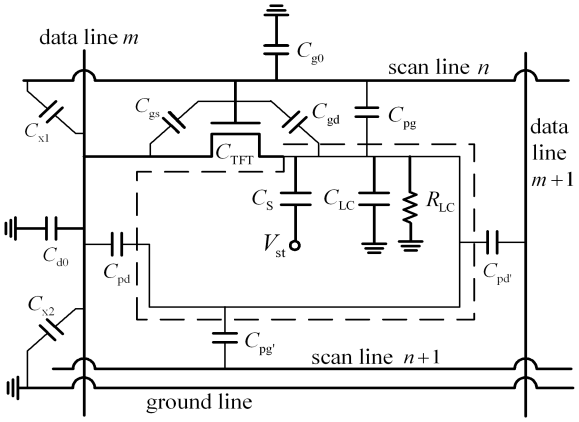

Fig. 1. Equivalent circuit of a pixel.

pixel capacitance can be decomposed as [4]

$$\begin{aligned} C_{\rm px} &= C_S + C_{\rm LC} + C_{\rm gd} + C_{\rm pd'} + C_{\rm pd} + C_{\rm pg'} + C_{\rm pg} \\ &\simeq C_S + C_{\rm LC} \end{aligned}$$

where we assume the parasitic capacitances $C_{\rm gd}$, $C_{\rm pd'}$, $C_{\rm pd}$, $C_{\rm pg'}$, $C_{\rm pg}$ are much smaller than $C_{\rm LC}$ and the storage capacitance C_S.

To estimate the loading effect of a pixel on a scan line [9], [10], first calculate the equivalent resistance $R_{\rm scan}$ as

$$R_{\rm scan} = \rho_{\rm scan} \frac{L_{\rm scan}}{A_{\rm scan}}$$

where $A_{\rm scan} = t_{\rm scan} \times W_{\rm scan}$ is the cross-sectional area of the scan line, $\rho_{\rm scan}$, $W_{\rm sacn}$ and $t_{\rm scan}$ are the resistivity, width, and thickness, respectively, of the scan line, $L_{\rm scan}$ is the length of the scan line across a pixel. The load capacitance $C_{\rm scan}$ can be approximated as

$$C_{\rm scan} \simeq C_{\rm gs} + C_{\rm TFT} + C_{\rm g0} + C_{\rm x1} + C_{\rm gd} + C_{\rm pg} + C_{\rm pg'} \quad (1)$$

Next, consider the loading effect of a pixel on a data line. The equivalent resistance $R_{\rm data}$ can be calculated as

$$R_{\rm data} = \rho_{\rm data} \frac{L_{\rm data}}{A_{\rm data}}$$

where $A_{\rm data} = t_{\rm data} \times W_{\rm data}$ is the cross-sectional area of the data line, $\rho_{\rm data}$, $W_{\rm data}$, and $t_{\rm data}$ are the resistivity, width, and thickness, respectively, of the data line, and $L_{\rm data}$ is the length of the data line across a pixel. The load capacitance $C_{\rm data}$ can be approximated as

$$C_{\rm data} \simeq C_{\rm x1} + C_{\rm x2} + C_{\rm d0} + C_{\rm gs} + C_{\rm pd'} + C_{\rm pd}$$

A scan line or a data line can be modeled as a lossy transmission line with the per-unit-length resistance and capacitance of R and C, respectively. Assume the signal line

has a finite length ℓ and is open circuited at $z = \ell$, and the driving voltage at $z = 0$ is a step function of time, then the waveform at $z = \ell$ will be [4]

$$\frac{v(\ell,t)}{V_g} = 1 + \frac{4}{\pi}\sum_{n=1}^{\infty}\frac{(-1)^n}{2n-1}\exp\left[-\frac{(2n-1)^2\pi^2}{4RC\ell^2}t\right] \quad (2)$$

When $t > RC\ell^2$, (2) can be approximated as

$$\frac{v(\ell,t)}{V_g} \simeq 1 - \frac{4}{\pi}\exp\left(-\frac{\pi^2 t}{4RC\ell^2}\right)$$

Thus, it takes the delay time of $1.03RC\ell^2$, $1.96RC\ell^2$ and $2.25RC\ell^2$ for the voltage at the load to reach $v(\ell,t)/V_g = 90\%$, 99%, and 99.5%, respectively.

III. Constraints on Pixel Design

As shown in Fig. 1, the voltage V_e at the display electrode is a function of the data line voltage V_d as [5], [6]

$$V_e = \frac{1 - ae^{-t/\tau}}{1 - be^{-t/\tau}}V_d$$

with

$$a = \frac{V_d - V_{e0}}{V_d}\frac{2(V_s - V_t - V_d) + V_d}{2(V_s - V_t - V_d) + V_d - V_{e0}}$$
$$b = \frac{V_d - V_{e0}}{2(V_s - V_t - V_d) + V_d - V_{e0}}$$
$$\tau = \frac{C_{\rm px}}{\beta_0(V_s - V_t - V_d)}$$

where V_s is the voltage on the scan line, V_t is the threshold voltage of the TFT, $V_{e0} = V_e(t = 0)$, and $\beta_0 = \mu_{\rm eff}C_gW/L$ is a parameter determined by the TFT geometry and material [4]. The channel width W and length L of the TFT are the design parameters to be optimized.

A. Charging Phase

First express the rise-time t_r in units of τ as $t_r = k_t\tau$, and define the voltage ratio $r_c = V_e/V_d$, then k_t can be expressed as

$$k_t = \ln\frac{a - br_c}{1 - r_c}$$

The rise-time must be shorter than the period $T_{\rm row}$ allocated for displaying one row of pixels, deducting the delay over the scan line, namely,

$$t_r < T_{\rm row} - T_{\rm delay}$$

where $T_{\rm delay}$ is the maximum allowable delay time over a scan line. Thus, we obtain the first constraint

$$\frac{W}{L} > \frac{C_{\rm px}}{\mu_{\rm eff}C_g(V_s - V_t - V_d)}\frac{k_t}{(T_{\rm row} - T_{\rm delay})} \quad (3)$$

Note that the delay time along a sacn line depends on the TFT parameters. Hence the maximum allowable delay time must be estimated iteratively, incorporating the other constraints that will be discussed later.

B. Holding Phase

In the holding phase, the charge leaks through the equivalent RC circuit formed by $R_{\rm LC}$, $R_{\rm off}$ and $C_{\rm px}$, where $R_{\rm off} = V_{ed}/I_{\rm off}$ is the off-resistance of the TFT with $V_{ed} = V_e - V_d$ [10]. The time constant of the pixel during the holding phase is

$$\tau_{\rm px} = \frac{R_{\rm LC}R_{\rm off}}{R_{\rm LC} + R_{\rm off}}C_{\rm px} \quad (4)$$

The leakage current $I_{\rm off}$ can be expressed as [10]

$$I_{\rm off} \simeq \frac{\sigma_{\rm D}t_{\rm semi}V_{ed}W}{L}$$

where $\sigma_{\rm D}$ and $t_{\rm semi}$ are the dark conductivity and thickness, respectively, of the semicoductor layer.

Define the retention ratio in the holding phase as

$$r = e^{-T_{\rm frame}/\tau_{\rm px}}$$

To display a distortion-free image, the voltage deviation due to leakage must be less than one grey level, which leads to

$$r > 1 - \frac{1}{2^{N_{\rm bit}}} \quad (5)$$

where $N_{\rm bit}$ is the number of bits. Substituting (4) into (5), we obtain the second constraint

$$\frac{W}{L} < \frac{C_{\rm px}}{T_{\rm frame}2^{N_{\rm bit}}\sigma_{\rm D}t_{\rm semi}} \quad (6)$$

C. Asymmetric Kickback

At the end of the charging phase, the TFT is turned off and the pixel is switched to the holding phase, the voltage at the gate terminal of $C_{\rm gd}$ is pulled low, and the display electrode at the other terminal of $C_{\rm gd}$ is pulled low, too. By imposing the law of charge conservation and assuming the scan pulse is a square pulse, a kickback voltage of magnitude [4]

$$\Delta V_{\rm kb} = (v_{s,\rm on} - v_{s,\rm off})\frac{C_{\rm gd} + C_{\rm pg}}{C_{\rm gd} + C_{\rm pg} + C_{\rm LC}(V) + C_S}$$

will appear at the display electrode of the pixel, where $v_{s,\rm on}$ and $v_{s,\rm off}$ are the voltages on the scan line at the on and off states, respectively, $C_{\rm gd}$ is the parasitic capacitatance between the gate and the drain electrodes of TFT, and $C_{\rm LC}(V)$ is the voltage across the pixel.

Define the deviation of $\Delta V_{\rm kb}$ as

$$\begin{aligned}\Delta(\Delta V_{\rm kb}) &= \frac{\Delta V_{\rm kb,max} - \Delta V_{\rm kb,min}}{2} \\ &= \frac{(v_{s,\rm on} - v_{s,\rm off})(C_{\rm gd} + C_{\rm pg})}{2(C_{\rm gd} + C_{\rm pg} + C_{\rm LC,min} + C_S)} \\ &\quad \frac{C_{\rm LC,max} - C_{\rm LC,min}}{C_{\rm gd} + C_{\rm pg} + C_{\rm LC,max} + C_S}\end{aligned} \quad (7)$$

The average of $\Delta V_{\rm kb}$ can be compensated by tuning the voltage level of the common electrode on the color-filter substrate, but the voltage deviation $\Delta(\Delta V_{\rm kb})$ tends to induce a residual direct current with a preferred polarity, which will degrade the quality of the liquid crystal. Hence, $\Delta(\Delta V_{\rm kb})$ must be constrained by an acceptable residual voltage threshold $F_{\rm kb}$ as [9]

$$\Delta(\Delta V_{\rm kb}) < F_{\rm kb} \quad (8)$$

The capacitance $C_{\rm gd}$ can be expressed in terms of $\tilde{C}_{\rm gd}$, the gate-to-drain capacitance per unit channel width, as

$$C_{\rm gd} = \tilde{C}_{\rm gd} W \tag{9}$$

Substituting (7) and (9) into (8), and assuming $C_{\rm gd} \ll C_{\rm LC} + C_S$, a third design constraint is derived as

$$W < \frac{\dfrac{2\left(C_{\rm LC,min}+C_S\right)\left(C_{\rm LC,max}+C_S\right)F_{\rm kb}}{\left(v_{s,\rm on}-v_{s,\rm off}\right)\left(C_{\rm LC,max}-C_{\rm LC,min}\right)} - C_{\rm pg}}{\tilde{C}_{\rm gd}} \tag{10}$$

D. Delay

To estimate the delay along a scan line using the lossy transmission line model, first approximate the per-unit-length resistance and capacitance along the scan line as $R = R_{\rm scan}/L_{\rm scan}$ and $C = C_{\rm scan}/L_{\rm scan}$, respectively. If there are $N_{\rm data}$ pixels along one scan line, the total length of the scan line will be $N_{\rm data}L_{\rm scan}$. The delay $t_{\rm d,scan}$ for the voltage to reach 90% of its intended level can thus be calculated as

$$t_{\rm d,scan} = 1.03 N_{\rm data}^2 R_{\rm scan} C_{\rm scan} \tag{11}$$

This delay must be shorter than the specified $T_{\rm delay}$, namely,

$$t_{\rm d,scan} < T_{\rm delay} \tag{12}$$

Substituting (1) and (11) into (12), we obtain the fourth constraint on the channel width W as

$$W < \frac{\dfrac{T_{\rm delay}}{1.03 N_{\rm data}^2 R_{\rm scan}} - \left(C_{\rm g0}+C_{\rm x1}+C_{\rm pg}+C_{\rm pg'}\right)}{2\tilde{C}_{\rm gd} + \epsilon_{\rm insu}\epsilon_0 L/t_{\rm insu}}$$

where $C_{\rm gs} \simeq C_{\rm gd} = \tilde{C}_{\rm gd} W$, $C_{\rm TFT} = \epsilon_{\rm insu}\epsilon_0 WL/t_{\rm insu}$, $\epsilon_{\rm insu}$ and $t_{\rm insu}$ are the relative dielectric constant and thickness, respectively, of the insulator layer.

Similarly, one may substitute $R = R_{\rm data}/L_{\rm data}$ and $C = C_{\rm data}/L_{\rm data}$ into the lossy transmission line model to estimate the delay along a data line. Since a data line runs across $N_{\rm scan}$ rows of pixels, the total length of a data line is $N_{\rm scan}L_{\rm data}$, thus we derive another constraint

$$W < \frac{\dfrac{T_{\rm delay}}{1.03 N_{\rm scan}^2 R_{\rm data}} - \left(C_{\rm x1}+C_{\rm x2}+C_{\rm d0}+C_{\rm pd}+C_{\rm pd'}\right)}{\tilde{C}_{\rm gd}}$$

IV. Pixel Design for FSC LCDs

Under the same resolution and screen size, the frame period $T_{\rm frame}$ and the pixel size $A_{\rm pixel}$ of the FSC LCDs and the CF LCDs are related as

$$T_{\rm frame,FSC} = \frac{1}{3} T_{\rm frame,CF}$$
$$A_{\rm pixel,FSC} = 3 A_{\rm subpixel,CF}$$

As a consequence, $T_{\rm row,FSC} = \dfrac{1}{3} T_{\rm row,CF}$, $C_{\rm LC,FSC} = 3C_{\rm LC,CF}$, and $R_{\rm LC,FSC} = \dfrac{1}{3} R_{\rm LC,CF}$. Define the ratio between the size of storage capacitor and that of the pixel as $h = A_{C_S}/A_{\rm pixel}$, then $C_{\rm px,FSC}$ can be rephrased as

$$C_{\rm px,FSC} \simeq C_{\rm LC,FSC}\left(1 + \frac{\epsilon_{\rm insu} d_{\rm LC}}{t_{\rm insu}\epsilon_{\rm LC}} h_{\rm FSC}\right)$$

where $\epsilon_{\rm LC}$ and $d_{\rm LC}$ are the relative dielectric constant and thickness, respectively, of the liquid crystal layer.

Similar to the derivation leading to (3), the lower bound $(W/L)_{\rm charge,FSC}$ for FSC LCDs can be derived as

$$\frac{C_{\rm px,FSC}}{\mu_{\rm eff} C_g \left(V_s - V_t - V_d\right)} \frac{k_t}{\left(T_{\rm row,FSC} - T_{\rm delay}\right)}$$

As a comparison, the lower bound $(W/L)_{\rm charge,CF}$ for CF LCDs is

$$\frac{C_{\rm px,CF}}{\mu_{\rm eff} C_g \left(V_s - V_t - V_d\right)} \frac{k_t}{\left(T_{\rm row,CF} - T_{\rm delay}\right)}$$

Since $T_{\rm row,FSC} = \dfrac{1}{3} T_{\rm row,CF}$ and $C_{\rm LC,FSC} = 3C_{\rm LC,CF}$, the two lower bounds are related as

$$\left(\frac{W}{L}\right)_{\rm charge,FSC} \simeq 9 \left(\frac{1 + \dfrac{\epsilon_{\rm insu} d_{\rm LC}}{t_{\rm insu}\epsilon_{\rm LC}} h_{\rm FSC}}{1 + \dfrac{\epsilon_{\rm insu} d_{\rm LC}}{t_{\rm insu}\epsilon_{\rm LC}} h_{\rm CF}}\right) \left(\frac{W}{L}\right)_{\rm charge,CF}$$

Following the derivation leading to (6), the upper bounds of W/L derived from the holding phase constraint are

$$\left(\frac{W}{L}\right)_{\rm hold,FSC} = \frac{C_{\rm px,FSC}}{T_{\rm frame,FSC} 2^{N_{\rm bit}} \sigma_{\rm D} t_{\rm semi}}$$
$$\left(\frac{W}{L}\right)_{\rm hold,CF} = \frac{C_{\rm px,CF}}{T_{\rm frame,CF} 2^{N_{\rm bit}} \sigma_{\rm D} t_{\rm semi}}$$

respectively. They are related by

$$\left(\frac{W}{L}\right)_{\rm hold,FSC} \simeq 9 \left(\frac{1 + \dfrac{\epsilon_{\rm insu} d_{\rm LC}}{t_{\rm insu}\epsilon_{\rm LC}} h_{\rm FSC}}{1 + \dfrac{\epsilon_{\rm insu} d_{\rm LC}}{t_{\rm insu}\epsilon_{\rm LC}} h_{\rm CF}}\right) \left(\frac{W}{L}\right)_{\rm hold,CF}$$

Similar to the derivation of (10), another upper bound of W based on the asymmetric kickback voltage constraint, $W_{\rm kb,FSC}$, is derived as

$$\frac{\dfrac{2\left(C_{\rm LC,min,FSC}+C_{S,\rm FSC}\right)\left(C_{\rm LC,max,FSC}+C_{S,\rm FSC}\right)F_{\rm kb}}{\left(v_{s,\rm on}-v_{s,\rm off}\right)\left(C_{\rm LC,max,FSC}-C_{\rm LC,min,FSC}\right)} - C_{\rm pg}}{\tilde{C}_{\rm gd}}$$

for the FSC LCDs, and the counterpart $W_{\rm kb,CF}$ for the CF LCDs is

$$\frac{\dfrac{2\left(C_{\rm LC,min,CF}+C_{S,\rm CF}\right)\left(C_{\rm LC,max,CF}+C_{S,\rm CF}\right)F_{\rm kb}}{\left(v_{s,\rm on}-v_{s,\rm off}\right)\left(C_{\rm LC,max,CF}-C_{\rm LC,min,CF}\right)} - C_{\rm pg}}{\tilde{C}_{\rm gd}}$$

The kickback voltage is a function of the falling slope of the scan pulse, a steeper slope induces a larger kickback voltage. In this analysis, an infinite slope is assumed to derive the largest possible kickback voltage.

Similar to (11), the scan-line delay $t_{\rm d,scan,FSC}$ for the voltage to reach 90% of its intended level can be expressed as

$$t_{\rm d,scan,FSC} = 1.03 N_{\rm data,FSC}^2 R_{\rm scan,FSC} C_{\rm scan,FSC}$$

Under the same resolution, screen size and process condition, and assuming the R, G and B subpixels on the CF screen are aligned horizontally, the sacn line length passing through an FSC pixel will be three times that passing through

TABLE I
GENERAL PERFORMACES OF 30" AND 2.4" LCD PIXEL, *: AR=0.

parameter	30" HDTV	2.4" portable
resolution	WXGA (1,366×768)	QVGA (320×240)
aspect ratio	16:9	4:3
$T_{\rm delay}$	1.7 μs	17 ns
$A_{\rm px,FSC}(\mu{\rm m}^2)$	236,500	23,226
$A_{\rm subpx,CF}(\mu{\rm m}^2)$	78,833	7,742
$h_{\rm FSC}$	(0.120, 0.496)	(0.116, 0.941*)
$h_{\rm CF}$	(0.430, 0.876*)	(0.416, 0.903*)
$W_{\rm FSC}(\mu{\rm m})$	(157, 284)	(3.59, 223.8)
$W_{\rm CF}(\mu{\rm m})$	(34, 70)	((0.93, 73.33)
${\rm AR}_{\rm FSC}(\%)$	(42, 79)	(0, 82)
${\rm AR}_{\rm CF}(\%)$	(0, 45)	(0, 48)
$\frac{{\rm AR}_{\rm FSC,max}}{{\rm AR}_{\rm CF,max}}$	1.76	1.7

a CF subpixel, hence $N_{\rm data,FSC} = \frac{1}{3}N_{\rm data,CF}$, $R_{\rm scan,FSC} \simeq 3R_{\rm scan,CF}$, $C_{\rm scan,FSC} \simeq 3C_{\rm scan,CF}$, and $t_{\rm d,scan,FSC} \simeq t_{\rm d,scan,CF}$.

The data-line delay $t_{\rm d,data,FSC}$ for the voltage to reach 90% of its intended level can be expressed as

$$t_{\rm d,data,FSC} = 1.03N^2_{\rm scan,FSC}R_{\rm data,FSC}C_{\rm data,FSC}$$

Since $N_{\rm scan,FSC} = N_{\rm scan,CF}$, we have $R_{\rm data,FSC} \simeq R_{\rm data,CF}$, $C_{\rm data,FSC} \simeq C_{\rm data,CF}$, and $t_{\rm d,data,FSC} \simeq t_{\rm d,data,CF}$.

Since a scan line drives more pixels than a data line does, $t_{\rm d,scan} > t_{\rm d,data}$, thus the delay time $T_{\rm delay}$ during the charging phase is dominated by the scan line delay, hence

$$T_{\rm delay,FSC} \simeq T_{\rm delay,CF}$$

namely, both FSC LCDs and CF LCDs have similar delay time budget.

In summary, the major constraint on the FSC pixel design is the short charging time. On the other hand, the FSC pixel design is less restricted in the holding, asymmetric kickback, and delay mechanisms. Since $C_{\rm LC,FSC} = 3C_{\rm LC,CF}$ and $C_{\rm px} \simeq C_{\rm LC} + C_S$, the storage capacitance required in the FSC LCDs can be decreased. Since the storage capacitor and the TFT are opaque, smaller h and W are preferred. A higher aperture ratio can be realized in the FSC LCDs, which requires lower backlight intensity and hence lower power consumption.

V. ASSESSMENT OF DIFFERENT SCREEN SIZES

In this section, the performances of a 30" WXGA and a 2.4" QVGA LSD will be analyzed. The FSC LCDs and the CF LCDs will be compared in terms of operation window, aperture ratio, and power consumption.

A. Operation Window

Fig. 2 shows the operation windows of 30" WXGA LCDs based on the design constraints, where W is the TFT channel width and $h = A_{C_S}/A_{\rm pixel}$ is the ratio between the size of the storage capacitor and that of the pixel. The operation window of the FSC LCD has relatively low h and high W compared with that of the CF LCD, with $h_{30",\rm FSC} > 0.121$ and $h_{30",\rm CF} > 0.423$.

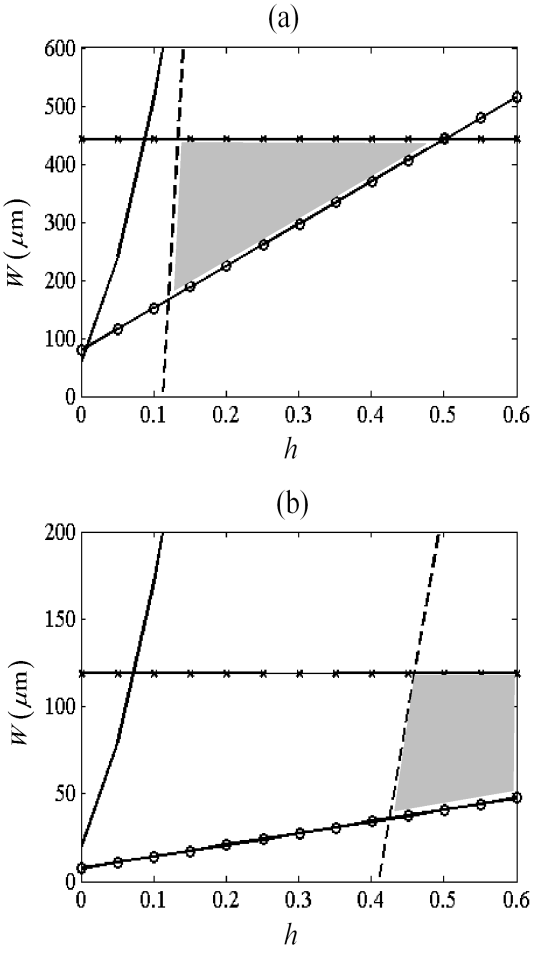

Fig. 2. Operation window of 30" WXGA LCD, (a) FSC LCD, (b) CF LCD, $-\circ-$: charging constraint, $---$: holding constraint, —: asymmetric kickback constraint, $-*-$: scan-line delay constraint, cell gap is $d_{\rm LC} = 4.7$ μm, line widths are $W_{\rm scan} = 20$ μm and $W_{\rm data} = 10$ μm, sheet resistance is 16.8 nΩm, dielectric constant and thickness of insulator are $\epsilon_{\rm insu} = 6.9$ and $t_{\rm insu} = 300$ nm, parameters of TFT are $\mu_{\rm eff} = 0.15 \times 10^{-4}$ m^2/Vs and $V_t = 0.7$ V.

If the minimum channel widths, $W_{30",\rm FSC} = 157$ μm at $h_{30",\rm FSC} = 0.121$ and $W_{30",\rm CF} = 34$ μm at $h_{30",\rm CF} = 0.423$, respectively, are chosen, the maximum aperture ratios will be ${\rm AR}_{30",\rm FSC} = 79\%$ and ${\rm AR}_{30",\rm CF} = 45\%$. The available AR at different channel widths and area ratios are marked in Fig. 3. The maximm AR of the FSC LCDs is about twice that of the CF LCDs.

The performance parameters of two different LCD screen sizes are summarized in Table I. The lower bound of W is determined by the charging phase constraint for both screen sizes, but the dominant factors for the upper bound of W are different. For the large-size LCDs, the upper bound of W is determined by the holding phase and the scan-line delay constraints. For the small-size LCDs, the asymmetric kickback constraint affects the operation window and can not be neglected as shown in Fig. 4.

For 2.4" QVGA LCDs, the minimum TFT channel widths

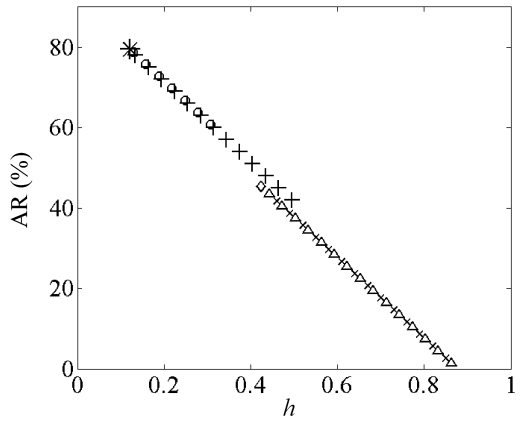

Fig. 3. AR of 30" WXGA LCD, *: $W_{30",\mathrm{FSC}} = 157\ \mu$m, ○: $W_{30",\mathrm{FSC}} = 284\ \mu$m, +: $W_{30",\mathrm{FSC}} = 411\ \mu$m, ◇: $W_{30",\mathrm{CF}} = 34\ \mu$m, △: $W_{30",\mathrm{CF}} = 70\ \mu$m, ×: $W_{30",\mathrm{CF}} = 108\ \mu$m.

of the FSC LCD and the CF LCD are $3.59\ \mu$m and $0.93\ \mu$m, respectively. At a given h, larger L implies larger W based on the holding and charging constraints, and the intercept point of the charging and holding bounds will be moved toward smaller h and larger W. In this case, the asymmetric kickback constraint instead of the holding constraint will dominate the upper bound of the operation window in the FSC LCDs.

Note that the scan driver can be used to drive the scan line at both ends simultaneously, and the longest delay will occur at the center of the scan line. When using this double-driver technique, T_{delay} can be reduced to about one quarter that of using conventional single driver.

The pixel area A_{pixel} is proportional to C_{px}. In the charging phase, larger current is required to charge a larger C_{px}, and the charging current of TFT is determined by the channel width W. Thus, there is a positive correlation between the channel width W and the pixel area A_{pixel}.

The capacitive load on a scan line can be reexpressed as

$$C_{\mathrm{scan}} = \left(2\tilde{C}_{\mathrm{gd}} + \epsilon_{\mathrm{insu}}\epsilon_0\frac{L}{t_{\mathrm{insu}}}\right)W + 2\epsilon_{\mathrm{insu}}\epsilon_0\frac{t_{\mathrm{insu}}L_{\mathrm{scan}}}{s_{\mathrm{pg}}} + \epsilon_0\left(\epsilon_{\mathrm{LC}}\frac{L_{\mathrm{scan}}}{d_{\mathrm{LC}}} + \epsilon_{\mathrm{insu}}\frac{W_{\mathrm{data}}}{t_{\mathrm{insu}}}\right)W_{\mathrm{scan}}$$

Thus, the delay T_{delay} can be rephrased as

$$1.03N_{\mathrm{data}}^2\rho_{\mathrm{scan}}\frac{L_{\mathrm{scan}}}{t_{\mathrm{scan}}}\left(\frac{B}{W_{\mathrm{scan}}} + D\right)$$

where

$$B = \left(2\tilde{C}_{\mathrm{gd}} + \epsilon_0\epsilon_{\mathrm{insu}}\frac{L}{t_{\mathrm{insu}}}\right)W + \epsilon_0\epsilon_{\mathrm{insu}}\frac{t_{\mathrm{insu}}L_{\mathrm{scan}}}{s_{\mathrm{pg}}}$$

$$D = \epsilon_0\left(\epsilon_{\mathrm{LC}}\frac{L_{\mathrm{scan}}}{d_{\mathrm{LC}}} + \epsilon_{\mathrm{insu}}\frac{W_{\mathrm{data}}}{t_{\mathrm{insu}}}\right)$$

For 30" LCDs, signal delays can not be neglected, and wider scan-lines are needed to reduce the delay along the scan lines. For example, if choosing $W_{\mathrm{scan},30"} = 20\ \mu$m and $W_{\mathrm{scan},2.4"} = 3\ \mu$m, the delay times will be 1.7 μs and 17 ns, respectively.

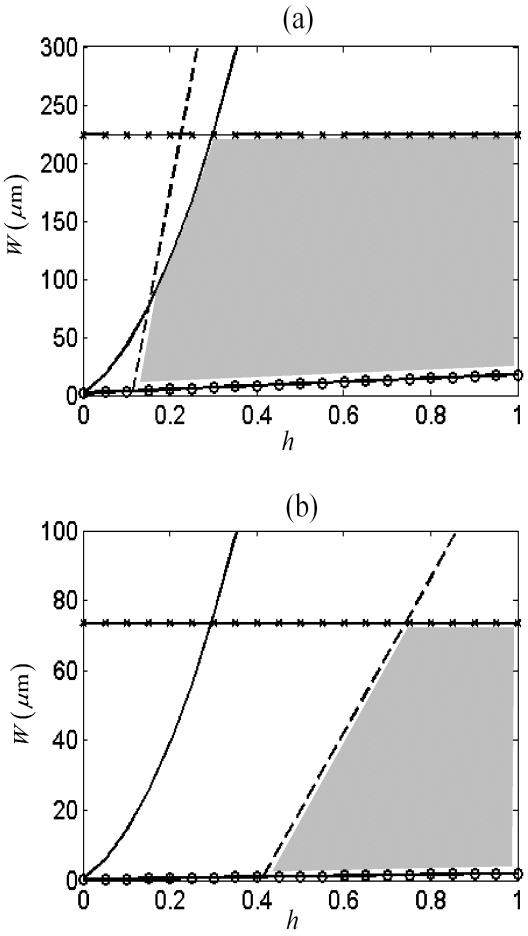

Fig. 4. Operation window of 2.4" QVGA LCD, (a) FSC LCD, (b) CF LCD, $-\circ-$: charging constraint, $---$: holding constraint, —: asymmetric kickback constraint, $-*-$: scan-line delay constraint, parameters the same as in Fig.3, excep $W_{\mathrm{scan}} = W_{\mathrm{data}} = W_{\mathrm{ground}} = 3\ \mu$ m.

B. Aperture Ratio

The aperture ratio is defined as

$$\mathrm{AR} = \frac{A_{\mathrm{pixel}} - A_{\mathrm{opaque}}}{A_{\mathrm{pixel}}}$$

where A_{opaque} is the opaque area in a pixel. As shwon in Fig. 1, A_{opaque} is decomposed as

$$A_{\mathrm{opaque}} = A_{\mathrm{data}} + A_{\mathrm{scan}} + A_{\mathrm{ground}} + A_{\mathrm{TFT}} + A_{C_S} - A_{\mathrm{cross}}$$

where $A_{\mathrm{data}} = L_{\mathrm{data}} \times W_{\mathrm{data}}$, $A_{\mathrm{scan}} = L_{\mathrm{scan}} \times W_{\mathrm{scan}}$, $A_{\mathrm{ground}} = L_{\mathrm{scan}} \times W_{\mathrm{ground}}$ are the areas of data line, scan line, and ground line, respectively, in the (m,n)th pixel, $A_{\mathrm{TFT}} = W \times L$ is the area of the TFT, $A_{C_S} = hA_{\mathrm{pixel}}$ is the area of the storage capacitor, and $A_{\mathrm{cross}} = W_{\mathrm{data}} \times (W_{\mathrm{scan}} + W_{\mathrm{ground}})$ is the overlapping area between a scan line and a data line. The relation between C_S/C_{px} and h is

$$\frac{C_S}{C_{\mathrm{px}}} \simeq \frac{C_S}{C_S + C_{\mathrm{LC}}} = \frac{hd_{\mathrm{LC}}}{hd_{\mathrm{LC}} + t_{\mathrm{insu}}\epsilon_{\mathrm{LC}}/\epsilon_{\mathrm{insu}}}$$

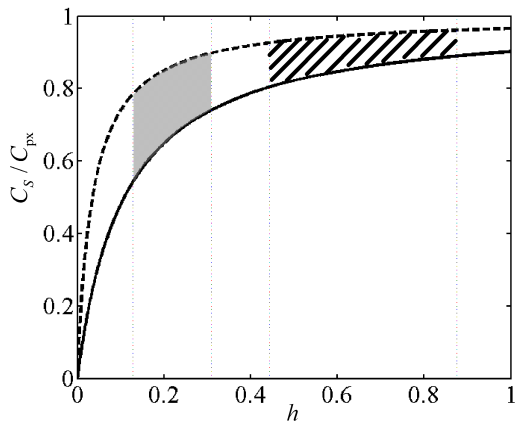

Fig. 5. Relation between capacitance ratio and area ratio, grey area for FSC with $W = 284$ μm, slit area for CF with $W = 70$ μm, $--$: $\epsilon_{\rm LC} = 3.8$, —: $\epsilon_{\rm LC} = 11.7$, parameters the same as in Fig.3.

Fig. 5 shows the capacitance ratio $C_S/C_{\rm px}$ as a function of h, with $d_{\rm LC} = 4.67$ μm, $t_{\rm insu} = 0.3$ μm, $\epsilon_{\rm insu} = 6.9$, and $3.8 \leq \epsilon_{\rm LC} \leq 11.7$. Take $W_{\rm FSC} = 284$ μm, $0.128 < h_{\rm FSC} < 0.309$ and $W_{\rm CF} = 70$ μm, $0.443 < h_{\rm CF} < 0.876$, respectively, as deduced from the operation windows shown in Fig. 2. Note that $0.55 \leq$ $C_S/C_{\rm px}$ ≤ 0.9 for the FSC LCDs, and $0.80 \leq$ $C_S/C_{\rm px}$ ≤ 0.96 for the CF LCDs. Smaller $C_S/C_{\rm px}$ ratio implies that smaller storage capacitance is needed to satisfy the holding constraint. Because the storage capacitor is opaque, larger $C_S/C_{\rm px}$ ratio implies smaller aperture ratio. Note that ${\rm AR}_{\rm FSC} > {\rm AR}_{\rm CF}$ and the ratio ${\rm AR}_{\rm FSC,max}/{\rm AR}_{\rm CF,max}$ is about 1.7.

The backlight consumes the most power in the LCDs. Higher aperture ratio implies higher backlight efficiency or less power consumption. In the FSC LCDs, the backlight efficiency is three times that of the CF LCDs since no color filters are used. If ${\rm AR}_{\rm FSC,max}/{\rm AR}_{\rm CF,max}$ is about two, then the total backlight power consumption of the FSC LCDs will be only one sixth that the the CF LCDs. For example, if the 30" CF LCDs require 130 W of backlight, then the 30" FSC LCDs will require only 24 W to provide the same luminance. Similarly, for 2.4" LCDs, if the CF LCDs require 500 mW of backlight, the FSC ones will require only 90 mW.

C. Power Consumption

The power consumption of the data driver can be estimated as [11]

$$P = V_{\rm DD} \frac{N_{\rm scan} C_{\rm data} \Delta V_{d,\max}}{2T_{\rm row}} N_{\rm data}$$

where $V_{\rm DD}$ is the power supply voltage, $\Delta V_{d,\max}$ is the maximum voltage swing on the data lines. Thus, the power consumption ratio between the FSC LCDs and the CF LCDs is close to one.

VI. Conclusions

Design constraints on the FSC LCDs have been derived and demonstrated with two different screen sizes. The FSC pixel design is less constrained in the holding, asymmetric kickback and delay mechanisms, but is more strictly constrained in the charging phase. Higher aperture ratio and less power consumption can be achieved for the FSC LCDs due to the smaller storage capacitance needed. The line width and channel width are critical in large-size LCDs, especially in the FSC LCDs. Although the frame rate of the FSC LCDs is three times that of the CF LCDs, the power consumption in pixel related circuitries of the FSC LCDs is close to that of the CF LCDs.

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Session: 118 **10:00-11:40** **Honolulu**

Dielectric Resonator Antennas for Mobile Communications

10:00 118.1 Modeling and Experimental Study of Dielectric Loaded Monopoles for UWB Applications.....541
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Dept. Electrical Eng. and Grad. Inst. Commun. Eng., National Taiwan University, Taipei, Taiwan

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V. Hamsakutty, M. T. Kattackal, Y. Jaimon
Electronics, Cochin University of Science and Technology, Kochi, India

6/11 上午 11:00 報告發表的論文 “Broadband DR-loaded planar monopole”。此研究乃是利用介質共振器作為輻射體，取代原本金屬輻射體，將原本在微帶線上的傳導電流，轉換成位移電流而輻射，類似一個單極天線。操作在高頻時能夠有效減少金屬功率損耗，以增加輻射效率。在低頻時，有接近全方向性的輻射場型；當頻率升高的時候，由於介質共振器高階模態被激發，使得輻射場型在 H 平面成為橢圓形。研究中亦發現，當介質長度逐漸增加，其對頻率改變的影響較不明顯，且發現在單極天線底部的介質能夠有效地把傳導電流轉換成位移電流，而當介質移至單極天線末端，其效果則不明顯。未來改善輻射場型的方法，可以嘗試改變介質的形狀，或嘗試在介質表面貼上一些帶狀金屬。其他類似的研究有 “Modeling and experimental study of dielectric loaded monopoles for UWB applications”，此研究係將介質覆蓋於矩形單極天線之矩形金屬面上，藉由調整介電常數與介質大小以獲得最大頻寬。

Session: 230 **11:45-13:45** **Coconut Grove (Interactive Forum)**

Broadband Dielectric Resonator Antennas

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C. L. Tsai[1], S. M. Deng[1], T. W. Chen[2], Y. C. Chang[1]
[1]Dept. of Electronics Engineering, Ming-Chuan University, Taipei,Taiwan, Taiwan
[2]Materials Research Laboratories, Industrial Technology Research Institute, Hsinchu, Taiwan, Taiwan

IF230.2 A CPW Fed Broadband Dielectric Resonator Antenna Array for WALN Applications at 802.11a/j.....2730
H. Yu
Beijing University of Posts and Telecommunications, Beijing, China

IF230.3 Bandwidth Enhancement by Merging Resonant Modes of Dielectric Resonator Antenna.....2733
T. -H. Chang, J. -F. Kiang
Dept. Electrical Eng. and Grad. Inst. Commun. Eng., National Taiwan University, Taipei, Taiwan

IF230.4 Ultra-Wideband Dielectric Rod Antenna with Biconical Dipole and Reflector.....2737
M. D. Blech, M. M. Leibfritz, T. F. Eibert
Institute of Radio Frequency Technology, Stuttgart, Germany

這次的Poster是在隔壁飯店的草坪上進行，11:45-13:45 期間大家齊聚在這裡，報告者把海報貼在草坪四周的壁板上，與會者則拿著準備好的午餐，隨意挑張餐桌，或是可以邊吃邊瀏覽有興趣的研究主題，有任何問題則可以直接詢問報告者。報告者必須頂著艷陽，站在海報前兩個小時，回答所有的問題。由於擔心一離開便有與會者好奇前來，所以片刻也不敢離開，也沒有時間吃午餐。這次發表的研究主題是「Bandwidth enhancement by merging resonant modes of dielectric resonator antenna」，是利用矩形介質共振器天線的TE_{111}、TE_{112}與TE_{113}三個模態，雖然TE_{112}模態在*H*平面的輻射場型與其他兩者不同，本研究設計該介質的長、寬與高比例，使得三個模態的共振頻率相近，以利用TE_{111}與TE_{113}模態補償TE_{112}模態，使得天線在阻抗頻寬內有良好的增益。再者，在介質內挖一不對稱的溝槽，不僅可以增加頻寬，也可以增加天線在H平

面上的增益，使天線在頻帶內有broadside的輻射場型。對介質共振器天線有興趣的同行曾問為什麼可以用TE_{112}模態，或是詢問實驗與模擬的誤差可能的原因，或是詢問介質與接地面的縫隙對天線的影響等等。

其他寬頻介質天線的作法，如 “Ultra-wideband dielectric rod antenna with biconical dipole and reflector”，利用雙偶極天線饋入錐狀、低介電常數的陶瓷，以在介質內激發行進波而逐漸輻射，具有 3-10 GHz 的頻寬與高指向性，且在波束面上有極佳的等相位面，可以做為地面探測天線等用途。

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Slot Loaded UWB Monopoles and Dipoles

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[1]ESAT/TELEMIC, Catholic University of Leuven, Leuven, B-3001, Belgium
[2]MCP/DARTS, IMEC, Leuven, B-3001, Belgium

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[1]Electrical and Computer Engineering Department, South Dakota School of Mines and Technology, Rapid City, SD, United States
[2]School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA, United States

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J. -K. Kim, S. -K. Ryu, D. -H. Lee, I. -H. Hwang
ETRI(Electronics and Telecommunications Research Institute), Daejeon, South Korea

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[1]ECE, Georgia Institute of Technology, Atlanta, GA, United States
[2]NASA Glenn Research Center, Cleveland, OH, USA

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Radio communications engineering, Korea Univ., seoul, South Korea

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S. Sadat[1], S. D. Seyed Javan[2]
[1]Antenna & Propagations, Iran Telecommunication Research Centre, Tehran, Iran
[2]communications, Islamic Azad University of Mashhad, Mashhad, Iran

關於 UWB antenna 的研究，目前大部分的 UWB 天線大多屬於平面單極天線，差別只在於輻射體形狀的改變，如圓形、橢圓形、環形、矩形等，也有較多的參數可以調整其頻寬。或改變接地面的大小、形狀，來改善其輻射場型。以目前所發表的 UWB 天線，其在低頻時的輻射場型大多仍能維持全方向性；然而當頻率逐漸升高，在水平面的輻射場型大多會變形，而不再是全方向性，因此適合應用在較短距離的傳輸。由於 UWB 頻帶涵蓋 3-10 GHz，為了減少與其他系統的互相干擾，某些研究在輻射金屬面上挖去部分金屬形成溝槽，產生一個止帶(band notch)，以防止干擾，而溝槽的形狀包含矩形、U 型和雙 U 型。其中在 “Study of circular CPW-fed slot antenna with a resistive load” 中，在圓形的金屬天線上挖一矩形溝槽，並在溝槽中加一電阻做為負載，可降低天線的共振頻率，並達到寬頻的效果。

目前部份的研究利用 MEMS 技術製作薄膜式可變電容，作為天線的負載，利用電壓改變電容，進而改變天線的操作頻率或是輻射場型。其反應時間約為數個毫秒。或利用 stubs 改變天線的負載，使天線能適應各種不同環境。

RFID是一個具有產業價值的研究主題，有多個Sessions都在探討相關的研究。RFID將來可以應用在物流業及商品貨物的管理，可減少所需人力，並大幅提高精確度與效率，減少清點所需花費的時間。RFID系統一般具有接收及發射天線與IC電路，天線將接收的訊號轉換成電能，透過傳輸線送至IC電路，訊號經過處理後再將送至天線輻射出去，因此天線與IC之間的阻抗匹配將影響RFID的效能。目前RFID可使用UHF頻帶，適用於較遠的可讀範圍。再者，RFID的體積要小，才有商業應用的價值，因此天線的大小與匹配電路便受到面積的限制。嘗試的天線有Yagi-Uda 天線，因其具有較高的指向性，可以延伸可讀取範圍，其10 dB頻寬約為50 MHz。由於RFID tag有時須緊貼著金屬面或其他介質表面，對天線的輻射產生影響，進而影響RFID tag的可讀取範圍。亦有研究是利用slot antenna作為RFID的天線，具有全方向性的輻射場型。

部分天線屬於軍事應用，例如把天線製作在衣服或鋼盔上，其天線的材質、設計方法、考量的因素，都和一般天線不同。例如像纖維狀的天線，可和衣服一起織造，利用衛星就可以得知穿戴者的所在位置。

這次會議的所有論文都放在一張光碟裡面，減少與會者的負擔，不需攜帶著厚重紙本跑場。但需要電腦才能開啟，沒帶電腦的人就無法事先查閱，或是聽報告的時候無法立即參照，有點不方便。其次，飯店的大廳有點小，每到休息的時候，所有的人幾乎都出現在走道或大廳，有點擁擠。

Broadband DR-Loaded Planar Monopole

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Introduction

Many approaches have been proposed to broaden the impedance bandwidths of monopoles. A common way is to replace the radiating wire with elements of different shapes to increase the radiating surface areas and impedance bandwidth [1], [2]. Since the current is concentrated on the outer edge of a planar monopole, the broadband characteristics are maintained when a hole is drilled off a planar monopole to form an annular strip [3]. Moreover, resonant elements can be embedded within annular planar monopoles to provide band-notched characteristics [4].

Printed monopoles with different shapes have been proposed proposed to provide broadband width [5], [6], dual-band [6], [7], and band-notched characteristic [8]. Printed monopoles can have a wider impedance bandwidth than wire monopole. However, the radiation pattern is deteriorated at higher frequency.

In this work, a compact monopole made of dielectric resonator (DR) is proposed. The conduction current in the microstrip line is transformed to the displacement current in the DR. The impedance bandwidth covers 5.745-14.94 GHz, over which the E_θ pattern on the xy-plane is nearly omnidirectional.

1 Design and Implementation

Fig. 1 shows the configuration of the DR-loaded planar monopole. A microstrip line of width w_m is extended over the ground plane by p and attached to a rectilinear dielectric resonator. A strip extended from the microstrip line is bent vertically and adhered on one side of the DR. The antenna is fabricated on an FR4 substrate of size $W_g \times L_g$ and thichness t.

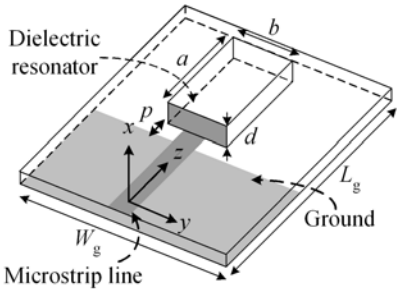
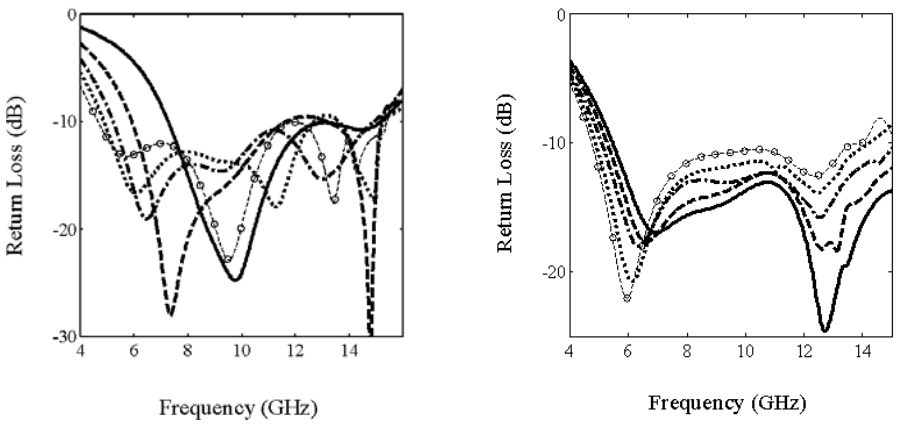


Figure 1: Panoramic schematic of DR-loaded planar monopole .

Fig. 2(a) shows the effect of the DR length a on the resonant frequency. The first



(a) (b)

Figure 2: Return loss of DR loaded planar monopole, $b = 5.34$ mm, $d = 2.5$ mm, $w_m = 1.15$ mm, $t = 0.6$ mm, (a) a effect, $p = 1.5$ mm, —: $a = 1$ mm, - - -: $a = 4$ mm, -·-: $a = 7$ mm, $\cdots$: $a = 10$ mm, -o-: $a = 16$ mm, (b) p effect, $a = 8$ mm, —: $p = 1.1$ mm, - - -: $p = 1.3$ mm, -·-: $p = 1.5$ mm, $\cdots$: $p = 1.7$ mm, -o-: $p = 1.9$ mm.

resonant frequeny decreases from 9.8 to 5.8 GHz as the length a is increased from 1 to 16 mm. Note that the decrease rate of resonant frequency slows down when the length a becomes larger. The DR acts as a monopole radiator, having stronger electric field near its feeding strip and weaker field at its end. The second resonant frequency is basically determined by the dimension of DR since the DR resonates at its higher-order mode. Fig. 2(b) shows the effects of gap p on the impedance and the resonant frequency. The effect of gap p has been discussed in [3], [5]. The first resonant frequency is reduced as the gap p is increased.

By tuning the gap p and adjusting the size of the loaded DR, the input impedance can be matched well. Fig. 3 shows the return loss of the proposed DR-loaded monopole. The measurement and simulation match reasonably well. The 10-dB impedance bandwidth covers 5.745-14.94 GHz. The bandwidth is achieved by merging by two resonant bands around at $f = 6.525$ and $f = 11.92$ GHz.

Fig. 4 shows the electric field distribution in the DR at these two resonant frequencies. The electric field distribution at the first resonant frequency is mainly in the z-direction, parallel to the current direction on the microstrip line. The antenna radiates a stronger E_θ component than the E_ϕ component on the xy-plane. The electric field distribution at the second resonant frequency shows two loops, and the radiated E_θ component is also stronger than the E_ϕ component.

Fig. 5 shows the measured and simulated radiation patterns of the DR-loaded planar monopole. It is observed that the E_θ component on the xy-plane (H-plane) is stronger than the E_ϕ component over the 10-dB bandwidth in almost all directions.

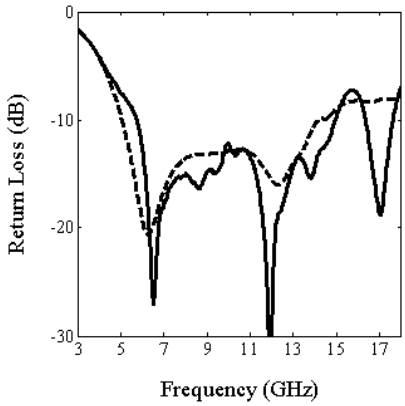
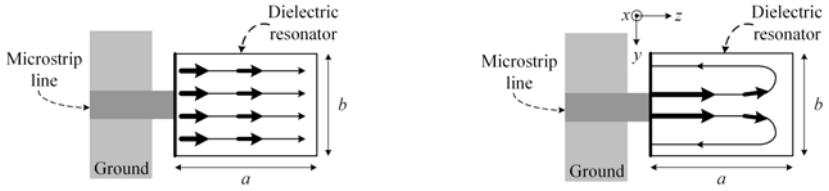
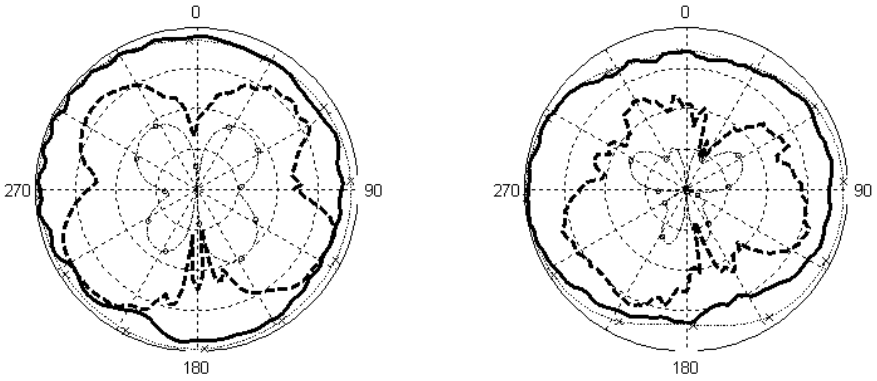


Figure 3: Return loss of DR loaded planar monopole, —: measurement, - - -: simulation, $a = 7.86$ mm, $b = 5.34$ mm, $d = 2.5$ mm, $p = 1.4$ mm, $w_m = 1.15$ mm, $t = 0.6$ mm.



(a) (b)

Figure 4: Electric field distributions inside the DR, (a) $f = 6.525$ GHz, (b) $f = 11.92$ GHz.



(a) (b)

Figure 5: Measured and simulated radiation patterns on the yz-plane, (a) $f = 6.5$ GHz, (b) $f = 11.865$ GHz, —: measured E_θ, - - -: measured E_ϕ, -×·: simulated E_θ, $\cdots \circ \cdot$: simulated E_ϕ, 10-dB per division on radials, all parameters are the same as in Fig. 3.

Conclusions

A broadband DR-loaded planar monopole is proposed with 10-dB impedance bandwidth over 5.745-14.94 GHz. A nearly omnidirectional radiation pattern of vertical polarization on the xy-plane is obtained. The antenna size is 8 mm $\times$ 5.5 mm $\times$ 2.5 mm.

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Bandwidth Enhancement by Merging Resonant Modes of Dielectric Resonator Antenna

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Introduction

Dielectric resonators (DR) have the merits of high efficiency and low loss [1]. Compared to the conventional microstrip antenna, the DR antenna features a wider impedance bandwidth since the latter radiates through multiple facets of the DR. The radiation pattern of DR is determined by the field distribution on the DR surface. Hence, different radiation patterns can be obtained by exciting proper resonant modes.

Different approaches have been proposed to increase the bandwidths of DRs. For example, stacking two cylindrical DRs of different sizes to merge their resonant bands [2], attaching parasitic metal strips on DR surface to incur additional resonance [3], leaving air gaps between a DR and the ground plane to incur more effective radiation [4], adjusting the aspect ratio of a DR to reduce its Q factor [5], modifying the DR shape to create discontinuities [6], [7], and so on.

In this work, a broadband DR antenna is designed by merging three resonant modes. The radiation patterns of the mixed modes are studied. A wide impedance bandwidth of 29% and a broadside radiation pattern of vertical polarization on the xy-plane are achieved.

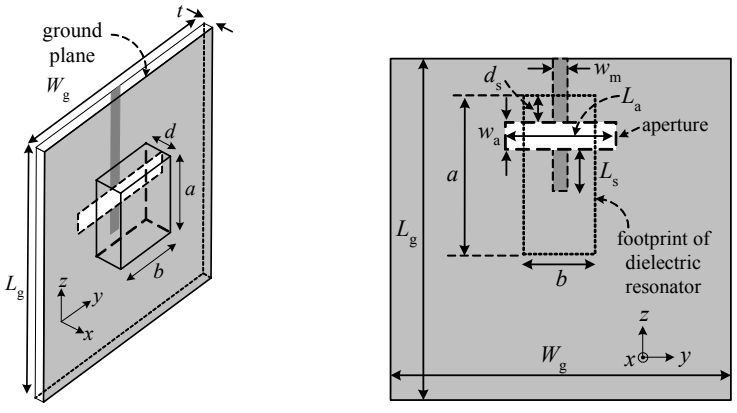
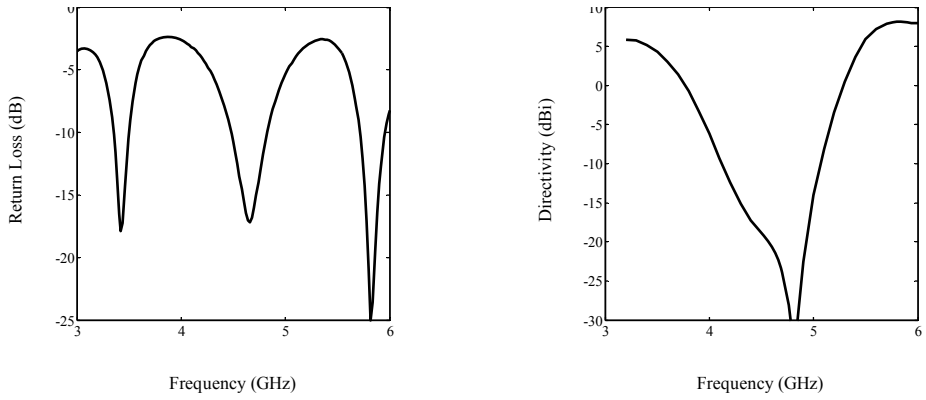


Figure 1: (a) A rectangular DR on a ground plane, (b) schematic .

1 Design and Implementation

Fig. 1 shows a rectangular DR fed by a microstrip line through a coupling aperture. The dimension of the DR is $a \times b \times d$, and the coupling aperture has dimension of $L_a \times w_a$. The relative position between the aperture and the DR is d_s, and the length of microstrip stub over the aperture is L_s. The ground of dimension $W_G \times L_g$ is fabricated on an FR4 substrate of thickness t.



(a) (b)

Figure 2: (a) Simulated return loss of a rectangular DR, (b) directivity of E_θ at $\theta = 90°$, $\phi = 0°$, $a = 20$ mm, $b = 8$ mm, $d = 10$ mm, $d_s = 11$ mm, $w_a = 1$ mm, $L_a = 7$ mm, $L_s = 4$ mm, $W_g = L_g = 70$ mm.

The DR with ground plane is equivalent to an isolated DR of dimension $a \times b \times 2d$ in free space. Based on the dielectric waveguide model, which two opposite surfaces are assumed to be total reflection boundaries in while the other four sides behave like PMC walls, we have $k_x = \pi/2d$, $k_z = m\pi/a$, and k_y is determined by [8]

$$\frac{k_y b}{2} = \tan^{-1}\left(\frac{\sqrt{k_x^2 + k_z^2}}{k_y}\right) \tag{1}$$

The resonant frequency can thus be determined as

$$f_r = (c/\sqrt{\epsilon_r})\sqrt{k_x^2 + k_y^2 + k_z^2}. \tag{2}$$

Consider a rectangular DR of dimension 20 mm × 8 mm × 10 mm, the resonant frequencies of the TE^y_{111}, TE^y_{112}, and TE^y_{113} modes are 3.2, 4.53, and 6.1 GHz, respectively, by using (2). By tuning the coupling aperture size $L_a \times w_a$ and the microstip stub length L_s, the input impedance can be matched well, and the three modes can be excited simultaneously, as shown in Fig. 2(a) by using HFSS. The nulls of the return loss occur at $f = 3.42$ GHz, 4.66 GHz, and 5.82 GHz, which are associated with the resonant frequencies of the TE^y_{111}, TE^y_{112}, and TE^y_{113} modes, respectively.

It is well known that the TE^y_{111} and TE^y_{113} modes of a rectangular DR incur broadside radiation patterns of vertical polarization on the xy-plane. On the other hand, the

directivity of the E_θ pattern associated with the TE^y_{112} mode is close to zero around $\theta = 90°$. Fig. 2(b) shows the directivity of the E_θ pattern at $\theta = 90°$, $\phi = 0°$. Since the opposite electric field on the top surface of the DR cancels to each other at $\theta = 90°$, the directivity around the resonant frequency of the TE^y_{112} mode is significantly decreased.

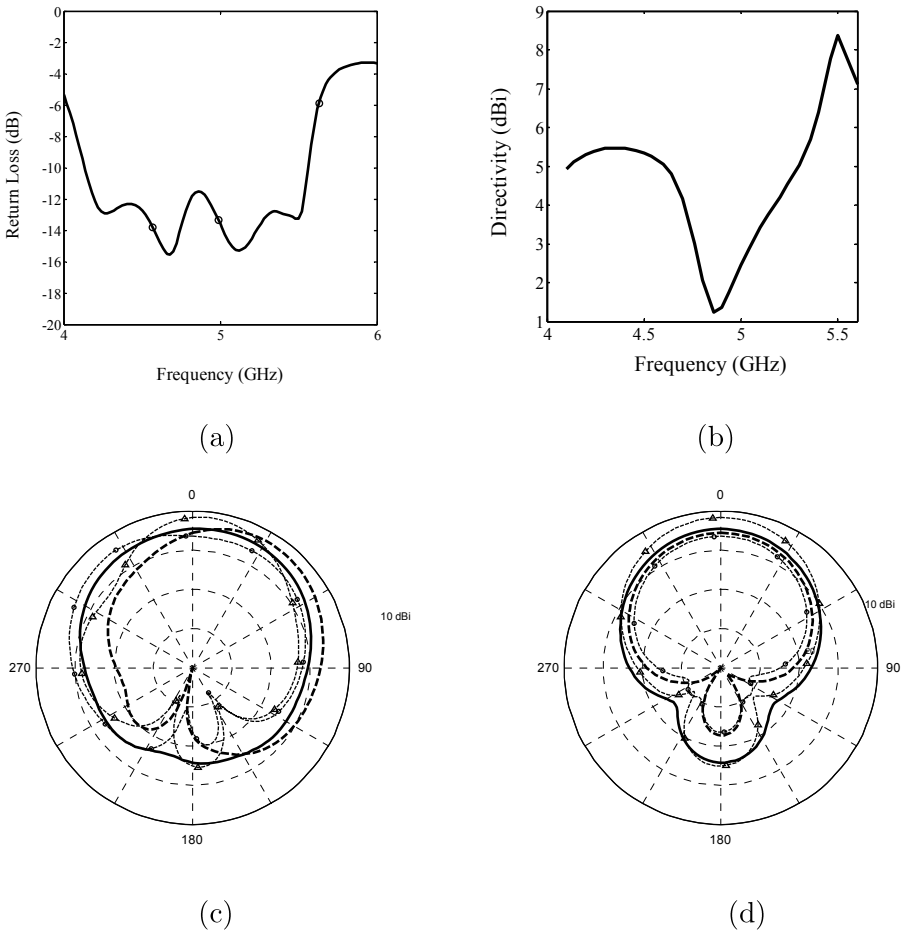


Figure 3: (a) Return loss of a rectangular DR, ∘ marks the resonant frequencies of TE^y_{111}, TE^y_{112}, and TE^y_{113} modes, respectively, (b) directivity of E_θ at $\theta = 90°$ and $\phi = 0°$, and directivity of E_θ pattern (dBi) on the (c) xz-plane, (d) xy-plane, —: $f = 4.26$ GHz, - - -: $f = 4.68$ GHz, $-\circ-$: $f = 5.12$ GHz, -△-: $f = 5.5$ GHz, 10-dB per division on radials, $a = 29$ mm, $b = 19$ mm, $d = 4$ mm, $d_s = 11$ mm, $w_a = 1$ mm, $L_a = 7$ mm, $L_s = 3.5$ mm, $W_g = L_g = 70$ mm.

If the resonant bands of these three modes are merged, the directivity of E_θ pattern on the xy-plane around the resonant frequency of the TE^y_{112} mode can be increased to some extent. Hence, merging the resonant bands of the TE^y_{111}, TE^y_{112}, and TE^y_{113} modes can achieve a wide bandwidth in both impedance and radiation pattern.

Consider a rectangular DR of dimension 29 mm × 19 mm × 4 mm, the resonant frequencies of the TE^y_{111}, TE^y_{112}, and TE^y_{113} modes are 4.573 GHz, 5 GHz, and 5.637 GHz. Fig. 3(a) shows the return loss of the DR antenna. The nulls of return loss do not occur at the resonant frequencies of the resonant modes due to mode coupling

and the feeding structure. Since the three resonant frequencies are close enough, their bands are merged to form an impedance bandwidth of 29%.

Fig. 3(b) shows the directivity at $\theta = 90°$, $\phi = 0°$. Note that the directivity at the frequency around resonant frequency of the TE^{y}_{112} mode is raised to certain extent.

Figs. 3(c) and 3(d) show the directivity of the E_θ pattern on the xz-plane and xy-plane, respectively, at different frequencies. A broadside radiation pattern is observed over the bnad. The directivity of the E_θ pattern at $\theta = 90°$ and $\phi = 0°$ is slightly reduced as $f = 5.12$ GHz. The E_θ pattern is changed as the frequency is increased, however, its maximum roughly keeps at $\theta = 90°$. Hence, the directivity on the xy-plane is not significantly reduced.

Conclusions

In this work, the resonant bands of different modes in a rectangular DR is mergerd to achieve a wide bandwidth in both impedance and radiation pattern. The antenna can be used for WLAN applications in an indoor environment.

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