CMOS exponential function generator

Weihsing Liu and Shen-Iuan Liu

A new CMOS exponential function generator is presented. The proposed circuit is compact, with low power and wide dynamic range. The proposed circuit has been fabricated in a 0.50 μm CMOS process. Experimental results show that the output range of the proposed exponential function generator can be more than 15 dB with the liner error less than ±0.5 dB. The supply voltage is ±1.5 V and the power dissipation is less than 0.4 mW. Experimental results are given to demonstrate the proposed circuit.

Introduction: The exponential function generator is one of the important building blocks in a variable gain amplifier (VGA) [1]. However, unlike the BJT device, there is no intrinsic logarithmic device working in saturation for CMOS technologies. To realise the exponential function, the approximated Taylor's series expansion [2–4] can be utilised. Alternatively, a pseudo-exponential function [5, 6] can be used to generate the required exponential function. In this Letter, a new CMOS pseudo-exponential function generator is presented and the experimental results are given to verify the theoretical analysis.

Design principle and circuit implementation: The pseudo-exponential function $f(x)$, which can mimic the exponential function $\exp(2x)$ [6], is expressed as

$$f(x) = \frac{1+x}{1-x} \simeq \exp(2x) \quad \text{if } |x| < 1 \tag{1}$$

The comparison between the pseudo-exponential function and $\exp(2x)$ is shown in Fig. 1. The Figure shows that as x varies from −0.4 to 0.4, the output dynamic range can be more than 15 dB while the difference between $f(x)$ and $\exp(2x)$ is within ±0.5 dB.

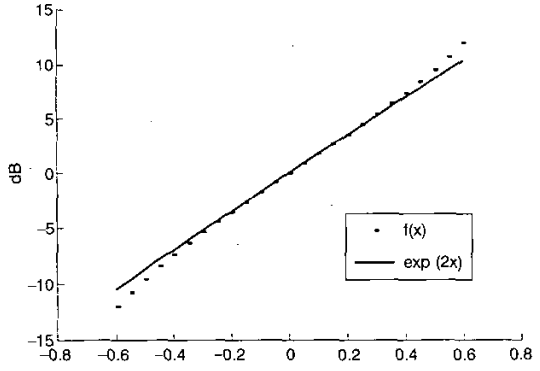

Fig. 1 *Comparison between function $f(x) = (1+x)/(1-x)$ and $\exp(2x)$*

The proposed CMOS pseudo-exponential function generator is shown Fig. 2. Assume that both transistors M1 and M2 are biased in the triode region without body effect. The source currents I_1 and I_2 can be expressed as

$$I_1 = \frac{K_{n1}}{2}(2(-V_{SS} - V_{Tn1})V_{DS1} - V_{DS1}^2) \tag{2}$$

and

$$I_2 = I_b + I_{\text{in}} = \frac{K_{n2}}{2}(2(V_{G2} - V_{SS} - V_{Tn2})V_{DS2} - V_{DS2}^2) \tag{3}$$

where I_b is a reference current, $K_{n1,2}$ are the transconductance parameters and $V_{Tn1,2}$ are the threshold voltages of M1 and M2, respectively. The current mirror, M5 and M6, is used to duplicate the current I_1 as

$$I_1 = I_3 = I_4 \tag{4}$$

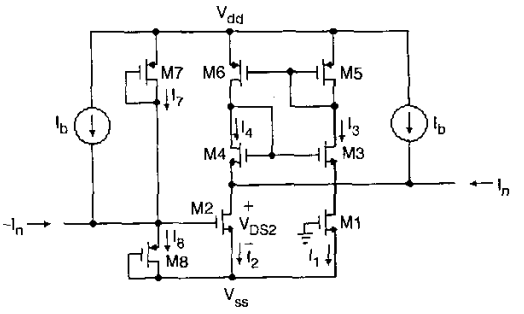

Fig. 2 *Proposed exponential function generator*

Assume that M3 and M4 are perfectly matched (i.e. $K_{n3} = K_{n4}$ and $V_{Tn3} = V_{Tn4}$) and both are biased in saturation. According to the square-law characteristics of MOSFETs, the following equation can be obtained

$$V_{GS3} = V_{GS4} = \sqrt{\frac{2I_1}{K_{n3}}} + V_{Tn3} \tag{5}$$

According to (5) and $V_{GS3} + V_{DS1} = V_{GS4} + V_{DS2}$, one can have

$$V_{DS1} = V_{DS2} \tag{6}$$

Since the source voltages of M3 and M4 are equal (i.e. $V_{SB3} = V_{SB4}$), one can find $V_{Tn3} = V_{Tn4}$. Substituting (2), (4) and (6) into (3) and assuming that M1 and M2 are perfectly matched (i.e. $K_{n1} = K_{n2} = K_n$ and $V_{Tn1} = V_{Tn2} = V_{Tn}$), one can have

$$I_b + I_{\text{in}} \simeq K_n \cdot V_{G2} \cdot V_{DS2} \tag{7}$$

A current-to-voltage converter is composed of M7 and M8 [7]. Assume that M7 and M8 are perfectly matched (i.e. $K_{p7} = K_{p8} = K_p$ and $V_{Tp7} = V_{Tp8} = V_{Tp}$) and both are embodied in individual wells to avoid the body effect. If the supply voltages $V_{DD} = |V_{SS}|$, the gate voltage can be expressed as

$$V_{G2} = \frac{I_8 - I_7}{2K_p(V_{DD} - |V_{Tp}|)} = \frac{I_b - I_{\text{in}}}{2K_p(V_{DD} - |V_{Tp}|)} \tag{8}$$

Substituting (8) into (7) and comparing to (1) yields

$$\begin{aligned} V_{DS2} &= \frac{2K_p(V_{DD} - |V_{Tp}|)}{K_n} \cdot \frac{I_b + I_{\text{in}}}{I_b - I_{\text{in}}} \\ &= \frac{2K_p(V_{DD} - |V_{Tp}|)}{K_n} \cdot \frac{1 + I_{\text{in}}/I_b}{1 - I_{\text{in}}/I_b} \\ &\simeq \frac{2K_p(V_{DD} - |V_{Tp}|)}{K_n} \cdot \exp\left(\frac{2}{I_b} I_{\text{in}}\right) \end{aligned} \tag{9}$$

Therefore, a pseudo-exponential function generator can be realised.

Experimental results: The proposed circuit has been fabricated in a 0.5 μm CMOS process. The die photograph is shown in Fig. 3. The aspect ratios of all the transistors for the proposed circuit are $(W/L) = (1\ \mu\text{m}/1\ \mu\text{m})$ and the experiments were performed with supply voltages $V_{DD} = |V_{SS}| = 1.5$ V. The experimental results of the proposed pseudo-exponential function generator are shown in Fig. 4. With the reference current $I_b = 40$ μA, when I_{in} varies from −30 to 15 μA, the output dynamic range could be more than 15 dB while the linearity error is within ±0.5 dB and the power dissipation is less than 0.4 mW. The experimental results confirm the theoretical analysis calculated by (9).

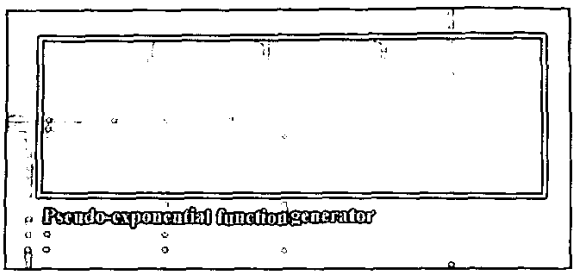

Fig. 3 *Die photo of proposed exponential function generator*

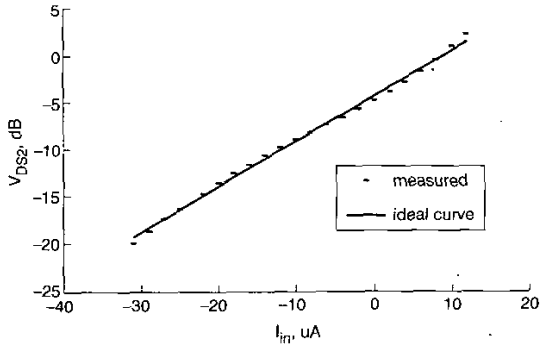

Fig. 4 *Experimental results of proposed exponential function generator*

Conclusion: A new CMOS pseudo-exponential function generator has been developed. Experimental results have been given to confirm the validity of the theoretical analysis. The proposed circuit is expected to be useful in the design of VGA and other analogue signal processing applications.

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Combined radix<2 and 1.5 bit/stage pipelined analogue-to-digital converter

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A new pipeline architecture that combines the radix<2 and traditional 1.5 bit gain-stages is presented. The 10 bit, 60 MHz, 3 V pipelined analogue-to-digital converter has been designed in a 0.25 μm 1P4M CMOS technology using digital self-calibration. The converter achieves more than 57 dB SNDR from a 3 V supply (10% lower than nominal 3.3 V) within −40 to +120°C temperature range.

Introduction: The 1.5 bit/stage pipelined analogue-to-digital converter (ADC) is almost the most power efficient architecture, but suffers from a complicated and long digital self-calibration period. This is a drawback because digital self-calibration has become more attractive for modern deep submicron CMOS technologies, in which the implementation of a digital circuit is becoming easier and faster. The radix<2 architecture has the advantage of having a simpler digital self-calibration but is more sensitive to circuit non-idealities. It also requires a higher number of stages compared to its 1.5 bit/stage counterpart, leading to larger power dissipation. In this Letter, a combined architecture of radix<2 and 1.5 bit/stage is presented. The few first stages make use of radix<2 architecture and digital self-calibration, while the remaining stages use 1.5 bit/stage in which no calibration is employed. This architecture minimises the power dissipation, while requiring a simpler digital self-calibration. The presented 10 bit, 60 MHz, 3.3 V ADC consumes 50 mA in 3.0 V supply (10% lower than nominal voltage) and achieves >57 dB SNDR in all process corner cases and temperature ranges. The IM3 of the converter is >60 dB.

Converter architecture: The first four stages have different radix factors as 1.4, 1.8, 1.75 and 1.75 while the remaining nine stages are traditional 1.5 bit/stage. Overall there are 14 raw bits, four from the radix stages, and ten from the rest. The ADC output number associated with its full-scale level is 8180 out of which 3 bits are truncated resulting in 1024 levels (10 bit) at the output of the calibration/error-correction unit. Fig. 1 shows the corresponding weights of the raw bits, the ADC architecture, and the digitally calibrated stages. The ten least significant bits come from the overlapped 9 bit-pairs of the 1.5 bit/stage stages. Fig. 1 shows the full-scale range from $-V_{ref}$ to $+V_{ref}$ divided into 8180 codes by the ADC. The corresponding code of $-V_{ref}$ is 0 and that of $+V_{ref}$ is 8180. System level Monte-Carlo simulations using Matlab show that including non-idealities the converter achieves <0.05 LSB DNL and INL after calibration.

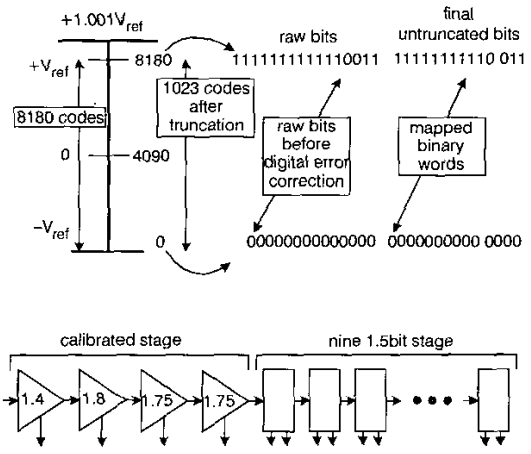

Fig. 1 *Architecture of proposed ADC, bit weights, and full-scale distribution of codes*

Radix<2 gain-stage architecture and calibration: Fig. 2 shows the input–output transfer function of the first four stages as well as the