5.7 GHz low-power variable-gain LNA in 0.18 μm CMOS

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A variable-gain low-noise amplifier (LNA) suitable for low-voltage and low-power operation is designed and implemented in a standard 0.18 μm CMOS technology. With a current-reused topology, the common-source gain stages are stacked for minimum power dissipation while achieving high small-signal gain. The fully integrated 5.7 GHz LNA exhibits 16.4 dB gain, 3.5 dB noise figure and 8 dB gain tuning range with good input and output return losses. The LNA consumes 3.2 mW DC power from a supply voltage of 1 V. A gain/power quotient of 5.12 dB/mW is achieved in this work.

Introduction: The convenience introduced by the use of portable wireless devices has drastically influenced the way people communicate. Owing to the increasing demands on the wireless services, it is desirable to implement RF front-ends with lower cost and higher level of integration. With the advances in the high-frequency characteristics of both active and passive devices, CMOS technology has recently attracted great attention for the implementation of RF circuits. Though exhibiting the potential for applications at multi-gigahertz frequencies, CMOS RF designs typically involve higher power dissipation owing to the inherently low transconductance of the MOSFETs. In addition, conventional CMOS RF circuits also impose restrictions on the supply voltage, and the performance degrades significantly as the supply voltage decreases. Therefore, effort has been made to develop low-power and low-voltage techniques for CMOS RF circuits [1–6]. In this Letter, a 5.7 GHz fully integrated variable-gain LNA is presented. By using current-reused cascaded stages, the LNA is designed for high gain with low power consumption and low supply voltage.

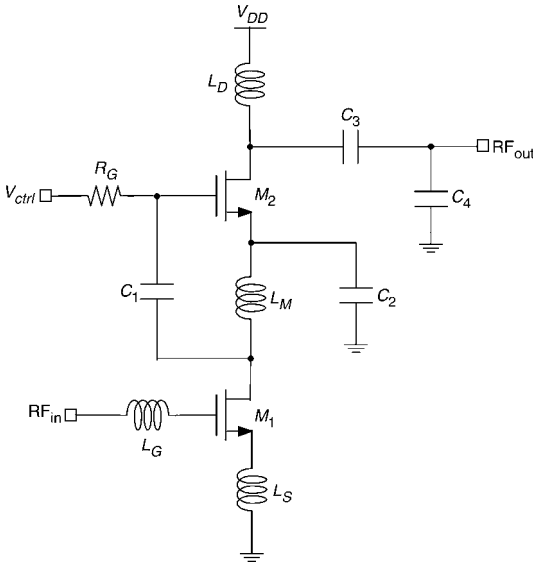

Fig. 1 *Schematic of variable-gain LNA*

Circuit design: The schematic of the LNA with all on-chip components is shown in Fig. 1. With M_1 and M_2 sharing the same bias current, the total power consumption of the current-reused amplifier is minimised. To achieve higher gain than a conventional cascade LNA, both M_1 and M_2 are in common-source configurations. The design considerations of the current-reused LNA are similar to those of a cascaded amplifier. The gate width and the bias current of the transistors are chosen to maximise the transconductance while maintaining low-power requirement. In the design of the input stage M_1, source-degeneration L_S and gate inductance L_G are employed for the input matching. The small-signal equivalent circuit of the input stage is shown in Fig. 2, where R_o is the output resistance of M_1 and C_{in2} is the input capacitance of M_2. Trade-off has been made between impedance matching and noise matching in determining the inductances L_S and L_G. As can be seen in Fig. 2, the load of the input stage is composed of parallel connection of R_o, L_M and C_P. In this design, L_M is chosen to resonate with C_P at the frequency of interest. With the parallel resonance at the drain of M_1, the gain of the input stage is enhanced regardless of the input capacitance of the second stage. As a result, the overall noise figure is reduced owing to the suppression of the noise contribution from the second stage. In addition, L_M and C_1 are also used as the inter-stage matching between M_1 and M_2. The output matching network is composed of L_D, C_3 and C_4, providing broad band impedance matching of the LNA. The gain-controlled mechanism is achieved by adjusting the bias voltage at the gate of M_2. As the gate voltage of M_2 decreases, the drain voltage of M_1 is suppressed, moving the transistor bias out of its high gain region. Therefore, the variable gain of the LNA is obtained without significant degradation in the input and output return losses. The fully integrated LNA is fabricated in a standard 0.18 μm CMOS technology. Fig. 3 shows the micrograph of the fabricated LNA with a chip area of 810 × 720 μm.

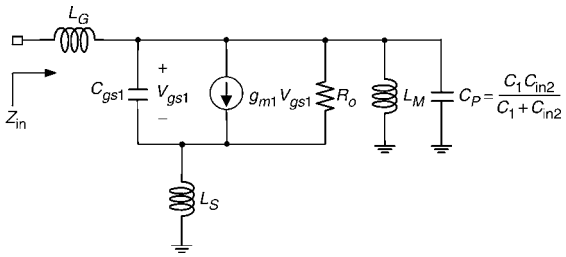

Fig. 2 *Small-signal equivalent circuit of input stage*

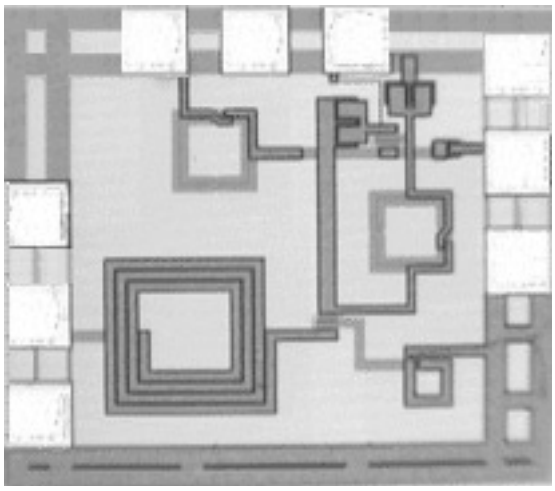

Fig. 3 *Micrograph of fabricated LNA*

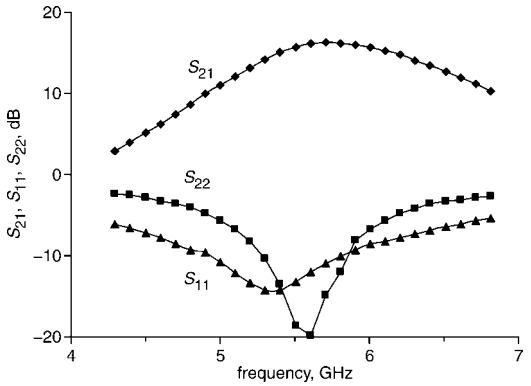

Fig. 4 *Measured S-parameters and noise figure*

Experimental results: On-wafer probing was performed to characterise the *S*-parameters and the noise figure of the LNA. Fig. 4 shows the measured results. Consuming a DC power of 3.2 mW from a 1 V supply, the LNA exhibits 16.4 dB gain and 3.5 dB noise figure at 5.7 GHz. The input and output reflection coefficients are −11 and −15 dB, respectively. With the current-reused gain stages and inter-stage parallel resonance, a gain/power quotient, which is frequently

used as the figure-of-merit for low-power design, of 5.12 dB/mW is achieved at 5.7 GHz in this work. The gain and noise figure of the LNA against various control voltages are shown in Fig. 5. As can be seen, a gain tuning range of 8 dB is achieved with insignificant increase in the noise figure. Comparison of the LNA performance with previously published data [1–5] is summarised in Table 1.

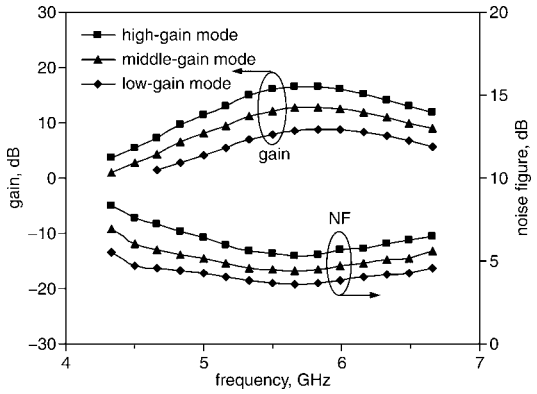

Fig. 5 *Measured gain and noise figure for various control voltages*

Table 1: Comparison of LNA performance with previously published data

Technology	Frequency (GHz)	V_{DD} (V)	Gain (dB)	NF (dB)	Pdc (mW)	Gain/Pdc (dB/mW)	Ref.
0.18 µm CMOS	5.7	1.0	16.4	3.5	3.2	5.12	This work
0.35 µm SOI	1.6	0.6	6.4	2.5	1.2	5.33	[1]
90 nm CMOS	5.5	0.6	11.2	3.2	2.1	5.33	[2]
0.18 µm CMOS	5.8	1.0	13.2	2.5	22.2	0.59	[3]
0.18 µm CMOS	5.0	1.0	20.0	3.5	17.0	1.17	[4]
0.18 µm CMOS	5.7	1.8	21.4	4.4	16.2	1.32	[5]

Conclusion: A low-power variable-gain LNA with current-reused topology is designed and fabricated in a standard 0.18 µm CMOS technology. The 5.7 GHz LNA exhibits 16.4 dB gain, 3.5 dB noise figure and 8 dB gain tuning range while consuming a DC power of 3.2 mW from a 1 V supply. It demonstrates the potential of CMOS RF designs for low-power and low-voltage applications at multi-gigahertz frequencies.

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