High-performance Fully Integrated 4 GHz CMOS LC VCO in Standard 0.18-μm CMOS Technology

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Abstract - In this paper, we demonstrate that high Q-factor inductors on normal 750-μm-thick silicon substrate (in standard 0.18-μm CMOS technology) can be achieved by optimization of the layout of the inductors. To study the effect of pattern-ground-shield (PGS) on our designed inductors, we compare the performance of the inductors with and without PGS. In addition, a state-of-the-art 4-GHz CMOS LC voltage-controlled oscillator (VCO) with phase noise of -119.94 dBc/Hz measured at 1 MHz offset frequency is reported.

Index Terms – CMOS, LC, VCO, PGS

I. Introduction

Recently, the on-chip spiral inductor has been extensively studied because it is a must for the fulfillment of single-chip radio. However, the quality (Q) factor of on-chip inductors is low due to losses in the conductive substrate as well as the series resistance of the metallization. Various methods have been reported to enhance the Q factor such as high-resistivity silicon [1], front-side micromachining [2][3], back-side micro-machining [4], porous silicon [5], proton implantation [6]. Most of the proposed methods are very difficult, if not impossible, to be integrated into the standard CMOS technology because they are non-standard processing steps. In addition, the front-side etching has inherent limitations as to how far circuits can be placed from the inductors [3]. Therefore, the CMOS technology compatible patterned ground shield (PGS) method [7], which can improve the Q in the frequency bands of interest, seems to be a better choice.

In this work, the performance of high Q-factor on-chip inductors with and without PGS is reported. In addition, based on these high Q-factor inductors, a state-of-the-art 4-GHz CMOS LC VCO is implemented.

II. Designs of the Inductors and the 4-GHz LC VCO

A. Inductors

To optimize Q-factor, self-resonant frequency (f_{SR}) of the inductors, metal width, metal space, and inner dimension of the inductors were carefully selected based on the simulated results of EM simulation tools of Sonnet Software's SONNET and "Momentum" of Agilent's advanced design system (ADS). Fig. 1 shows the layouts of the 2.5-turn on-chip inductors with PGS (PGS IND) and without PGS (STD IND) implemented in a standard 0.25 μm CMOS process provided by the commercial foundry UMC. The track width and spacing are 20 μm and 2 μm, respectively. The slot spacing and metal strip width of the PGS are both 0.24 μm.

B. 4-GHz LC VCO

CMOS VCOs with integrated inductors are well suited for wireless applications [8], [9]. To prevent the unwanted frequency pulling effect, a VCO operating at twice the carrier frequency with a following divide-by-2 stage can be utilized as the local oscillator in a direct-conversion transceiver. For wireless applications such as DCS, PCS, and WCDMA, a phase noise of -113dBc/Hz at 600 kHz offset from the carrier frequency is the minimum requirement for a 3.8−4.2 GHz VCO. When the operating frequency exceeds 3 GHz, losses caused by the induced eddy current in the silicon substrate begins to degrade the Q-factor of inductors. For LC VCOs, Q of the resonance tank, which is strongly related to the phase noise, will also be pulled down by such painful loss. Therefore, considerable power consumption is usually necessary to maintain an acceptable phase noise performance in VCOs.

Fig. 2 shows the schematic diagram of our designed 3.9-4.2 GHz monolithic low-phase noise CMOS VCO with 7.5 mW DC power consumption by using the standard 0.18 μm CMOS technology. The circuit parameters are: PMOS transistor size: W/L = 300 μm/0.34 μm, resistor size: W/L = 4×10 μm/40 μm, varactor size: W/L = 120μm/1 μm, and inductor value = 0.56 nH. The negative conductance required to sustain a stable oscillation is generated by the cross-coupled PMOS pair. Although a NMOS or CMOS topology seems to be more power-saving, VCO cores consisting of NMOS usually suffer from excess 1/f noise. To prevent the up-conversion of low frequency noise, the tail current is defined by a poly-silicon resistor instead of an FET current source which may contribute considerable 1/f noise.

III. Experimental Results and Discussions

A. Inductors

The frequency-dependent S-parameters measurements were performed from 0.1 GHz to 40 GHz by an HP-8510C network analyzer. The measured Q-factor versus frequency characteristics of the 2.5-turn inductors in Fig. 1 are shown in Fig. 3. PGS increases the Q_{max} of STD IND from 10.7 (at

4.7 GHz) to 12.69 (at 5.1 GHz). While increasing the Q_{max} of STD IND, the PGS IND has a lower self-resonance frequency f_{SR} (11.4 GHz) than that (16.5 GHz) of STD IND.

The measured effective inductance (L_{eff}) versus frequency characteristics of the STD IND and the PGS IND are shown in Fig. 4. The inductances of the two inductors are almost the same (~ 2 nH) at lower frequencies and are kept constant up to 8 GHz and 12 GHz for PGS IND and STD IND, respectively.

The reason why PGS can only improve Q_{max} but deteriorate f_{SR} of an inductor can be explained as follows. Based on the theory introduced in [10], substrate loss factor of Q-factor, specifically Q_{max}, can be improved by making the silicon substrate either close to a short circuit (i.e. PGS, etc.) or close to an open circuit (i.e. substrate transfer etc. [11]). Compared to a normal silicon substrate, a short- and an open-circuited silicon substrate make the equivalent substrate capacitance larger and smaller, respectively, which in turn result in a smaller and a larger f_{SR}, respectively.

B. 4-GHz LC VCO

The die photo of the 4-GHz CMOS LC VCO is shown in Fig. 5. The VCO can operate from 3.9 to 4.2 GHz as shown in Fig. 6. Fig. 7 shows this VCO achieves very good phase noise of -119.94 dBc/Hz at 1 MHz offset frequency. Table I is a summary of the state-of-the-art 4 to 6 GHz CMOS LC VCO, in which the "FOM" means the widely accepted figure-of-merit defined as follows [8].

$$FOM = 10\log\left[\left(\frac{\Delta f}{f_o}\right)^2 \cdot P_{DC}\right] + L(\Delta f) \ \text{(dBc/Hz)}, \qquad (1)$$

where f_o means carrier frequency, Δf means offset frequency, and $L(\Delta f)$ means phase noise. According to table I, the FOM of our VCO is compatible with the reported state-of-the-art 4-6 GHz CMOS LC VCO with a practical tuning range (> ~ 5 %).

IV. Conclusions

In this paper, first, high Q-factor inductors on normal 750-μm-thick silicon substrate in standard 0.18-μm CMOS technology were realized by optimization of the layout of the inductors. Second, PGS was used to further improve the performance of the inductors in the frequency bands of interest. Finally, a state-of-the-art 4-GHz CMOS LC VCO with phase noise of -119.94 dBc/Hz measured at 1 MHz offset frequency is also implemented.

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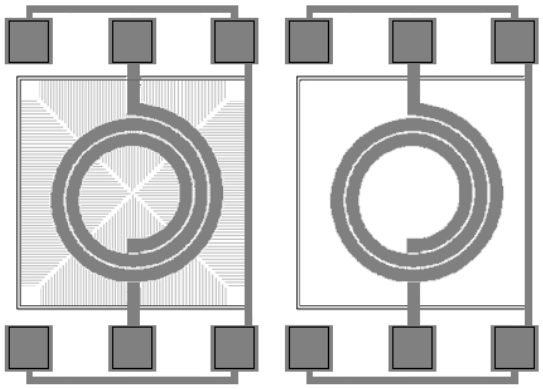

Fig. 1 Layouts of the 2.5-turn on-chip inductors with PGS (PGS IND) and without PGS (STD IND)

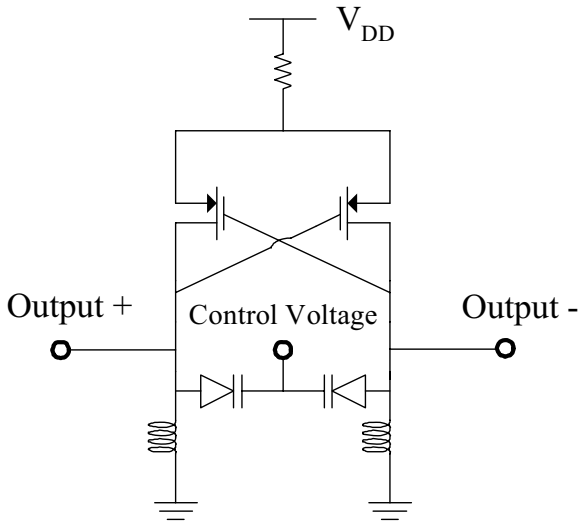

Fig. 2 The schematic of the 4-GHz CMOS LC VCO.

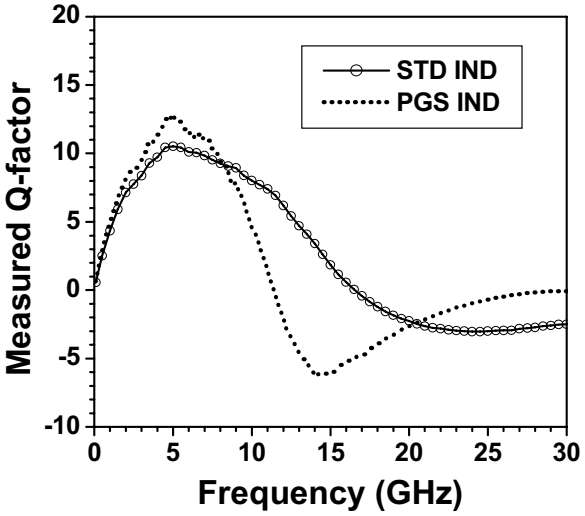

Fig. 3 Measured Q-factor versus frequency characteristics of the STD IND and PGS IND inductors.

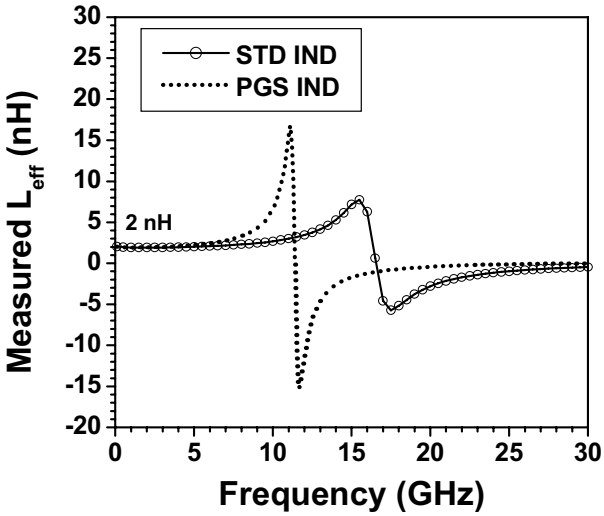

Fig. 4 Measured equivalent inductance (L_{eff}) versus frequency characteristics of the STD IND and PGS IND inductors.

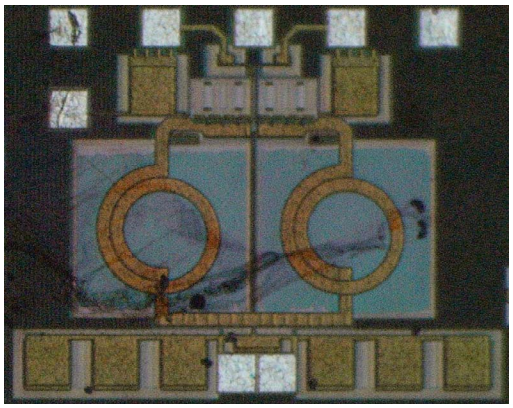

Fig. 5 The front-side die photograph of the 4-GHz CMOS LC VCO.

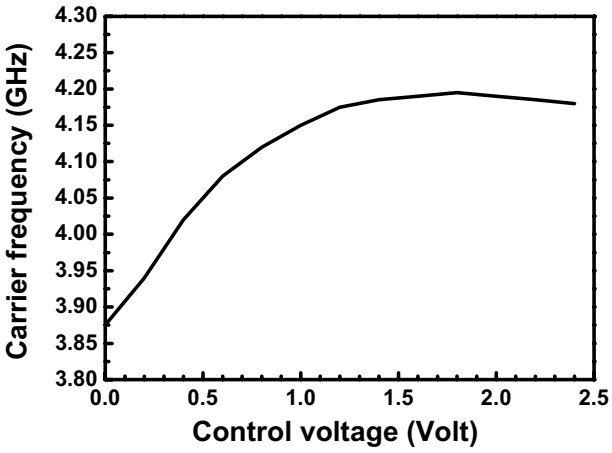

Fig. 6 The measured tuning range of the 4-GHz CMOS LC VCO.

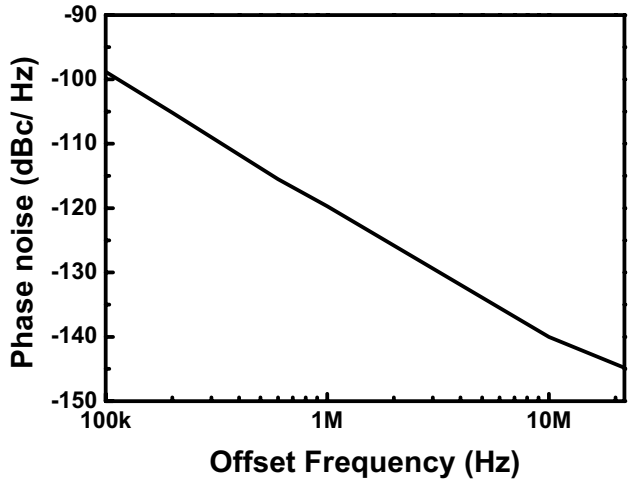

Fig. 7 The measured phase noise of the 4-GHz CMOS LC VCO.

Table I A Summary of the presented and the previously reported state-of-the-art 4 to 6 GHz CMOS LC VCO.

	P_{DC} (mW)	Carrier frequency (GHz)	Phase noise at 1MHz (dBc/Hz)	FOM (dBc/Hz)
This work 0.25 μm CMOS	7	4.2 GHz	-119.94	-183.9
[9] 0.25 μm CMOS	7.5	4 GHz	-117	-180.3
[12] 0.18 μm CMOS	5.9	5.6 GHz	-116.7	-184