Roughness-Enhanced Reliability of MOS Tunneling Diodes

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***Abstract*—Both electrical and optical reliabilities of PMOS and NMOS tunneling diodes are enhanced by oxide roughness, prepared by very high vacuum prebake technology. For the rough PMOS devices, as compared to the flat PMOS devices, the Weibull plot of T_{BD} shows 2.5-fold enhancement at 63% failure rate, while both the D_2 and H_2-treated flat PMOS devices show similar inferior reliability. For the rough NMOS devices, as compared to the flat NMOS devices, the Weibull plot of T_{BD} shows 4.9-fold enhancement at 63% failure rate. The time evolutions of the light emission from the rough PMOS and NMOS diodes degrade much less than those of the flat PMOS and NMOS diodes. The momentum reduction perpendicular to the Si/SiO_2 interface by roughness scattering could possibly make it difficult to form defects in the bulk oxide and at the Si/SiO_2 interface by the impact of the energetic electrons and holes.**

***Index Terms*—Electroluminescence, MOS, reliability, roughness, ultrathin oxide.**

I. Introduction

THE SILICON dioxide in MOSFETs plays a major role in the electrical properties of such devices. As the oxide thickness continues to scale down, the roughness of the gate oxide is no longer negligible. Several groups have reported the effects of interface roughness on the electrical performance. The interface roughness degraded MOSFET channel mobility due to the surface scattering [1], [2], degraded the time-dependent dielectric breakdown (TDDB) characteristics of MOS capacitors, and increased the tunneling current through the oxide [3]. On the other hand, the advantage of oxide roughness has also been utilized to enhance the electroluminescence efficiency in the MOS tunneling diodes [4], but the oxide roughness has not been reportedly beneficial to the electrical properties of MOS devices. The deuterium enhanced oxide reliability has been investigated by many groups for years [5]–[7], but no isotope effect has been observed in the deuterium-treated MOS devices stressed in the hole injection condition [8]–[10]. The tunneling-hole-induced traps in bulk oxide are responsible for this soft breakdown, and oxide degrades even with the deuterium passivation [10], [11]. Therefore, it is of great importance and interest to improve the reliability of ultrathin gate oxide in a hole-stressed device. In this letter, we investigate the oxide roughness effect on the reliability of PMOS tunneling diodes and demonstrate that the rough oxide can enhance both the electrical and optical reliability of PMOS tunneling diodes. The same results are also observed in the NMOS tunneling diodes.

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II. Growth and Device Fabrication

The ultrathin gate oxide was grown by rapid thermal oxidation (RTO) on 1–10 Ω-cm n/p-type silicon wafer at the 850 °C. The gas flows were 500 sccm nitrogen and 500 sccm oxygen at a reduced pressure. After a HF dip, the wafers were *in-situ* baked in the very high vacuum condition ($<3\times10^{-6}$ torr, maintained by a turbo pump) at 1000 °C to obtain the rough Si surface [12], and then the wafers were baked in hydrogen at 1000 °C for 1 min before the rapid thermal oxidation. Note that this very high vacuum prebake should also yield a clean silicon surface [13]. After the growth of ultrathin oxide, the sample was *in situ* annealed in nitrogen for 10 min at 900 °C. The oxide thickness was measured by ellipsometry. Due to the roughness on the oxide surface and at oxide/Si interface, the thickness of rough oxide cannot be well defined if there is small deviation from conformal growth model. The electrical thickness by tunneling current or capacitance–voltage (C–V) method cannot be measured accurately due to the large effective area on the rough oxide, and the two-dimensional (2-D) electrical effect in the rough oxide [14], which is unknown. The meaningful thickness of rough oxide itself is an issue to be further investigated. Here, we simply use the thickness measured from ellipsometry as a reference. The roughness was measured by atomic force microscope (AFM) and X-ray reflectivity. The interface roughness was measured by AFM right after HF dip to remove the oxide. The roughness magnitude of the oxide surface is very similar to that of the oxide/silicon interface. This confirms the conformal growth of the oxide [15]. The MOS tunneling diodes were evaporated with Al gate electrodes with different circular areas defined by photolithography.

III. Results and Discussion

Fig. 1 shows the time evolutions of gate tunneling current for the flat and the rough PMOS tunneling diodes with the oxide thickness of 2.7 nm and 2.8 nm, respectively, under constant voltage stress (CVS) at gate voltage (V_g) of 2 V. The area size of the devices is 3×10^{-4} cm^2. As oxide scaling down, the mechanism of oxide degradation is dominated by the soft breakdown,

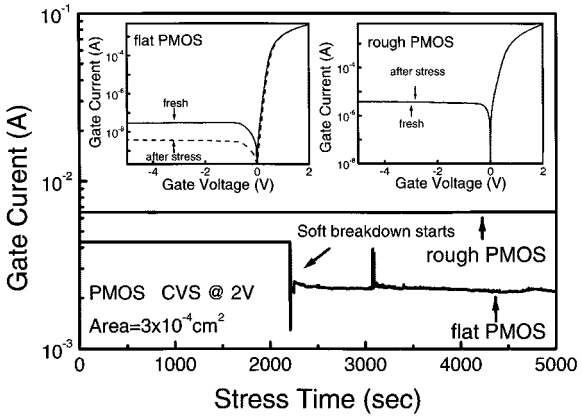

Fig. 1. Time evolutions of gate current of the flat and the rough PMOS tunneling diodes under 2 V constant voltage stress. The insets are I–V curves before and after stress (left: the flat device, right: the rough device).

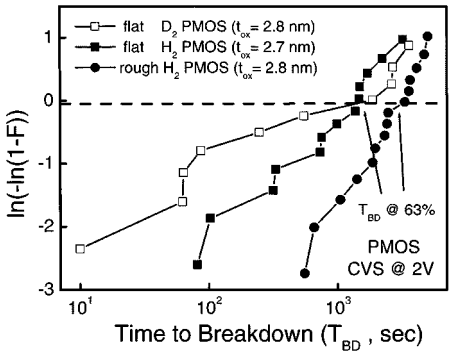

Fig. 2. Weibull plot of the T_{BD} characteristics for the flat (H_2, D_2) and the rough (H_2) PMOS tunneling diodes under CVS at $V_g = 2$ V.

which is characterized by the increase of the gate noise [16]. In our case, the breakdown criterion is that the gate current fluctuation (spike) occurs during the CVS as indicated in Fig. 1. The flat PMOS device with the oxide roughness of 0.15 nm reveals degradation after ~2200 s stress, while the rough PMOS devices with the oxide roughness of 1.46 nm shows very little gate current fluctuation under the same stress condition. Note that the rough device has larger injection current density than the flat device probably due to the 2-D electrical effect and the large effective area at Si/SiO_2 interface. Similar results have been observed in [3]. The current–voltage (I–V) characteristics before and after stress are shown in the insets of Fig. 1. The gate current of the flat PMOS device shows a large disparity between the fresh device and the stressed device (left inset). The gate tunneling current in the rough PMOS device remains almost the same after stress (right inset). This indicates that the rough PMOS device has better oxide reliability than the flat PMOS devices.

Fig. 2 shows the Weibull plot of the time to breakdown (T_{BD}) characteristics for both the flat (H_2 and D_2-treated) and the rough (H_2-treated) PMOS tunneling diodes under CVS at $V_g = 2$ V. For the rough H_2-treated device, as compared to the flat H_2-treated device, the Weibull plot of T_{BD} shows 2.5-fold enhancement at 63% failure rate, while both the flat D_2 and H_2-treated PMOS devices show similar inferior reliability. The Weibull plot of charge to breakdown (Q_{BD}) also shows

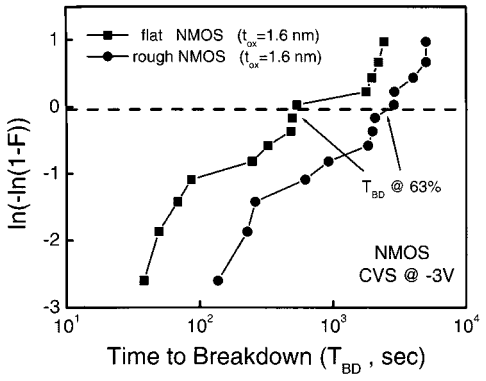

Fig. 3. Weibull plot of the T_{BD} characteristics for the flat (H_2) and the rough (H_2) NMOS tunneling diodes under CVS at $V_g = -3$ V.

5.7-fold enhancement at 63% failure rate (not shown here). It is shown that deuterium cannot improve the oxide degradation of the PMOS devices under the hole injection stress [10]. Two kinds of current components exist in the PMOS tunneling diodes. The electron current tunnels from Si conduction band to Al and the hole current tunnels from Al to Si valence band. The hole tunneling from Al to Si can be trapped in the oxide directly and/or break the Si–H bonds at Si/SiO_2 interface. Even in the direct tunneling, the tunneling hole can still have excessive energy with respect to the valance band edge. This energy can break the Si–H(D) bonds [8]. The electron tunneling from Si to Al cannot damage the Si/SiO_2 interface, since there is no excess electron energy at the Si/SiO_2 interface. In the PMOS devices with rough oxide, the injected holes are scattered by the rough Si/SiO_2 and Al/SiO_2 interfaces, and thus the hole momentum perpendicular to the interface is reduced. The perpendicular hole momentum seems crucial for the direct hole trapping in the oxide and the breakage of Si–H bonds at Si/SiO_2 interface. The reduction of this momentum prevents the defect formation in the bulk oxide and at the Si/SiO_2 interface, and leads to enhanced reliability in the rough devices. The rough oxide may be an alternative to improve the oxide reliability during the hole injection. Fig. 3 shows the Weibull plot of T_{BD} characteristics for both the H_2-treated flat and rough NMOS tunneling diodes with the same oxide thickness of 1.6 nm, under CVS at $V_g = -3$ V. For the rough device, as compared to the flat device, the Weibull plots of T_{BD} and Q_{BD} (Q_{BD} plot not shown here) shows 4.9 and 2.9-fold enhancement, respectively, at 63% failure rate. The rough NMOS tunneling diodes also reveal improved electrical reliability than the flat NMOS tunneling diodes. Previous works on the voltage acceleration characteristics were based on uniform electric field across the oxide. However, for the rough oxide, the electric field in the oxide is 2-D, and not uniform in the oxide. The maximum electric field in the rough oxide can be larger than that in the flat oxide even at lower gate voltage [14]. The voltage acceleration factor is complicated and still under investigation.

To further investigate the roughness effect on the oxide reliability, the light emission intensity at bandgap energy is measured. The detailed mechanism can be found in [17]. The time evolutions of emission intensity from the flat and the rough PMOS diodes are shown in Fig. 4. The operation gate current is 100 mA and the device area is 1.5×10^{-2} cm^2. The intensity of

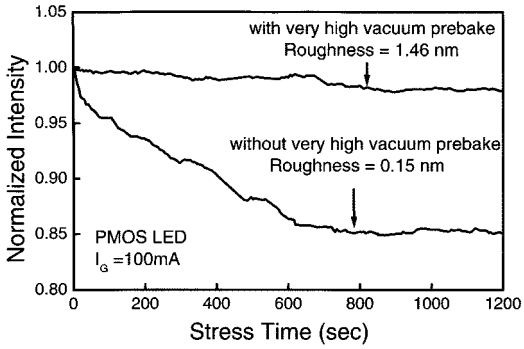

Fig. 4. Time evolutions of light emission intensity from the flat and the rough PMOS diodes. The rough PMOS diode shows much less emission intensity degradation than the flat PMOS device.

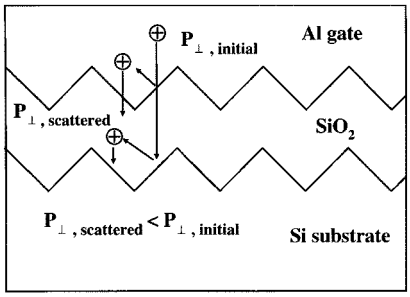

Fig. 5. Illustration of the speculative mechanism of the roughness-enhanced reliability. The hole impact energy perpendicular to the Si/SiO_2 and Al/SiO_2 interface is reduced due to the surface and interface roughness scattering. The multiple scattering of the tunneling hole are possible in this process.

the rough devices shows very slight variation during the stress time, while that of the flat devices degrades about 15% after 1200 s stress. The degradation of bandgap light emission indicates the formation of interface states, which act as nonradiative recombination centers. The interface states may be induced due to the breakage of the Si–H bonds by injected holes. The stress of hole current generates more interface states in the flat oxide than in the rough oxide. The rough oxide is more robust to tunneling carrier stress than the flat oxide, since the momentum (energy) of the injected hole tunneling from Al gate is scattered by the oxide roughness, and this lowers the injected hole momentum perpendicular to the interface to bombard the Si/oxide interface. The light emission of NMOS diodes showed similar results.

Fig. 5 shows the speculative mechanism of the roughness-enhanced oxide reliability in PMOS tunneling diodes. When the carriers tunnel through the oxide, they are scattered by the oxide roughness and the momentum of the injected holes perpendicular to the interface is reduced. In the PMOS tunneling diodes, the oxide degradation is related to the tunneling-hole-induced traps in bulk oxide [10], [11], and the threshold energy for the injected holes to be captured by O Vacancy is 1.8 eV [18]. This indicates that only the hole with injected energy higher than 1.8 eV can be trapped in the oxide and can induce oxide degradation. Since the reliability of the MOS tunneling diode is related to the energy of the injected holes, the perpendicular energy reduction of the holes tunneling through the oxide could improve the electrical and optical reliability of the devices. However, it is an intuitive model, and more evidence is needed to give a clear picture of the phenomenon.

IV. Conclusion

The ultrathin oxide reliability is enhanced by introducing oxide roughness. The very high vacuum prebake is demonstrated to be an effective method to produce such oxide roughness. The rough oxide can be a novel technology to improve both the electrical and optical reliability of MOS devices.

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