A High-Precision Time-to-Digital Converter Using a Two-Level Conversion Scheme

Chorng-Sii Hwang, *Student Member, IEEE*, Poki Chen, and Hen-Wai Tsao, *Member, IEEE*

***Abstract*—This paper describes a design of time-to-digital converter (TDC) using a two-level conversion scheme. The first level is accomplished by a multi-phase sampling technique with the aid of delay-locked loop (DLL). Then the input signal and its adjacent sampling clock are manipulated and sent into a vernier delay line (VDL) sampling circuit at the second level. The proposed TDC can provide high resolution with less hardware compared to one level VDL sampling circuit with the same dynamic range. A new architecture of dual DLL circuit is also implemented to stabilize delay control against process and ambient variations. A test chip is designed and fabricated in 0.35-μm logic technology. With an input reference clock within 130 to 160 MHz, the TDC achieves 24 to 30 ps resolution. The DNL is less than $\pm$0.55 LSB and INL is within $+1$ to -1.5 LSB.**

***Index Terms*—Delay-locked loop, time-to-digital converter (TDC), Vernier delay line.**

I. Introduction

TIME-TO-DIGITAL converter (TDC) has been widely used in many applications such as particle life time detection in high energy physics [1]–[3], equivalent-time sampling in oscilloscope [4], laser range finder [5], time-interval analyzer, frequency counter, and on-chip jitter measurement. Due to the rapid development in VLSI technology, most of the TDCs are integrated into the target systems so as to reduce the cost and power while achieving high resolutions.

Traditional analog approaches such as dual slope and time-to-amplitude methods are slow and vulnerable to system noise. New digital approaches using DLL have been widely adopted because DLL can provide accurate multi-phase sampling clocks and has the merit of lower power. However, there is a limitation on the minimum resolution due to the intrinsic gate delay of the unit delay buffer in DLL. Several techniques based on gate delay difference can improve the resolution up to sub-gate delay. The DLL array [2], multi-level [5] and vernier delay line (VDL) [3] methods have been presented. The VDL method provides excellent resolution but suffers from large chip area if a wide dynamic range is required. Here we propose a two-level conversion scheme combining the multi-phase sampling and VDL sampling methods to alleviate the burden of large number of delay stages in VDL method for a given dynamic range.

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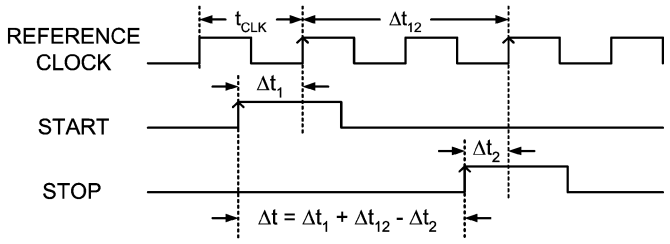

Fig. 1. Timing diagram of conversion.

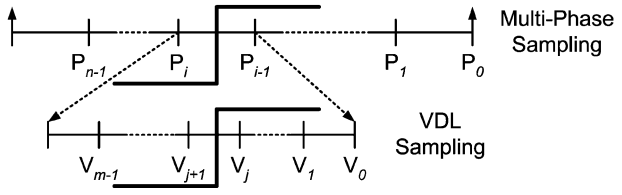

Fig. 2. Two-level conversion scheme.

II. Principle of Operation

Many TDC systems accept two asynchronous START/STOP input signals and measure their time difference. The timing diagram of a typical TDC is depicted in Fig. 1. The timing acquisition process consists of three phases. First, the time interval (Δt_1) between the rising edges of the START signal and the succeeding reference clock is measured. Secondly, a coarse counter is activated to measure the time interval (Δt_{12}) between the two rising edges of the reference clock immediately following the START and the STOP signals. Finally, the same procedure for measuring the time interval (Δt_2) between the rising edges of the STOP signal and the succeeding reference clock is also performed. The time interval between the START and STOP signals, Δt, may be determined as $(\Delta t_1 + \Delta t_{12} - \Delta t_2)$. The dynamic range for fine conversion of Δt_1 and Δt_2 is limited to only one reference clock cycle $(t_{\rm CLK})$. Since the coarse result is derived from the counter, the overall dynamic range of the time interval measurement may be extended by increasing the number of bits of the counter. The key design issue here is the fine measurement of the time intervals, Δt_1 and Δt_2.

The fine time conversion process in our proposed TDC is further interpolated into two levels as shown in Fig. 2. At the first level, the time interval between the rising edge of the input signal and the next rising edge of the clock is digitized by a multi-phase time sampler using n-stage equal-phase sampling clocks. Hence the resolution of the first level is $t_{\rm CLK}/n$. Then, the input signal and its adjacent sampling clock are fed into an

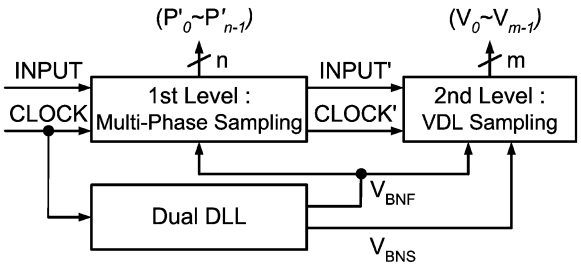

Fig. 3. TDC architecture.

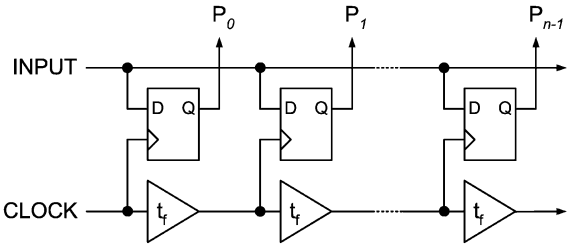

Fig. 4. Multi-phase sampler.

m-stage VDL time sampler. The resolution of the first level conversion is equal to the dynamic range of the second level conversion. The overall resolution of the two-level conversion can be as fine as $t_{\rm CLK}/(m*n)$. The dynamic range of the VDL time sampler used in the second level can be restricted to only a fraction of the whole reference clock cycle, which is equal to $t_{\rm CLK}/n$.

III. Circuit Description

The architecture of the proposed TDC for fine time digitization is shown in Fig. 3. Each block is fully described in the following sub-sections.

A. Multi-Phase Sampling

Conventionally, the multi-phase sampler consists of a tapped delay line and a set of D-flip/flops (DFF). To resolve the timing relationship between input signal and clock, we may apply the input or clock signals into the tapped delay lines. Delaying clock technique as shown in Fig. 4 is chosen to accomplish the equal-phase sampling function because it is more suitable to generate the necessary timing information between the input and its adjacent sampling clock. The delay of the tapped delay buffer is set to be t_f, which is stabilized by the dual DLL described in a later sub-section. Two starving-current inverters with NMOS-control [3] constitute the tapped delay buffer.

The difficulty in designing the two-level conversion scheme lies in selecting the sampling clock adjacent to the input signal. Decision must be made before sending the corresponding sampling clock into the second level circuitry. The easiest solution is to employ the information derived from the sampling results of the DFFs $(P_0 \sim P_{n-1})$.

In the ideal condition, these sampling results $(P_0 \sim P_{n-1})$ should rise from low to high sequentially in the interval of t_f because the sampling clocks are generated via tapped delay buffers. However, the DFFs used in the multi-phase sampler may suffer from the setup time violation. If the input signal is very close to any one of the sampling clocks, the resolving time of DFFs will become longer. This meta-stable behavior of DFFs will vary the time relationship of the input versus sampling results, especially the first one that becomes high.

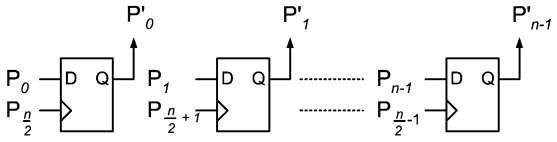

Fig. 5. Re-aligning circuit in the first level.

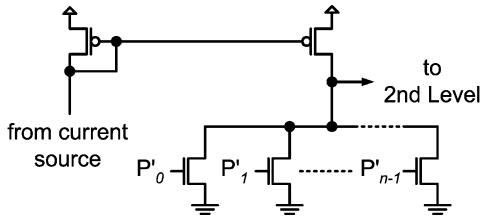

Fig. 6. Dynamic NOR.

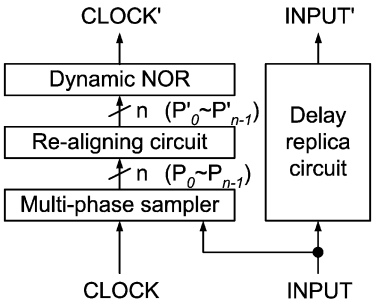

Fig. 7. Modified multi-phase sampling circuitry.

A solution to this undesirable problem is to introduce the re-aligning circuit by cascading an extra stage of DFFs after the outputs of the multi-phase sampler as shown in Fig. 5. Each of the sampling results (P_i) from the first level is re-aligned by another sampling result $(P_{n/2+i})$ to avoid the meta-stability by waiting half a cycle. In this proposed architecture, only half $(n/2)$ of the new sampling results $(P'_i \sim P'_{n/2+i-1})$ will be set to high. This will also be easier to read out the converted values from the first level. The penalty accompanied by the re-aligning circuit is the increased layout area and routing complexity when connecting the original outputs of multi-phase sampler into DFFs with equal loading.

The re-aligned outputs $(P'_0 \sim P'_{n-1})$ can then be sent into a dynamic NOR gate to extract the adjacent sampling clock information as shown in Fig. 6. A voltage bias is generated by a PMOS replica via a programmable current source.

The modified multi-phase sampling circuitry in the first level conversion is drawn in details in Fig. 7. Due to the extra circuitry described above, we must also add a delay replica circuit for the input signal to compensate for the increased delay in the clock path. The total delay in the first level conversion induced by the multi-phase sampler, re-aligning circuit and dynamic NOR gate can be estimated using the following formula

$$t_{\rm 1st} = t_{\rm DFF(multi\text{-}phase)} + 0.5{*}t_{\rm CLK} + t_{\rm DFF(re\text{-}aligning)} + t_{\rm DNOR}. \quad (1)$$

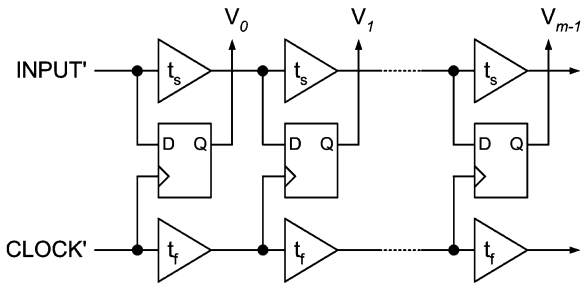

Fig. 8. VDL sampler.

The re-aligning circuit will increase the delay by

$$t_{(\text{re-aligning})} = 0.5{*}t_{\text{CLK}} + t_{\text{DFF(re-aligning)}}. \tag{2}$$

The delay through the delay replica circuit needs to match the total delay, $t_{1\text{st}}$, exactly considering all parasitic effects from the actual layout. A trimmed-down copy of the clock path circuit was used to create the delay replica circuit for the input signals in order to mimic the delay of the clock path.

B. VDL Sampling

The major part of the second level conversion is the VDL sampler, which is composed of two tapped delay lines with different delay and a set of DFFs as shown in Fig. 8. The resolution of the VDL sampler is given by

$$\Delta t_r = t_s - t_f, \quad \text{where } t_s > t_f. \tag{3}$$

For simplicity of implementation, we use the same circuitry for delay buffers in both fast and slow delay lines. The delay of the fast line is also identical to the delay buffer in the multi-phase sampler. The voltage biases of both tapped delay lines are provided by the dual DLL.

The conversion process in the second level should be done after the clock signal (CLOCK') goes across the last tapped delay buffer to trigger the DFF. The conversion time is estimated to be

$$t_{2\text{nd}} = m{*}t_f + t_{\text{DFF(VDL)}}. \tag{4}$$

C. Dual DLL

In order to control the delay of the tapped delay lines in the multi-phase sampler and the VDL sampler, a dual DLL architecture is proposed as shown in Fig. 9. The dual DLL consists of a "fast" DLL and a "slow" one. Each DLL contains a tapped delay line, a phase detector, a charge pump, and a loop filter, which usually is a capacitor. The phase detector accepts the reference clock and the last stage output of the tapped delay line. If the reference clock leads, the phase detector will generate UP/DOWN signals to control the charge pump to decrease delay of the delay line until the reference clock and the last stage output are in phase.

The "fast" DLL in Fig. 9 contains n-stage delay buffers and regulates their delay to be $t_f (= t_{\text{CLK}}/n)$. The output of the

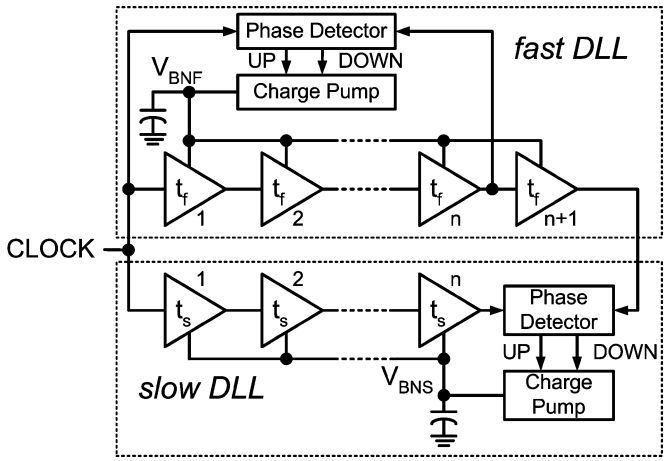

Fig. 9. Dual DLL.

$(n+1)$th delay buffer from the "fast" DLL is chosen to match the output of the nth delay buffer in the "slow" DLL. It forces the delay of the delay buffers in the "slow" DLL to become

$$n{*}t_{\text{s}} = (n+1){*}t_f \tag{5}$$

$$t_{\text{s}} = (t_{\text{CLK}}/n){*}(n+1)/n = t_{\text{CLK}}{*}(n+1)/n^2. \tag{6}$$

Then both of the bias voltages V_{BNF} and V_{BNS} are sent into the multi-phase and VDL samplers. The resolution, Δt_r, of the VDL sampler in the second level conversion can be obtained by the delay difference of the two gates in (3)

$$\Delta t_r = [t_{\text{CLK}}{*}(n+1)/n^2] - [t_{\text{CLK}}/n] = t_{\text{CLK}}/n^2. \tag{7}$$

Thus, the delay stage number in VDL sampler is the same as the number of the multi-phase sampler, i.e., m is equal to n. The main advantage of such a dual DLL is that it needs only a single reference clock instead of two phase-delayed reference clocks in a previous work [3].

D. Conversion Time Analysis

From (1) and (4), the total conversion time, t_{total}, can be estimated to be (m is equal to n)

$$\begin{aligned} t_{\text{total}} &= t_{1\text{st}} + t_{2\text{nd}} \\ &= (t_{\text{DFF(multi-phase)}} \\ &\quad + 0.5{*}t_{\text{CLK}} + t_{\text{DFF(re-aligning)}} + t_{\text{DNOR}}) \\ &\quad + (m{*}t_f + t_{\text{DFF(VDL)}}) \\ &= 1.5{*}t_{\text{CLK}} + t_{\text{DFF(multi-phase)}} + t_{\text{DFF(re-aligning)}} \\ &\quad + t_{\text{DFF(VDL)}} + t_{\text{DNOR}}. \end{aligned} \tag{8}$$

Assuming the delay of dynamic NOR is small compared to the clock cycle, t_{DNOR} can be omitted from (8). Then, we replace the delay of DFFs to be the maximum value among the three circuits with $t_{\text{DFF(max)}}$, the total time becomes

$$\begin{aligned} t_{\text{total}} &= 1.5{*}t_{\text{CLK}} + 3{*}t_{\text{DFF(max)}} \\ &= 3{*}(0.5{*}t_{\text{CLK}} + t_{\text{DFF(max)}}). \end{aligned} \tag{9}$$

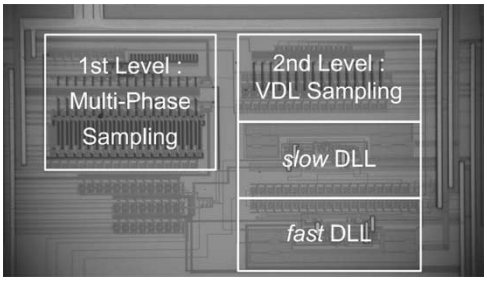

Fig. 10. Chip micrography.

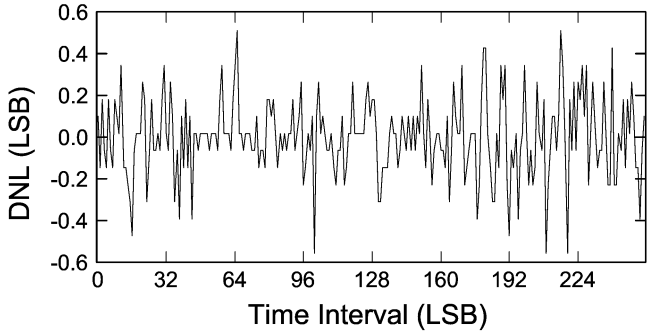

Fig. 11. Differential Nonlinearity.

For (2), we also replace $t_{\mathrm{DFF(re\text{-}aligning)}}$ to be $t_{\mathrm{DFF(max)}}$

$$t_{\mathrm{(re\text{-}aligning)}} = 0.5{*}t_{\mathrm{CLK}} + t_{\mathrm{DFF(max)}}. \tag{10}$$

From (9) and (10), the re-aligning circuit will increase 50% of the total conversion time of the system without the re-aligning circuit.

The conversion time represented in terms of clock cycle number will be dependent on the relationship between t_{CLK} and $t_{\mathrm{DFF(max)}}$. In our design, we choose t_{total} to be no greater than three clock cycles.

IV. Implementation and Measurement

A test chip of the proposed TDC was designed and fabricated in TSMC 0.35-μm SPQM Silicide logic process. The TDC uses 16 stages of delay buffers in both levels and provides 256 LSBs in one reference clock cycle. The micrograph of the test chip is shown in Fig. 10. The core area of this two-level TDC is 1000 μm $\times$ 600 μm. HP 81200 Data/Pulse Generator with 2 ps delay step is used to characterize the test chip. The TDC can operate at the clock rate within 130 to 160 MHz corresponding to one LSB of 24 to 30 ps. Due to the nonlinear characteristic of the delay buffer, the DLL will operate at its low delay gain so as to avoid the large loop jitter to affect the conversion accuracy. The differential nonlinearity (DNL) is less than $\pm$0.55 LSB and integral nonlinearity (INL) is within $+1$ to -1.5 LSB as shown in Figs. 11 and 12, respectively. The overall performance is summarized in Table I. The worst case of DNL and INL are mainly caused by the mismatch of layout paths in the multi-phase sampler and the crosstalk of input signals.

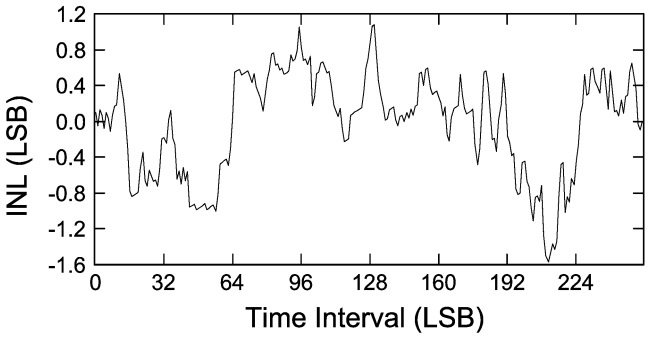

Fig. 12. Integral Nonlinearity.

TABLE I
Performance Summary

Operating Voltage	3.0 to 3.6V
Temperature	0^{o} to $+60^{o}$C
Clock Frequency	130 to 160MHz
Delay Stage (n)	16
Bin Size (n^2)	256
LSB (t_{CLK}/n^2)	24 to 30ps
Power	< 50mW

V. Conclusion

In this paper, a high-precision TDC using a two-level conversion scheme was proposed and fabricated in 0.35-μm logic technology. By employing the technique of multi-phase sampling at the first level, the stage number of the second-level VDL sampler can be reduced. A dual DLL providing delay regulation based on a single reference clock input is also presented. The test chip achieves 24 to 30 ps resolution with DNL less than $\pm$0.55 LSB and INL is within $+1$ to -1.5 LSB.

Acknowledgment

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