A Low-Phase-Noise K-Band CMOS VCO

Hsieh-Hung Hsieh, *Student Member, IEEE*, and Liang-Hung Lu, *Member, IEEE*

***Abstract*—A novel circuit topology for low-phase-noise voltage controlled oscillators (VCOs) is presented in this letter. By employing a PMOS cross-coupled pair with a capacitive feedback, superior circuit performance can be achieved especially at higher frequencies. Based on the proposed architecture, a prototype VCO implemented in a 0.18-μm CMOS process is demonstrated for K-band applications. From the measurement results, the VCO exhibits a 510-MHz frequency tuning range at 20 GHz. The output power and the phase noise at 1-MHz offset are −3 dBm and −111 dBc/Hz, respectively. The fabricated circuit consumes a dc power of 32 mW from a 1.8-V supply voltage.**

***Index Terms*—Capacitive feedback, CMOS radio frequency (RF), differential colpitts oscillators, K-band, LC-tank, low phase noise, voltage-controlled oscillators (VCOs).**

I. Introduction

VOLTAGE-CONTROLLED oscillators (VCOs) are one of the key building blocks in optical-fiber and wireless communication systems. In consideration of the implementation cost and system integration, VCOs fabricated in a standard CMOS process have attracted great attention in recent years. As the transistor feature size migrates into deep-submicron regime, fully integrated CMOS VCOs operating at millimeter-wave frequencies have been demonstrated [1]–[3]. However, due to the lack of high-Q on-chip passive components and the inherently high flicker noise of the MOSFETs, most of the VCO circuits suffer from inferior phase noise and reduced output swing especially at the high-frequency bands.

To overcome the performance limitations imposed on high-frequency CMOS VCOs, circuit techniques were reported by using transformers [4], coplanar striplines [5], and micromachined inductors [6]. In this letter, a novel circuit technique is proposed for the CMOS VCO designs. By employing a capacitive feedback in the cross-coupled VCO topology, a significant improvement in phase noise and output swing can be achieved while maintaining a compact chip layout. Using a 0.18-μm CMOS process, the VCO is designed and implemented at the 20-GHz frequency band for demonstration.

The design and analysis of the proposed VCO topology are presented in Section II. Experimental results are shown in Section III. Finally, the conclusion follows in Section IV.

Manuscript received January 9, 2006; revised March 31, 2006. This work was supported in part by the National Chip Implementation Center (CIC) and by the National Science Council of Taiwan, R.O.C., under Grants 94-2220-E-002-026 and 94-2220-E-002-009.

The authors are with the Graduate Institute of Electronics Engineering, Department of Electrical Engineering, National Taiwan University, Taipei 10617, Taiwan, R.O.C. (e-mail: lhlu@cc.ee.ntu.edu.tw).

Digital Object Identifier 10.1109/LMWC.2006.882386

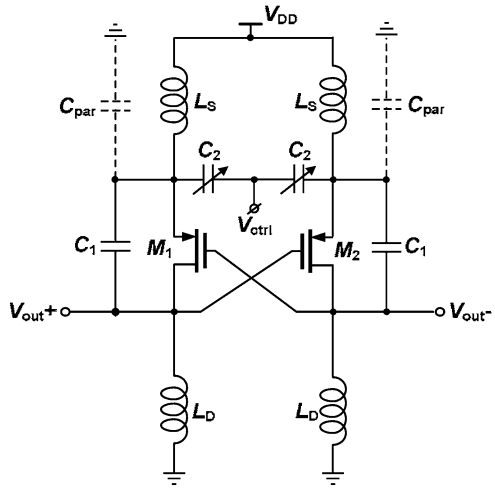

Fig. 1. Circuit schematic of the proposed K-band VCO.

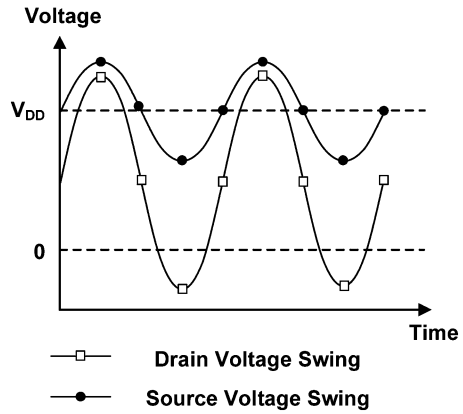

Fig. 2. Enhanced voltage swing due to the capacitive feedback.

II. Circuit Design and Analysis

The circuit schematic of the proposed VCO is shown in Fig. 1. Since the PMOS transistor exhibits a flicker noise approximately one decade lower than its NMOS counterpart [7], [8], a PMOS cross-coupled pair is employed in this design. To eliminate the additional flicker noise contribution, the tail-current transistor in a conventional VCO topology is replaced by a LC-resonator (L_S and $C_{\rm par}$) to provide the required dc bias while exhibiting high impedance in the vicinity of the oscillation frequency. In the proposed VCO, a capacitive feedback which is composed of capacitors C_1 and C_2 is employed. Due to the use of on-chip inductors and the in-phase relationship established by the capacitive feedback, the drain and source voltage can swing above the supply voltage and below the ground potential as illustrated in Fig. 2. Consequently, the output swing of the VCO is enhanced, leading to an improved close-in phase noise.

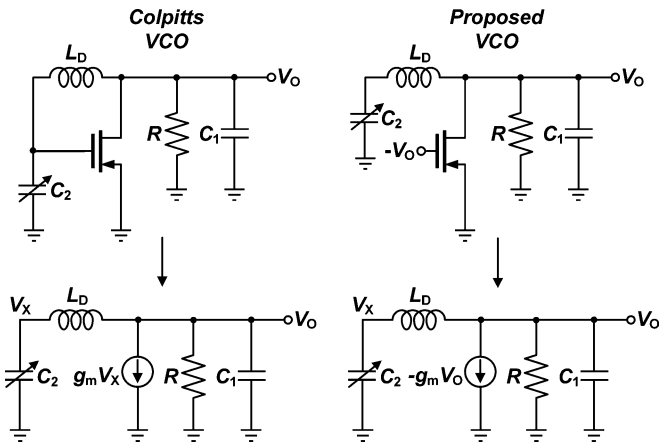

Fig. 3. Half circuits of the Colpitts and the proposed VCO.

With the differential operation of the VCO at oscillation, the half-circuit technique is employed to simplify the analysis. Fig. 3 shows the small-signal equivalent circuit of the VCO, where g_m is the transconductance of the cross-coupled pair and R represents the finite output resistance of the transistor and the losses from the LC-tank. To satisfy the Barkhausen criterion for a sustained oscillation, the oscillating frequency and the unity loop gain condition are given as

$$\omega_0 = \sqrt{(C_1 + C_2)/C_1 C_2 L_D} \tag{1}$$

$$g_m = \frac{1}{R}. \tag{2}$$

From the circuit schematic and the oscillation frequency as indicated in (1), it is observed that the capacitive feedback provided by the proposed VCO topology is similar to a Colpitts oscillator. Hence, it also benefits from the cyclo-stationary noise effect [9] in terms of the phase noise performance. However, due to the use of the cross-coupled pair, the unity loop gain condition is relaxed from the Colpitts oscillator which is expressed as

$$g_m = \frac{C_2}{C_1} \cdot \frac{1}{R}. \tag{3}$$

Note that the required transconductance in (2) is independent of the capacitance ratio C_2/C_1. A large value of C_2/C_1 can be used to boost the output swing for phase noise suppression without increasing the required transconductance to sustain the oscillation. Therefore, it provides an efficient mechanism to trade the frequency tuning range for phase noise, especially for high-frequency VCO designs.

III. Experimental Results

The proposed VCO is designed and implemented in a 1P6M 0.18-μm CMOS process where a top interconnect metal with a thickness of 2 μm is provided. In consideration of the loaded quality factor and the layout symmetry, center-tapped inductors are employed. Based on full-wave electromagnetic (EM) simulation, the inductors have a Q-factor of 15 in the vicinity of 20 GHz. Fig. 4 shows the microphotograph of the fabricated

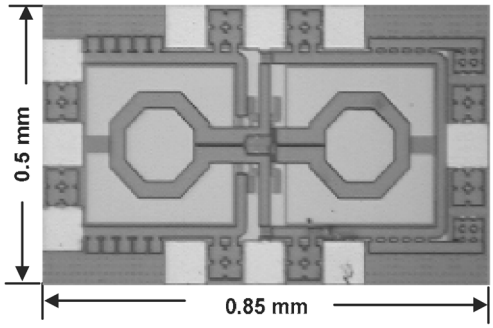

Fig. 4. Die photograph of the fabricated K-band CMOS VCO.

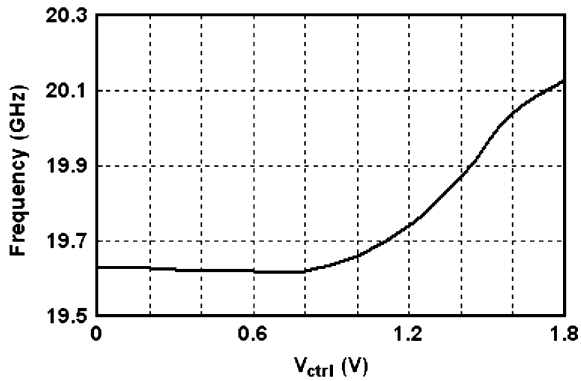

Fig. 5. Frequency tuning characteristics of the VCO.

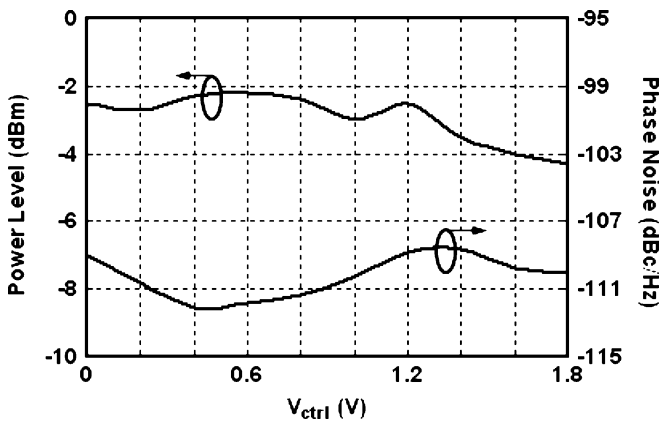

Fig. 6. Output power level and phase noise of the VCO.

VCO with chip area of 0.85×0.5 mm^2 including the pad frame. Using an Agilent E4407B spectrum analyzer, the performance of the VCO was characterized by on-wafer probing.

Operating at a supply voltage of 1.8 V, the VCO consumes a dc power of 32 mW. As the controlled voltage sweeps from 0 to 1.8 V, the oscillation frequency varies from 19.62 to 20.13 GHz as shown in Fig. 5, indicating a tuning range of 510 MHz and an average VCO gain of 283 MHz/V. The measured output power and phase noise at 1-MHz offset versus the controlled voltage are shown in Fig. 6. Within the VCO tuning range, the variations in output power and phase noise are less than ± 1 dB and ± 2 dB, respectively. Fig. 7 shows the close-in output spectrum of the VCO operating at a controlled voltage of 0.9 V. Due to

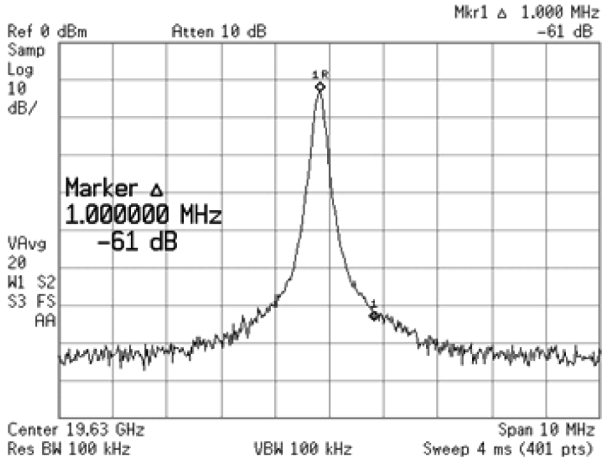

Fig. 7. Close-in output spectrum of the VCO at $V_{\rm ctrl} = 0.9$ V.

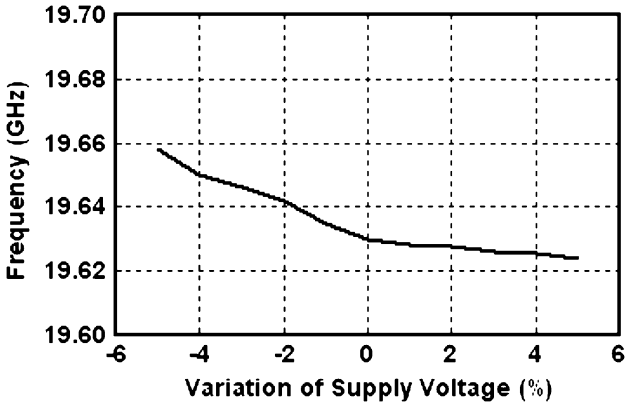

Fig. 8. VCO performance with respect to the supply variation.

the absence of the tail-current, the bias stability and its impact on the circuit performance are evaluated. Provided a $\pm 5\%$ variation in the supply voltage, the measured oscillation frequency is illustrated in Fig. 8. Only insignificant performance variation is observed from the measurement results. Table I summarizes the circuit performance of the proposed VCO.

IV. Conclusion

By employing a capacitive feedback in the cross-coupled pair, a novel VCO topology is presented to improve the phase noise and output swing. Based on the proposed topology, a 20-GHz VCO is implemented in a 0.18-μm CMOS process. It demonstrates the potential of implementing fully-integrated high-performance CMOS VCOs at millimeter-wave frequencies.

TABLE I
Performance Summary

		Unit	Performance
Technology		—	0.18-μm CMOS
Central Frequency		GHz	19.9
Tuning Range		MHz	510
V_{DD}		V	1.8
DC Power	Core	mW	32
	Buffer		7
Output Power Level		dBm	-3
Phase Noise@1-MHz offset		dBc/Hz	-111
FOM*		dBc/Hz	-182

* $\text{FOM} = 10\log_{10}[(\frac{f_o}{\Delta f})^2 \cdot \frac{1}{L\{\Delta f\} \cdot P_{dc}}]$.

References

[1] H. Shigematsu, T. Hirose, F. Brewer, and M. Rodwell, "CMOS circuit design for millimeter-wave applications," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Jun. 2004, pp. 123–126.

[2] C. Cao and K. K. O , "A 90-GHz voltage-controlled oscillator with a 2.2-GHz tuning range in a 130-nm CMOS technology," in *IEEE VLSI Dig.*, Jun. 2005, pp. 242–243.

[3] M. Tiebout, H.-D. Wohlmuth, and W. Simburger, "A 1 V 51 GHz fully-integrated VCO in 0.12 μm CMOS," in *ISSCC Dig.*, Feb. 2002, vol. 1, pp. 300–301.

[4] N.-J. Oh and S.-G. Lee, "11-GHz CMOS differential VCO with back-gate transformer feedback," *IEEE Microw. Wireless Compon. Lett.*, vol. 15, no. 11, pp. 733–735, Nov. 2005.

[5] H. Krishnaswamy and H. Hashemi, "A 26 GHz coplanar stripline-based current sharing CMOS oscillator," in *Proc. IEEE RFIC Symp.*, Jun. 2005, pp. 127–130.

[6] T.-P. Wang *et al.*, "A 22-GHz push-push CMOS oscillator using micromachined inductors," *IEEE Microw. Wireless Compon. Lett.*, vol. 15, no. 12, pp. 859–861, Dec. 2005.

[7] C.-M. Hung and K. K. O, "A 1.24-GHz monolithic CMOS VCO with phase noise of 137 dBc/Hz at a 3-MHz offset," *IEEE Microw. Guided Wave Lett.*, vol. 9, no. 3, pp. 111–113, Mar. 1999.

[8] Y.-K. Chu and H.-R. Chung, "A fully integrated 5.8 GHz U-NII band 0.18-μm CMOS VCO," *IEEE Microw. Wireless Compon. Lett.*, vol. 13, no. 7, pp. 287–289, Jul. 2003.

[9] R. Aparicio and A. Hajimiri, "A noise-shifting differential colpitts VCO," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1728–1736, Dec. 2002.